Troubleshooting Micro Power Off Mode on Élan™SC300 and ÉlanSC310 Microcontrollers and Evaluation Boards

AMD

Application Note

by Cliff Grant

Micro Power Off mode is a power management mode that allows you to maintain the system date, time, and configuration data when the rest of the system is powered down. This application note addresses some issues regarding Micro Power Off mode. The information in this application note is intended to be used in addition to the documents listed in the Reference Materials section at the end of the application note. The information discussed here applies equally to both Élan™SC300 and ÉlanSC310 microcontrollers. Note that this application note refers specifically to revision D of the Élan™SC300 Microcontroller Data Sheet*, order #18514 and revision B of the* Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.*

MICRO POWER OFF MODE TIMING AND POWER REQUIREMENTS

Micro Power Off mode allows you to remove power from the VCC1, VSYS, VSYS2, VCC5, and, optionally, VMEM power inputs to the Élan™SC300 microcontroller. This allows the RTC timer and RAM contents to be kept valid by using a battery back-up power source on the VCC core and AVCC (analog VCC) pins, which typically should use only 25 µA in this mode.

The system should not be powered up directly into Micro Power Off mode. As described on page 59 of the *Élan™SC300 Microcontroller Data Sheet*, order #18514D, the system must be allowed to fully power up into High-Speed (HS) mode upon initial power application of any power source. Because a battery has insufficient power for the ÉlanSC300 microcontroller to initialize in HS mode, the system design must first power up the ÉlanSC300 microcontroller from the main power source, and not allow the chip to be powered from the battery until after it is fully initialized in HS mode and properly transitioned into Micro Power Off mode. The *Élan™SC300 and Élan™SC310 Microcontrollers Solution For Systems Using A Back-Up Battery Application Note*, order #20746, describes a circuit that is intended to gate the battery off of the ÉlanSC300 microcontroller until after the system has been initialized from the main power source.

The timing sequence and specifications for powering-up, entering, and exiting Micro Power Off mode described on pages 99–101 of the ÉlanSC300 microcontroller data sheet must be met. Be sure to observe the power-up (and power-down) voltage sequencing specifications listed in the Notes section at the bottom of Table 51 on page 99 of the ÉlanSC300 microcontroller data sheet.

Refresh can be either enabled or disabled during Micro Power Off mode, and the VMEM power can be optionally removed, provided that either the memory is also powered off or all DRAM interface signals are kept at 0 V. Note that there are two possible timing sequences shown on page 101 for entering Micro Power Off mode with or without DRAM refresh enabled. For documentation showing an external workaround for disabling DRAM refresh prior to entering Micro Power Off mode, refer to Errata #EB30 (available by contacting your AMD FAE).

RSTDRV SIGNAL TIMING

As described on page 58 of the ÉlanSC300 microcontroller data sheet, the RSTDRV signal is High True output of the ÉlanSC300 microcontroller and is a function of the internal core's reset state, the state of the $\overline{\text{RESIN}}$ and $\overline{\text{IORESET}}$ signals, and the value for the PLL start-up timer in the Clock Control Register (Index 8Fh). Figures 32 and 33 on page 100 of the ÉlanSC300 data sheet provide timing information for the RSTDRV signal.

PROGRAMMER'S REFERENCE MANUAL

In a brief discussion about Off mode on page 1-7, the *Élan™SC300 Microcontroller Programmer's Reference Manual,* order #18470B, states, "The system cannot be programmed to enter Off mode directly. The only method of Off mode entry is by expiration of the Suspend to Off Mode Timer Register at Index 87h."

In the Micro Power Off Mode section on page 1-40, the manual states, "There is no software processing required or available to enter the Micro Power Off mode. For most applications, Micro Power Off mode is

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like completely turning off the power to the system while maintaining real-time clock operation and CMOS contents. The system enters Micro Power Off mode immediately when $\overline{\text{IORESET}}$ is sampled Low." Also on page 1-40 are more details and software information concerning the difference between power-up cold boot and exiting Micro Power Off mode.

Table 5-2 on page 5-3 of the programmer's reference manual lists the mandatory configuration bit settings that must be written soon after reset. See pages 5-10 and 5-11 for a list of registers related to controlling power management functions.

CRYSTAL AND PLL START-UP

Here are a few considerations when analyzing problems with power-on startup or getting the ÉlanSC300 microcontroller to wake up from Micro Power Off mode.

- If everything is working correctly, the ÉlanSC300 microcontroller should not take more than one second to power up. Refer to the ÉlanSC300 microcontroller data sheet timing specifications in Table 51 on page 99 and Figure 32 on page 100. These specifications show t_1 = 1 s, typical (0.5 s for the crystal to stabilize + 0.25 s for the PLLs to stabilize + 0.25 s system-design margin). The VCC power-on sequence shown in the footnotes at the bottom of Table 51 must also be met in addition to the other timing specifications.
- Refer to the crystal specifications on pages 95 and 96 in the ÉlanSC300 microcontroller data sheet and pay special attention to the component value limits listed in Table 49. The values of C_D and C_G must be kept within the recommended limits to ensure a reasonable start-up time for the oscillator circuit.
- Refer to Appendix C in the *ÉlanSC300 Microcontroller Evaluation Board User's Manual* for board layout suggestions.
- Refer to the Loop Filters section on page 97 in the ÉlanSC300 microcontroller data sheet and make sure that you program the Clock Control Register (Index 8Fh) to the recommended value of 256 ms or greater. The value programmed into this register determines the pulse width of the RSTDRV signal when exiting Micro Power Off mode. This allows at least 200 ms for the PLLs to start up when they have been powered down.

  A voltage level between 1 V and 2 V on the LF1–LF4 pins indicates that the PLLs are powered up. All four PLLs should power up with approximately the same timing and this should occur within 200 ms after VCC power is applied and the crystal has stabilized. RSTDRV (a High True output from the microcontroller) should go False when $\overline{\text{RESIN}}$ and $\overline{\text{IORESET}}$ are False and the PLLs are stable, and then should allow the CPU to begin executing instructions.
- The PLLs have a divide chain from which the clocks are built. See page 51 of the ÉlanSC300 microcontroller data sheet. Check to see if one of the PLLs is not powering up. Each of the four LF1–LF4 pins is associated with one of the PLLs:
  - LF1 is the high-speed PLL.
  - LF2 is the intermediate PLL.
  - LF3 is the low-speed PLL.
  - LF4 is the video PLL.

  If either the low-speed or intermediate PLL (the earlier ones in the chain) does not power up, the high-speed and video PLLs (the last ones in the chain) are prevented from powering up. If the intermediate PLL does not power up, then it will prevent all other PLLs from powering up.
- You can also check the voltage levels of LF1–LF4 to determine if the microcontroller is in the desired PMM mode. When one of the LF1–LF4 pins reaches its normal voltage level, does it stay stable or decay again? Not staying stable (High) indicates that the PLL has turned back off as a result of the microcontroller changing PMM modes. You can also program PGP0–PGP3 to automatically indicate when changes occur to or from different PMM modes.
- When exiting Micro Power Off mode, the specification for VCC High to $\overline{\text{IORESET}}$ High delay time (see t_5 in Figure 33 on page 100 of the ÉlanSC300 microcontroller data sheet) shows 5-µs minimum. However, this may not allow enough time if the PLLs need more time to power up. The ÉlanSC300 microcontroller evaluation board uses an RC circuit (1-MΩ series resistor with a 1-µF cap to ground) that provides approximately 450 ms of delay between VSYS and RSTDRV High and $\overline{\text{IORESET}}$ deassertion. This RC circuit is shown on page D-20 (schematic sheet #19) of the *Élan™SC300 Microcontroller Evaluation Board User's Manual*. You may also want to increase the RC time delay to the 450-ms value used on the evaluation board. On the other hand, if the PLLs are not powered up to their normal levels by the time the RSTDRV goes back Low, you may need to decrease this (t_5) RC delay or increase the PLL start-up time value in the Clock Control Register (Index 8Fh), which can be programmed for up to 1 s.
- Measure the start-up times of the 32-kHz crystal and the LF1–LF4 relative to the VCC, $\overline{\text{RESIN}}$, $\overline{\text{IORESET}}$, and RSTDRV signals to determine where the problem in power-on sequence is occurring. If everything mentioned previously is working correctly, you should see $\overline{\text{ROMCS}}$ access

soon afterwards. If $\overline{\text{ROMCS}}$ occurs in a reasonable amount of time, then focus on the software instructions being read by the CPU.

- Check to make sure that the ÉlanSC300 microcontroller is configured for the desired bus mode (that is, Full/Maximum ISA, Internal LCD, or Local Bus) by reading bits 5 and 6 in the Memory Configuration 1 Register (Index 66h). Refer to page 68 in the ÉlanSC300 microcontroller data sheet for a description of how to configure the bus mode at reset. Note that the timing diagram in Figure 8 is only for the purposes of demonstrating when the processor samples the CFG0–CFG1 bits and is not intended to imply timing sequence requirements for VCC, $\overline{\text{RESIN}}$, and $\overline{\text{IORESET}}$. These timing requirements are specified on pages 99–101 of the data sheet.
- If you are having problems with high current in Micro Power Off mode, then refer to the next section in this application note for the description of a known problem with high current on the ÉlanSC300 microcontroller evaluation board. If you are experiencing a different problem with higher than expected current, then isolate the VCC power input that is drawing the current to the ÉlanSC300 microcontroller's internal power planes. Next, check the voltage level on each individual signal powered by (VCCIO) or clamped to (VCC Clamp) that power plane to determine if that plane is being back-powered by one or more pins. If you leave DRAM powered up, then you must also either leave VMEM powered up or make sure that the ÉlanSC300 microcontroller's DRAM control signals are held at 0 V.
- If you are still unable to solve your problem, then you should attempt to isolate the problem. How many boards and ÉlanSC300 microcontroller chips are having the problem? Could the problem be isolated to a single board or chip instead of the design? Again, which power pin(s) are drawing current and which Loop Filters are active? What is the bus mode configuration? What is the DRAM configuration?

HIGH CURRENT PROBLEM IN MICRO POWER OFF MODE ON THE ÉLANSC300 EVALUATION BOARD

Although this problem is described in reference to the evaluation board, the information contained here can also be correlated to other customer-specific applications if similar symptoms appear.

The problem is defined by a high-current consumption on the VCC Core and Analog VCC inputs to the ÉlanSC300 microcontroller, when the VCC core typically draws between 29 mA and 30 mA and the AVCC approximately draws between 2 µA and 2.5 µA. The normal Micro Power Off mode power consumption is approximately 4 µA for VCC (core) and 19.8 µA for AVCC (see Typical Power Numbers on page 82 of the ÉlanSC300 microcontroller data sheet). The ÉlanSC300 evaluation board has exhibited this problem under three conditions:

1. At initial power-on
2. After pressing the Micro Power Off mode button twice in a very tight window of time
3. After entering Micro Power Off mode normally and then pressing the RESET button

- The initial power-on demonstrates this problem because the evaluation board powers up in Micro Power Off mode, with $\overline{\text{RESIN}}$ going High after approximately 1 s and $\overline{\text{IORESET}}$ kept Low by the logic until switch SW5 (the Micro Power Off mode button) is pressed. This is shown on page D-20 (schematic sheet #19) of the ÉlanSC300 and ÉlanSC310 evaluation board manuals. This does not allow the microcontroller to power up into High-Speed mode and properly initialize itself. A detailed description is provided on page 59 of the ÉlanSC300 microcontroller data sheet, part of which states, "The system should not be powered up directly into Micro Power Off mode. The system must be allowed to fully power up into High Speed mode upon initial power application of any power source."

  In the absence of any violation in the power-on timing specifications, the only external anomaly (other than the high-current consumption on the VCC core and Analog VCC) is that the Loop Filters are powered on to within a general approximation of their normal operating voltage of between 1 V and 1.6 V. This is the only external indication that represents the state of whether or not the internal PLLs are powered up and running. The conclusion that can be drawn here is that if the ÉlanSC300 microcontroller is not properly initialized and the PLLs are powered up while in this undefined state, then the microcontroller will draw an abnormally high level of current. Because this is documented in the data sheet, this should be considered a problem unique to the evaluation board design.
- The second occurrence of this high-current condition happens after the ÉlanSC300 microcontroller is properly initialized in High-Speed mode and then taken into a normal Micro Power Off mode.

  While the chip is in the Micro Power Off mode, if you press the Micro Power Off mode button twice in a very tight window of time (approximately between 400 ms and 500 ms), then it is possible to end up in Micro Power Off mode with the high-current problem.

Although the ÉlanSC300 microcontroller data sheet and programmer's reference manual do not specify timing requirements necessary before asserting $\overline{\text{IORESET}}$ and going into Micro Power Off mode, the RSTDRV signal (the High True system reset output from the ÉlanSC300 microcontroller) should be monitored to determine the following:

– The PLLs have stabilized.

– The CPU core has successfully exited the previous session of Micro Power Off mode.

– $\overline{\text{IORESET}}$ is not asserted again until RSTDRV has been deasserted by the CPU (RSTDRV stays True until $\overline{\text{IORESET}}$ deasserts High and the PLLs are stable).

Understanding the above manifestation of the high-current problem requires some understanding of the way Micro Power Off mode is implemented on the evaluation board. Refer to page D-20 (schematic sheet #19) of the ÉlanSC300 or ÉlanSC310 microcontroller evaluation board manual.

When you are already in Micro Power Off mode and you press the Micro Power Off button to wake up, the following occurs:

– P5VOLT (used to generate VCC5, VCCSYS, VCCSYS2, VCCMEM, and VCC1) is immediately switched on (5 V).

– RSTDRV (with its I/O pin powered by VCCSYS) goes True immediately following VCCSYS, while an RC circuit delays $\overline{\text{IORESET}}$ from being deasserted for approximately 450 ms (the specification requires 5 µs minimum).

The CPU core keeps its internal reset True during Micro Power Off mode because the PLLs are normally off and the Loop Filters (LF1–LF4) are at 0 V. Consequently, during Micro Power Off mode, RSTDRV, which is asserted High internally, sets at what would be a logic High (0.7 V to 0.8 V) instead of 0 V on the output pin. When VCCSYS is re-applied, the RSTDRV output is immediately reasserted High at 5 V. Approximately 450 ms after the 5-V power is applied and RSTDRV is True, $\overline{\text{IORESET}}$ goes False and LF1–LF4 are allowed to begin charging up to their powered-on levels of between 1 V and 1.6 V.

When the LF1–LF4 power is stable and the PLLs are also assumed to be stable, the RSTDRV signal goes back Low (False). The ÉlanSC300 microcontroller should be fully powered up and in High-Speed mode at this time. When the Micro Power Off mode button is pressed again, $\overline{\text{IORESET}}$ is reasserted immediately (with $\overline{\text{RESIN}}$ held High). Two DRAM refresh cycles later, P5VOLT will be switched off. This causes a brief glitch on the RSTDRV line because it attempts to go High when, simultaneously, $\overline{\text{IORESET}}$ is asserted and the VCCSYS is lost to its I/O driver. There is no direct correlation of any known problems related to this glitch. At this point everything is again in normal Micro Power Off mode.

In the previous scenario, the high-current failure occurs on the evaluation board when the following common event takes place:

When the Micro Power Off mode button is pressed the second time *exactly* when RSTDRV is going back Low, $\overline{\text{IORESET}}$ goes True again at the same time that RSTDRV is going False from the previous Micro Power Off mode session.

This event apparently sends conflicting information to the internal state machine inside the ÉlanSC300 microcontroller (that is, RSTDRV going False, allowing the CPU to begin executing instructions in High-Speed mode, and at the same time $\overline{\text{IORESET}}$ going True, telling the CPU to go back into Micro Power Off mode). This event also causes the glitch on RSTDRV to occur at approximately the same time, which may or may not be a contributing factor, because it does not seem to cause any problems with different timing. The only external indication of an anomaly (other than the current consumption on the VCC core and Analog VCC) is that the Loop Filters remain powered on to within a general approximation of their normal High-Speed operating voltage of between 1 V and 1.6 V. This indicates that the internal PLLs are powered up and running when they should be powered off.

The second condition in which the problem occurs is when Micro Power Off mode is entered normally and no high-current condition exists. If the Micro Power Off mode button is pressed twice in less than 450 ms, then $\overline{\text{IORESET}}$ remains deasserted (due to the 450-ms RC delay on $\overline{\text{IORESET}}$ deassertions). Because $\overline{\text{IORESET}}$ remained asserted without interruption, the ÉlanSC300 microcontroller never exits Micro Power Off mode, RSTDRV remains asserted internally, and the PLLs remain powered down.

■ The third condition in which the problem occurs is when you enter Micro Power Off mode normally and then press the RESET button. While $\overline{\text{IORESET}}$ remains Low (indicating Micro Power Off mode), pressing the RESET button makes the $\overline{\text{RESIN}}$ signal pulse Low. This causes the ÉlanSC300 microcontroller to attempt to initialize itself and the PLLs to power up, indicated by LF1–LF4 going High immediately after $\overline{\text{RESIN}}$ goes Low. The timing for this scenario is not an issue, assuming that enough time has passed for the ÉlanSC300 microcontroller to properly enter Micro Power Off mode before the RESET button is pressed.

Again, as in the previous conditions, the only external indication of an anomaly (other than the 30-mA current consumption on the VCC core and Analog VCC) is that the Loop Filters remain powered on to within a general approximation of their normal High-Speed operating voltage of between 1 V and 1.6 V. This indicates that the internal PLLs are powered up and running. This scenario is very much like the first one discussed, because at the point that $\overline{\text{RESIN}}$ is driven Low, the ÉlanSC300 microcontroller is no longer in Micro Power Off mode, and it functions the same as it would for a cold-boot sequence in which it attempts to go directly into High-Speed mode from power on.

REFERENCE MATERIAL

- *Élan™SC300 Microcontroller Data Sheet*, order #18514D
- *Élan™SC300 Programmer's Reference Manual,* order #18470B
- *Élan™SC300 Microcontroller Evaluation Board User's Manual* (http://www.amd.com/Embedded Processors/Available Literature)
- *Élan™SC300 and Élan™SC310 Microcontrollers Solution For Systems Using A Back-Up Battery Application Note*, order #20746
- Errata list, rev. B3 or rev. B4 (contact your AMD FAE)
- *Élan™SC310 Microcontroller Data Sheet*, order #20668
- *Élan™SC310 Programmer's Reference Manual,* order # 20665
- *Élan™SC310 Microcontroller Evaluation Board User's Manual* (http://www.amd.com/Embedded Processors/Available Literature)