# HM628511HI Series

4M High Speed SRAM (512-kword × 8-bit)

HITACHI

ADE-203-1035A (Z)
Rev. 1.0
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## Description

The HM628511HI Series is a 4-Mbit high speed static RAM organized 512-k word × 8-bit. It has realized high speed access time by employing CMOS process (4-transistor + 2-poly resistor memory cell)and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in 400-mil 36-pin plastic SOJ.

## Features

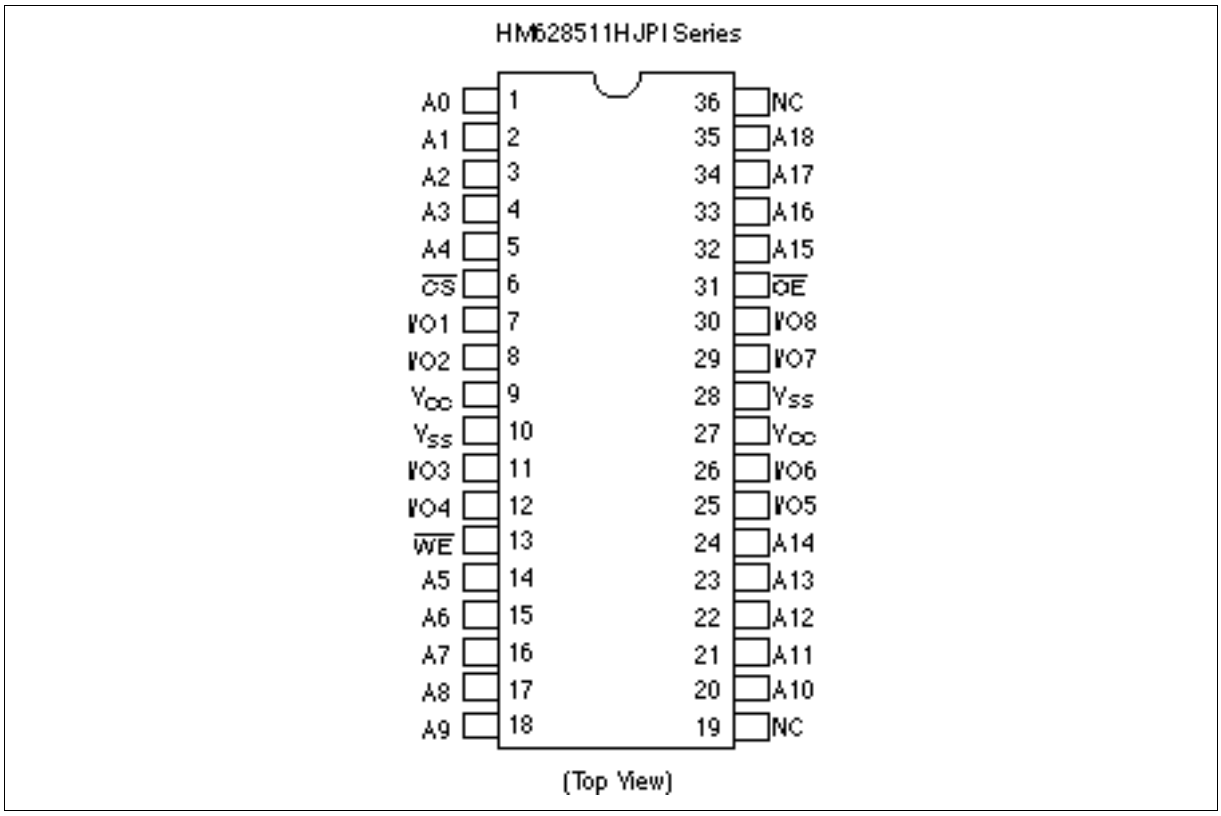
- Single 5.0 V supply : 5.0 V ± 10 %
- Access time 12 /15 ns (max)
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - — All inputs and outputs
- Operating current : 160 / 140 mA (max)
- TTL standby current : 60 / 50 mA (max)
- CMOS standby current : 5 mA (max)
- Center $V_{CC}$ and $V_{SS}$ type pinout
- Temperature range: –40 to 85°C

Hitachi semiconductor

## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HM628511HJPI-12 | 12 ns | 400-mil 36-pin plastic SOJ (CP-36D) |
| HM628511HJPI-15 | 15 ns | |

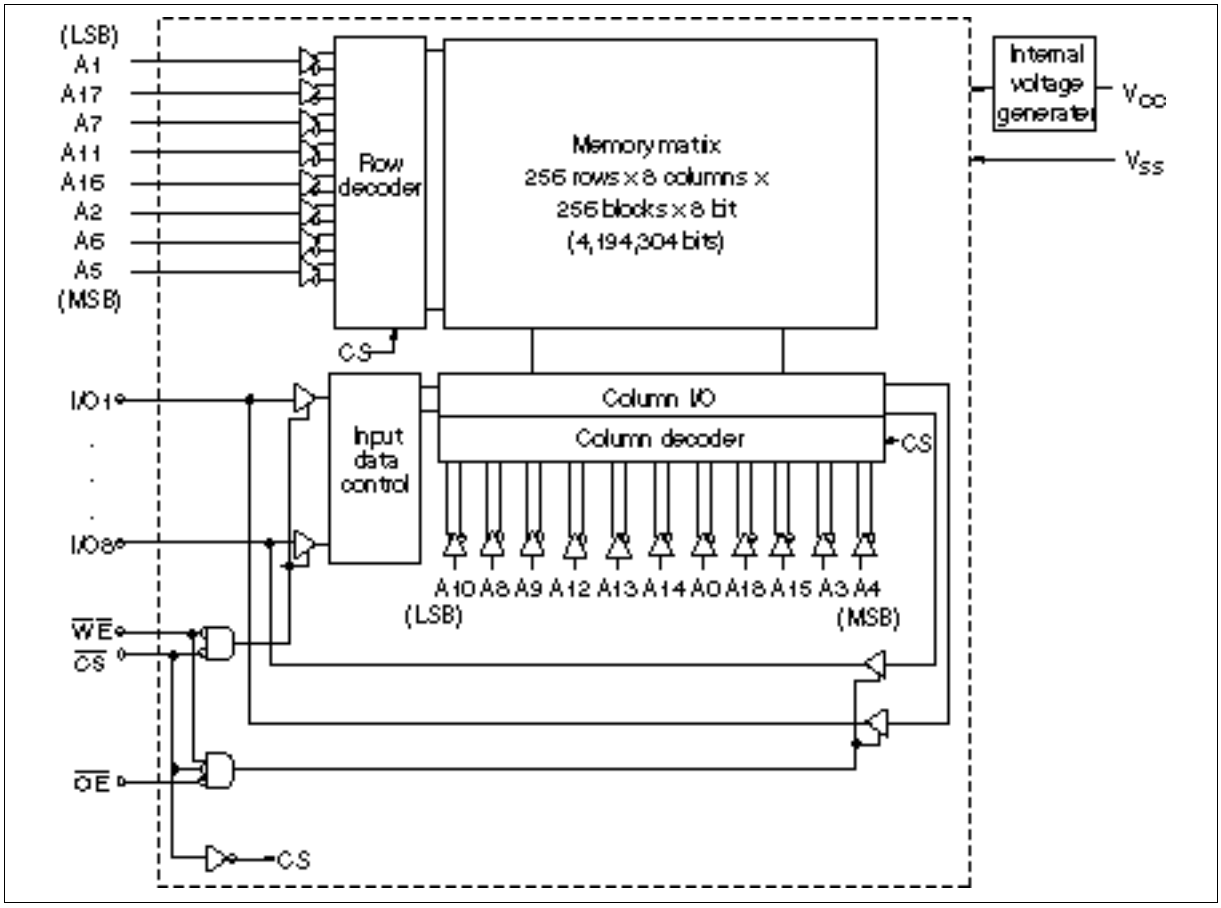
## Pin Arrangement



## Pin Description

| Pin name | Function |
|---|---|
| A0 to A18 | Address input |
| I/O1 to I/O8 | Data input/output |
| $\overline{CS}$ | Chip select |
| $\overline{OE}$ | Output enable |
| $\overline{WE}$ | Write enable |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |
| NC | No connection |

## Block Diagram



## Operation Table

| CS | OE | WE | Mode | $V_{CC}$ current | I/O | Ref. cycle |
|---|---|---|---|---|---|---|
| H | × | × | Standby | $I_{SB}$, $I_{SB1}$ | High-Z | — |
| L | H | H | Output disable | $I_{CC}$ | High-Z | — |
| L | L | H | Read | $I_{CC}$ | Dout | Read cycle (1) to (3) |
| L | H | L | Write | $I_{CC}$ | Din | Write cycle (1) |
| L | L | L | Write | $I_{CC}$ | Din | Write cycle (2) |

Note: ×: H or L

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | –0.5 to +7.0 | V |
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | –0.5*[1] to $V_{CC}$+0.5*[2] | V |
| Power dissipation | $P_T$ | 1.0 | W |
| Operating temperature | Topr | –40 to +85 | °C |
| Storage temperature | Tstg | –55 to +125 | °C |
| Storage temperature under bias | Tbias | –40 to +85 | °C |

Notes: 1. $V_T$ (min) = –2.0 V for pulse width (under shoot) 8 ns
2. $V_T$ (max) = $V_{CC}$+2.0 V for pulse width (over shoot) 8 ns

## Recommended DC Operating Conditions (Ta = –40 to +85°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$*[3] | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$*[4] | 0 | 0 | 0 | V |
| Input voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$ + 0.5*[2] | V |
| | $V_{IL}$ | –0.5*[1] | — | 0.8 | V |

Notes: 1. $V_{IL}$ (min) = –2.0 V for pulse width (under shoot) 8 ns
2. $V_{IH}$ (max) = $V_{CC}$+2.0 V for pulse width (over shoot) 8 ns
3. The supply voltage with all $V_{CC}$ pins must be on the same level.
4. The supply voltage with all $V_{SS}$ pins must be on the same level.

## DC Characteristics (Ta = –40 to +85°C, $V_{CC}$ = 5.0 V ± 10 %, $V_{SS}$ = 0V)

| Parameter | | Symbol | Min | Typ*[1] | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Input leakage current | | $\|I_{LI}\|$ | — | — | 2 | µA | Vin = $V_{SS}$ to $V_{CC}$ |
| Output leakage current | | $\|I_{LO}\|$ | — | — | 2 | µA | Vin = $V_{SS}$ to $V_{CC}$ |
| Operation power supply current | 12 ns cycle | $I_{CC}$ | — | — | 160 | mA | Min cycle<br>CS = $V_{IL}$, Iout = 0 mA<br>Other inputs = $V_{IH}/V_{IL}$ |
| | 15 ns cycle | $I_{CC}$ | — | — | 140 | | |
| Standby power supply current | 12 ns cycle | $I_{SB}$ | — | — | 60 | mA | Min cycle, CS = $V_{IH}$,<br>Other inputs = $V_{IH}/V_{IL}$ |
| | 15 ns cycle | $I_{SB}$ | — | — | 50 | | |
| | | $I_{SB1}$ | — | 0.1 | 5 | mA | f = 0 MHz<br>$V_{CC}$ CS $V_{CC}$ - 0.2 V,<br>(1) 0 V Vin 0.2 V or<br>(2) $V_{CC}$ Vin $V_{CC}$ - 0.2 V |
| Output voltage | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 8 mA |
| | | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = –4 mA |

Notes: 1. Typical values are at $V_{CC}$ = 5.0 V, Ta = +25°C and not guaranteed.

## Capacitance (Ta = +25°C, f = 1.0 MHz)

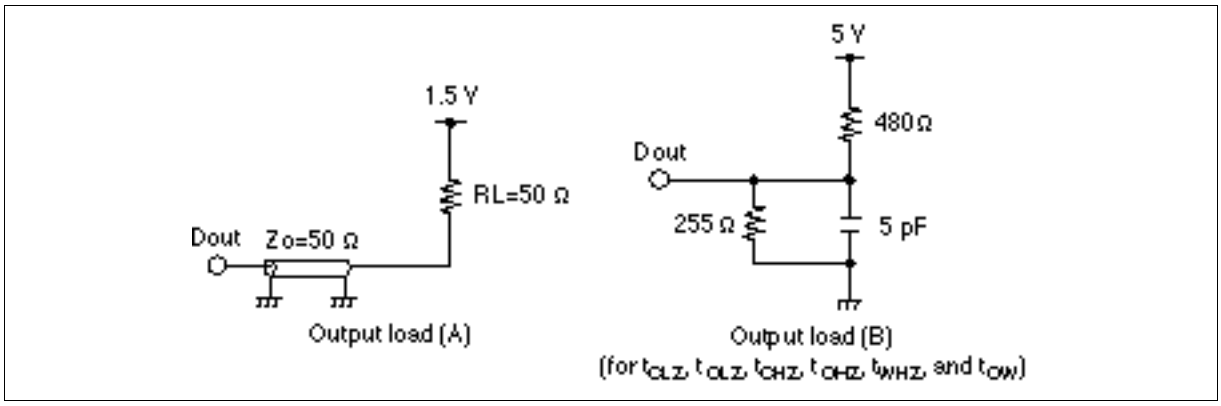
| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input capacitance*[1] | Cin | — | — | 6 | pF | Vin = 0 V |
| Input/output capacitance*[1] | $C_{I/O}$ | — | — | 8 | pF | $V_{I/O}$ = 0 V |

Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics (Ta = –40 to +85°C, $V_{CC}$ = 5.0 V ± 10 %, unless otherwise noted.)

### Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)




### Read Cycle

| | | HM628511HI | | | | | |
|---|---|---|---|---|---|---|---|
| | | -12 | | -15 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Read cycle time | $t_{RC}$ | 12 | — | 15 | — | ns | |
| Address access time | $t_{AA}$ | — | 12 | — | 15 | ns | |
| Chip select access time | $t_{ACS}$ | — | 12 | — | 15 | ns | |
| Output enable to outpput valid | $t_{OE}$ | — | 6 | — | 7 | ns | |
| Output hold from address change | $t_{OH}$ | 3 | — | 3 | — | ns | |
| Chip select to output in low-Z | $t_{CLZ}$ | 3 | — | 3 | — | ns | 1 |
| Output enable to output in low-Z | $t_{OLZ}$ | 0 | — | 0 | — | ns | 1 |
| Chip deselect to output in high-Z | $t_{CHZ}$ | — | 6 | — | 7 | ns | 1 |
| Output disable to output in high-Z | $t_{OHZ}$ | — | 6 | — | 7 | ns | 1 |

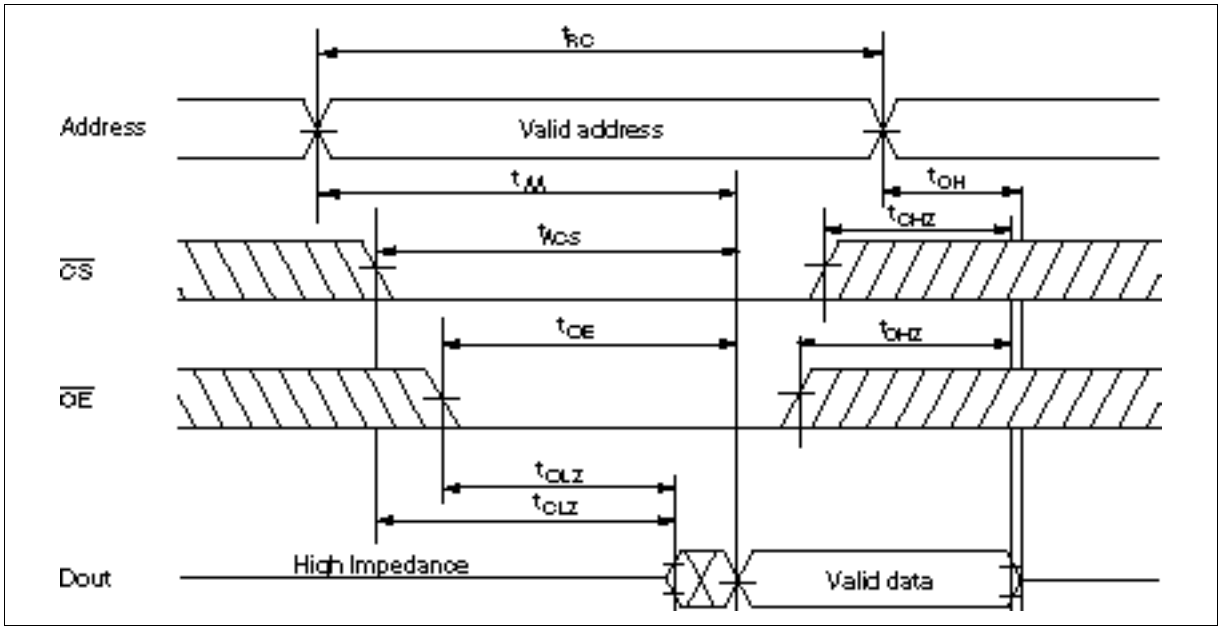
### Write Cycle

| | | HM628511HI | | | | | |
|---|---|---|---|---|---|---|---|
| | | -12 | | -15 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Write cycle time | $t_{WC}$ | 12 | — | 15 | — | ns | |
| Address valid to end of write | $t_{AW}$ | 8 | — | 10 | — | ns | |
| Chip select to end of write | $t_{CW}$ | 8 | — | 10 | — | ns | 9 |
| Write pulse width | $t_{WP}$ | 8 | — | 10 | — | ns | 8 |
| Address setup time | $t_{AS}$ | 0 | — | 0 | — | ns | 6 |
| Write recovery time | $t_{WR}$ | 0 | — | 0 | — | ns | 7 |
| Data to write time overlap | $t_{DW}$ | 6 | — | 7 | — | ns | |
| Data hold from write time | $t_{DH}$ | 0 | — | 0 | — | ns | |
| Write disable to output in low-Z | $t_{OW}$ | 3 | — | 3 | — | ns | 1 |
| Output disable to output in high-Z | $t_{OHZ}$ | — | 6 | — | 7 | ns | 1 |
| Write enable to output in high-Z | $t_{WHZ}$ | — | 6 | — | 7 | ns | 1 |

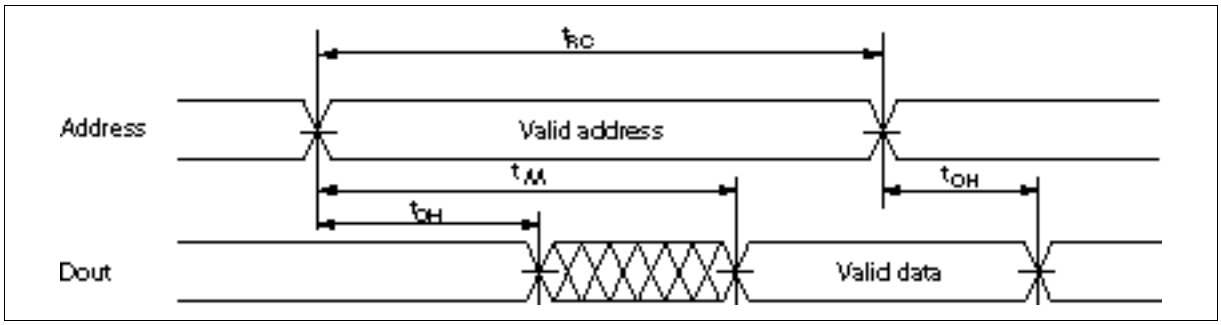
Note:
1. Transition is measured ±200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
2. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{WE}$ and/or $\overline{CS}$ must be high during address transition time.
4. if $\overline{CS}$ and $\overline{OE}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.
6. $t_{AS}$ is measured from the latest address transition to the later of $\overline{CS}$ or $\overline{WE}$ going low.
7. $t_{WR}$ is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the first address transition.
8. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. $t_{WP}$ is measured from the beginnig of write to the end of write.
9. $t_{CW}$ is measured from the later of $\overline{CS}$ going low to the the end of write.

## Timing Waveforms

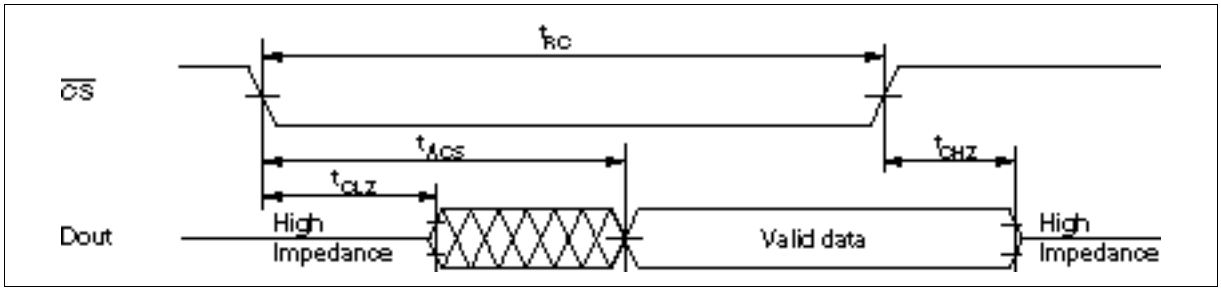
**Read Timing Waveform (1)** (WE = $V_{IH}$)



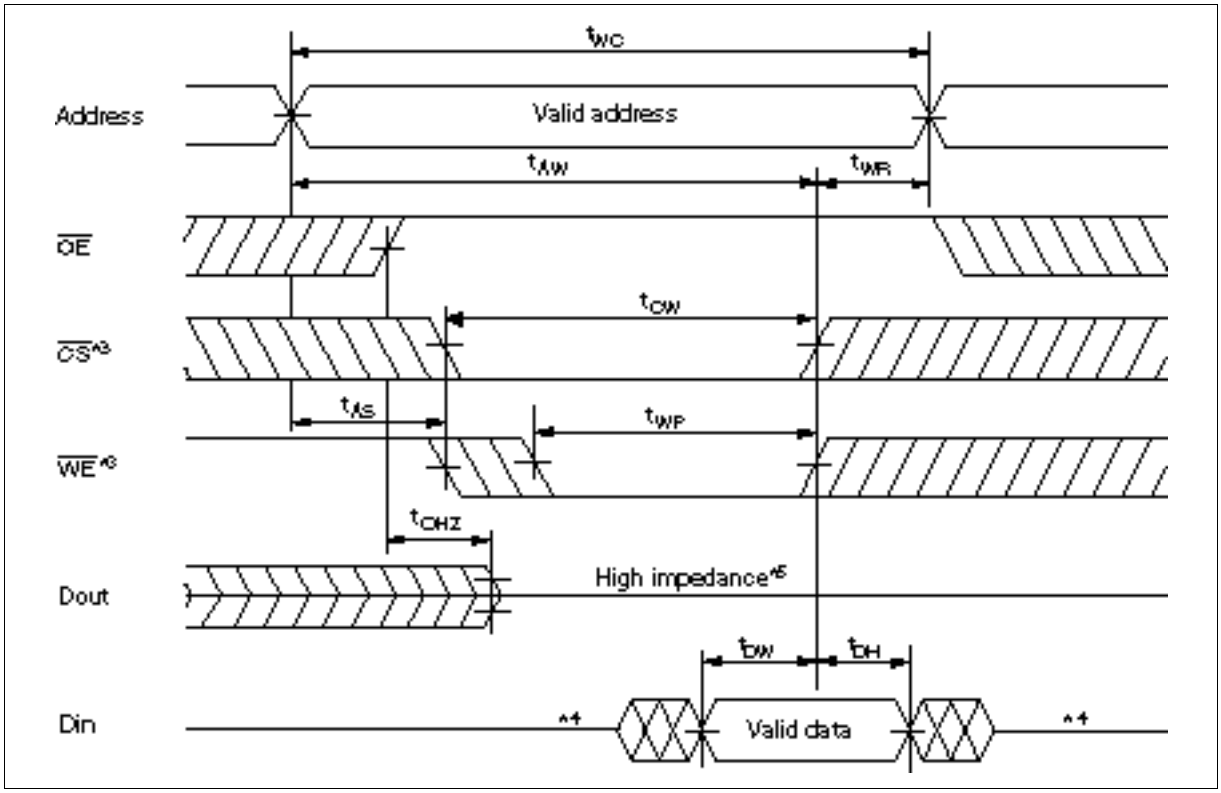

**Read Timing Waveform (2)** (WE = $V_{IH}$, CS = $V_{IL}$, OE = $V_{IL}$)



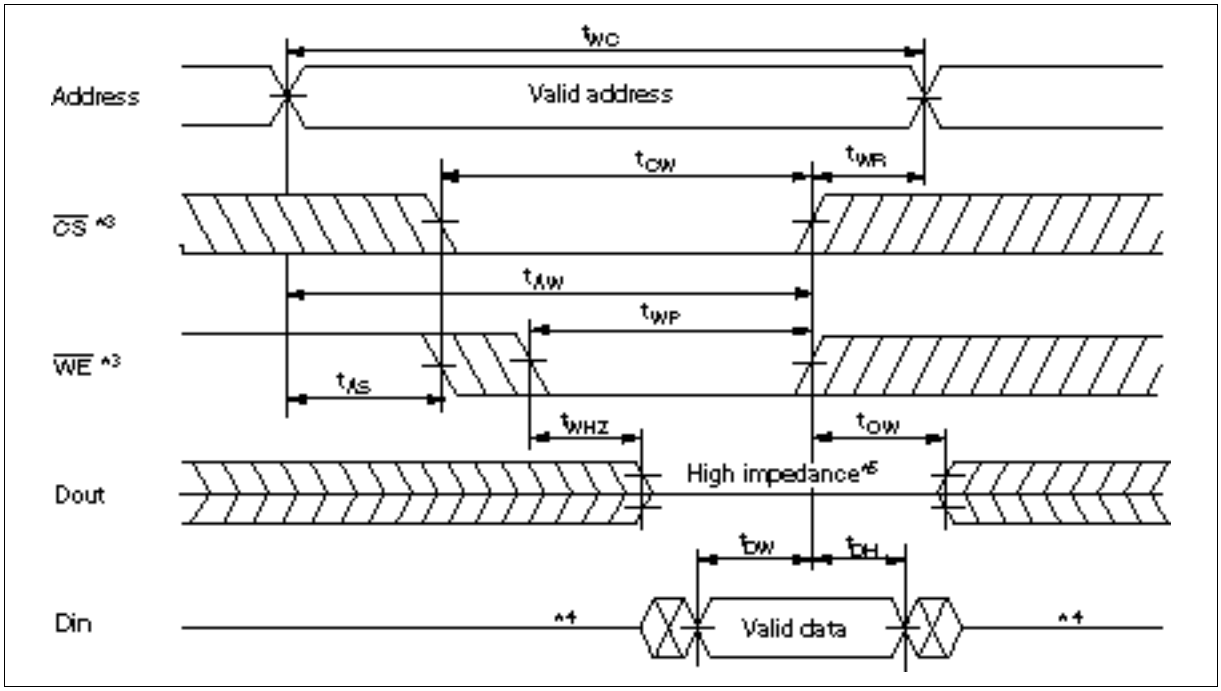
**Read Timing Waveform (3)** (WE = $V_{IH}$, CS = $V_{IL}$, OE = $V_{IL}$)*[2]




**Write Timing Waveform (1)** (WE Controlled)

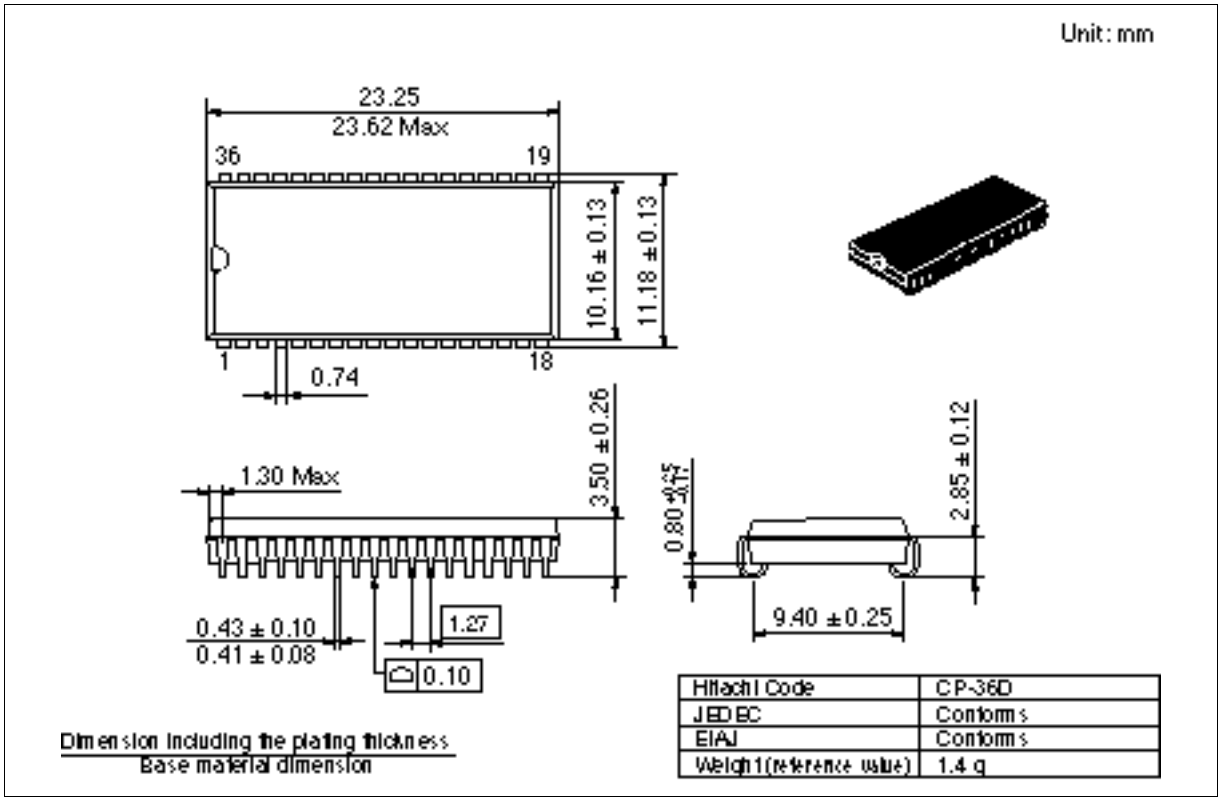


**Write Timing Waveform (2)** (CS Controlled)



## Package Dimensions

**HM628511HJPI Series** (CP-36D)



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## Revision Record

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| 1.0 | Apr. 15, 1999 | Initial issue | | |