BATRON

Specification for
BTHQ 128064AVC1-STF-06-LED02YG-COG

Version November 2004

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DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2004.11.18	First Release. Based on a.) Test Specification: VL-TS-COG-BTC12864-10 REV A, 2004.11.17 b.) VL-QUA-012B REV.W 2004.03.20 According to VL-QUA-012B, LCD size is small because Unit Per Laminate=15 which is more than 6pcs/Laminate.	ZHANG YAN FANG	LIN RONG SHOU

CONTENTS

Specification
of
LCD Module Type
Item No.: COG-BTC12864-10

1. General Description

- 128 x 64 dots STN Yellow Positive Transflective LCD Graphic Module.
- Viewing Direction: 6 O'clock.
- Driving duty: 1/65 Duty, 1/9 bias.
- "ULTRA CHIP" UC1601 (COG) LCD Controller-Driver or equivalent.
- Logic Power Supply: +3V.
- FPC connection.
- Yellow Green LED02 Backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	67.5(W) x 82.5(H) x 8.5(D)(Include FPC and Backlight)	mm
Viewing area (V.A.)	60.00 MIN.(W) x 40.00 MIN.(H)	mm
Active area (A.A.)	56.945(W) x 37.425(H)	mm
Display format	128 x 64	dots
Dot size	0.43(W) x 0.57(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.445(W) x 0.585(H)	mm
Weight:	TBD	grams

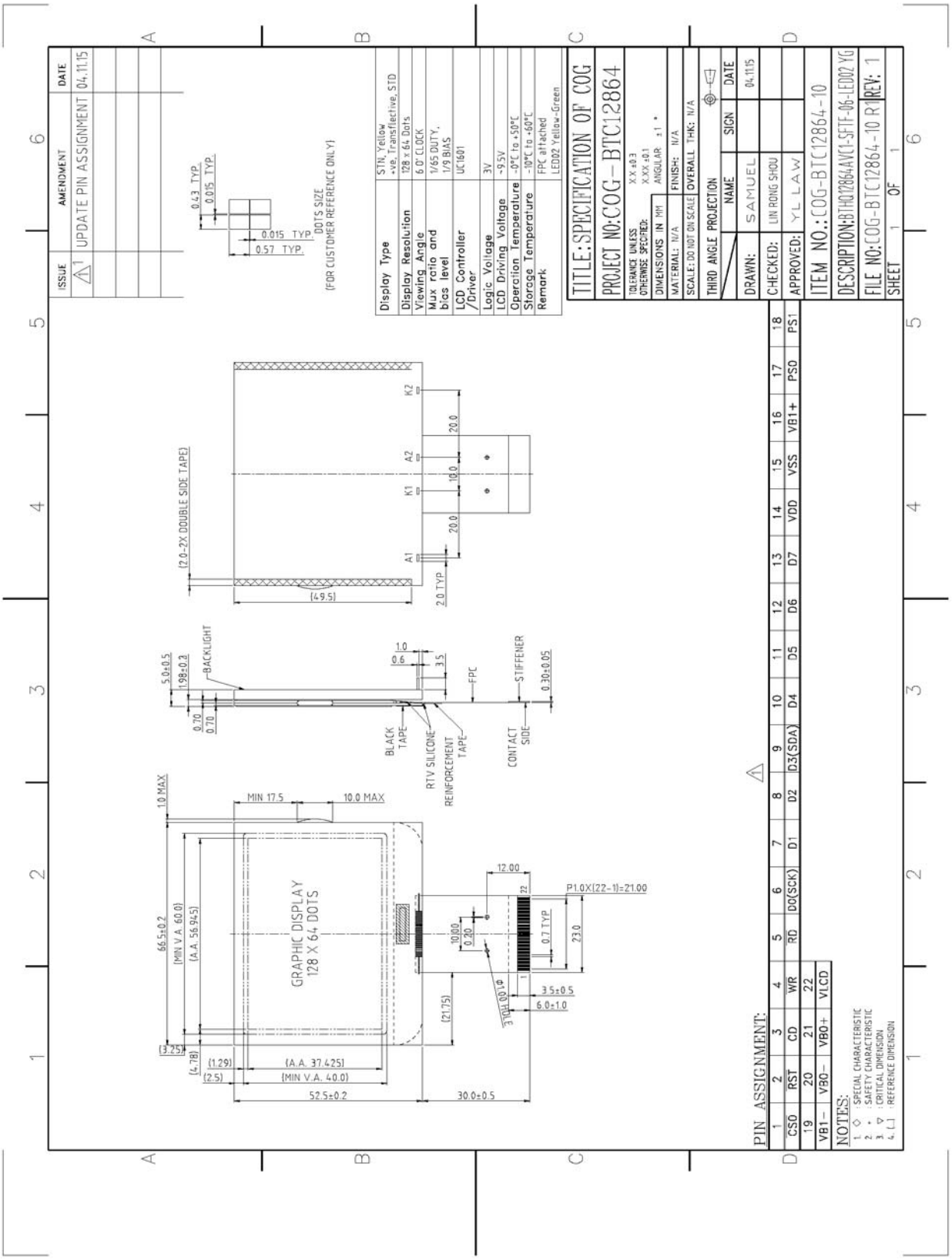

Figure 1: Module Specification

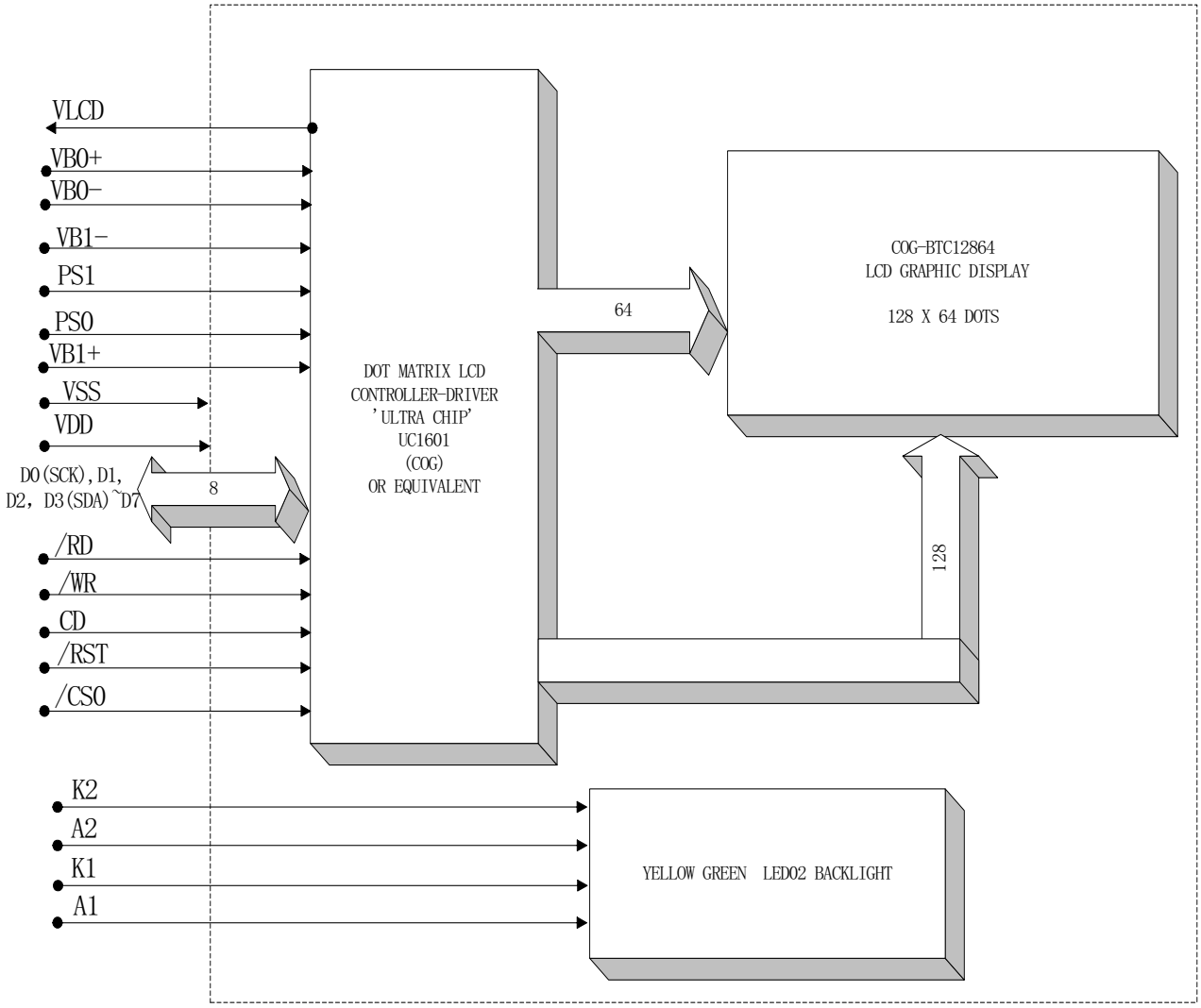

Figure 2: Block diagram

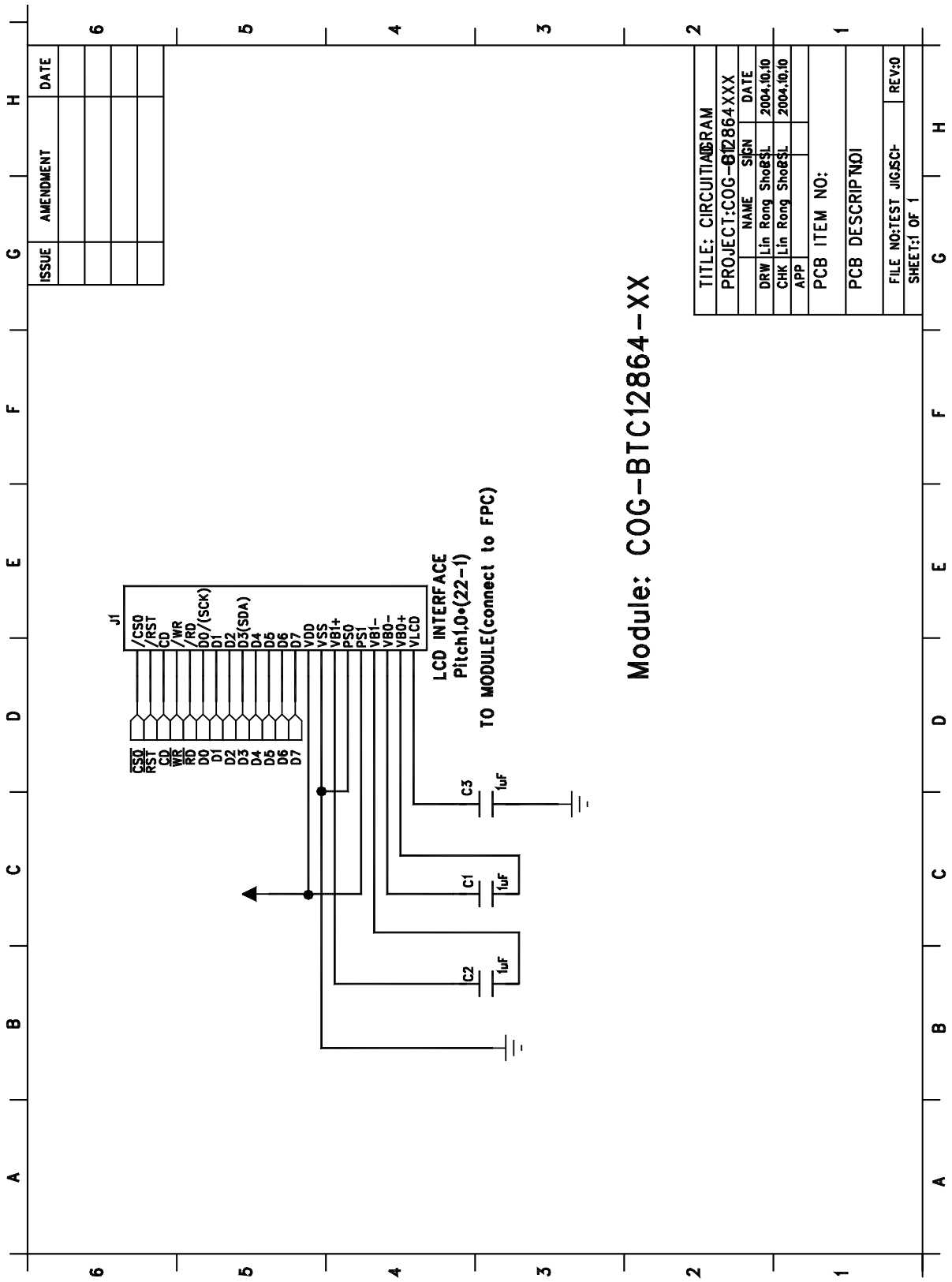

Figure 3: Application Circuit

3. Interface signals

Table 2

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>$\overline{CS0}$</td><td>Chip Select. In parallel mode and S8 mode, chip is selected when $\overline{CS0}$= “L” and CS1= “H”. When the chip is not selected, D[7:0] may be high impedance.</td></tr>
<tr><td>2</td><td>$\overline{RST}$</td><td>When $\overline{RST}$ = “L”, all control registers are re-initialized by their default states. When $\overline{RST}$ is not used, connect the pin to VDD.</td></tr>
<tr><td>3</td><td>CD</td><td>Select Command or Display Data for read/write operation.
“L”: Command “H”: Display data</td></tr>
<tr><td>4</td><td>$\overline{WR}$</td><td rowspan="2">$\overline{RD}$/$\overline{WR}$(WR[1:0]) controls the read/write operation of the host interface.
In parallel mode, RD/WR(WR[1:0]) meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used. Connect to VSS.</td></tr>
<tr><td>5</td><td>$\overline{RD}$</td></tr>
<tr><td>6</td><td>D0(SCK)</td><td rowspan="8">Bi-directional bus for both serial and parallel host interfaces.
In S8 and S9 mode, connect unused pins to VDD or VSS.
<table>
<tr><th></th><th>PS=1x</th><th>Ps=0x</th></tr>
<tr><td>D0</td><td>D0</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td></td></tr>
<tr><td>D2</td><td>D2</td><td></td></tr>
<tr><td>D3</td><td>D3</td><td>SDA</td></tr>
<tr><td>D4</td><td>D4</td><td></td></tr>
<tr><td>D5</td><td>D5</td><td></td></tr>
<tr><td>D6</td><td>D6</td><td></td></tr>
<tr><td>D7</td><td>D7</td><td></td></tr>
</table></td></tr>
<tr><td>7</td><td>D1</td></tr>
<tr><td>8</td><td>D2</td></tr>
<tr><td>9</td><td>D3(SDA)</td></tr>
<tr><td>10</td><td>D4</td></tr>
<tr><td>11</td><td>D5</td></tr>
<tr><td>12</td><td>D6</td></tr>
<tr><td>13</td><td>D7</td></tr>
<tr><td>14</td><td>VDD</td><td>VDD1 is the digital power supply and it should be connected to a voltage source that is no higher than VDD2&3.
VDD2&3 is the analog power supply and it should be connected to the same power source. Minimize the trace resistance for VDD2&3.</td></tr>
<tr><td>15</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>17</td><td>PS0</td><td rowspan="2">PS[1:0] Parallel/Serial.
Serial modes: “LL”: serial (S8) “LH”: serial (S9)
Parallel modes: “HL”: 8080 “HH”: 6800</td></tr>
<tr><td>18</td><td>PS1</td></tr>
<tr><td>16</td><td>VB1+</td><td rowspan="4">LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of CBX value between VBX+ and VBX–. The resistance of these four traces directly affects the SEG driving strength of the resulting LCD module. Minimize the trace resistance is critical in achieving high quality image.</td></tr>
<tr><td>19</td><td>VB1-</td></tr>
<tr><td>20</td><td>VB0-</td></tr>
<tr><td>21</td><td>VB0+</td></tr>
<tr><td>22</td><td>VLCD</td><td>Main LCD Power Supply. A by-pass capacitor CL is optional. When CL is used, connect CL between VLCD and VSS, and keep the trace resistance under 300 Ohm.</td></tr>
<tr><td>-</td><td>A</td><td>Anode of LED Backlight.</td></tr>
<tr><td>-</td><td>K</td><td>Cathode of LED Backlight.</td></tr>
</table>

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings – for IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	V_{DD}	-0.3	+3.3	V
LCD generator supply voltage	V_{DD2}	-0.3	+3.3	V
Analog circuit supply voltage	V_{DD3}	-0.3	+3.3	V
Voltage difference between V_{DD} and $V_{DD2/3}$	$V_{DD2/3}$ - V_{DD}		1.2	V
LCD generated voltage	V_{LCD}	-0.3	+12	V
Any input/output	$V_{IN/}$ / V_{OUT}	-0.4	V_{DD} +0.3	V

Note:

1. V_{DD} is based on V_{SS} = 0V.
2. Stress values listed above may cause permanent damages to the device.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 3V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic & booster)	VDD-VSS		2.85	3.0	3.15	V
LCD driving voltage (Built-in)	VLCD-VSS	At Ta = 0°C, Character mode, VDD = 3V,Note 1	-	9.5	-	V
		At Ta = +25°C, Character mode, VDD = 3V,Note 1	8.9	9.1	9.3	V
		At Ta = +50°C, Character mode, VDD = 3V, Note 1	-	8.6	-	V
Input signal voltage	V_{IH}	"H" level	0.8 VDD1	-	-	V
	V_{IL}	"L" level	-	-	0.2VDD1	V
Supply Current (Logic & booster)	IDD	Character mode, Note 1	-	0.5	0.75	mA
		Checker board mode, Note 1	-	0.54	0.81	mA
Supply Voltage of Yellow Green LED02 backlight	VLED02	Forward current =60mA	1.9	2.1	2.3	V
Wavelength of Yellow Green LED02 backlight	λ	No. of LED chips =2x4=8 dies.	-	570	-	nm
Luminance (on the backlight surface) of backlight			18	24	-	cd/m^2

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

Parallel bus timing characteristics (for 8080 MCU)

At Ta= 0°C to +50°C,VDD=3V±5%.

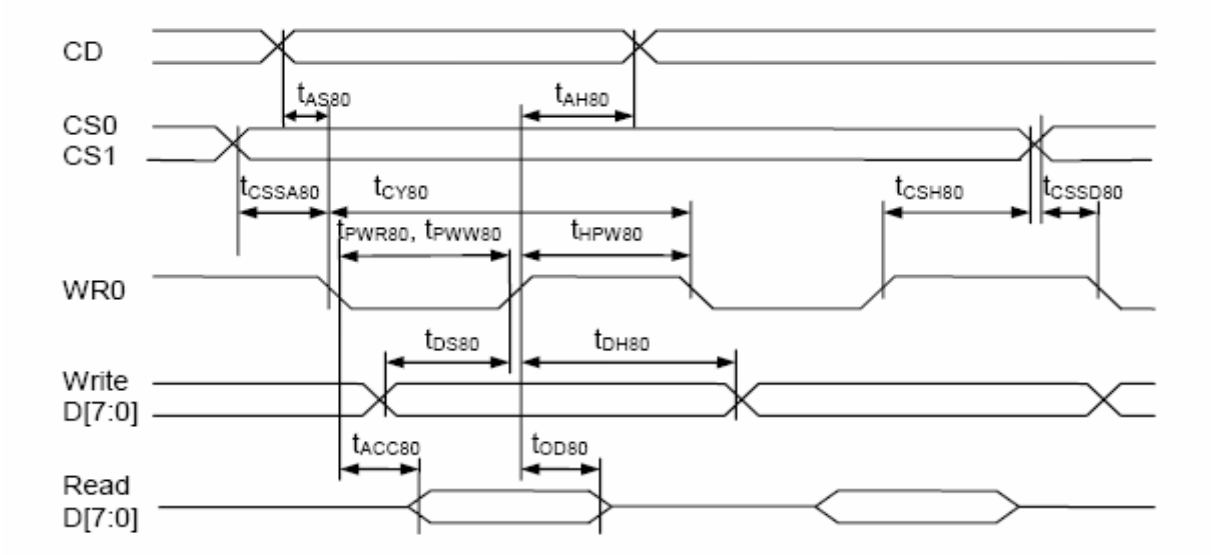

Figure: 4 Parallel Bus Timing Characteristics (for 8080 MCU)

At Ta= 0°C to +50°C,VDD=3V±5%.

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 40	–	nS
t_{CY80}		System cycle time		135	–	nS
t_{PWR80}	WR1	Pulse width (read)		65	–	nS
t_{PWW80}	WR0	Pulse width (write)		65	–	nS
t_{HPW80}	WR0, WR1	High pulse width		65	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 20	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	50 50	nS
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		nS

Parallel bus timing characteristics (for 6800 MCU)

At Ta= 0°C to +50°C,VDD=3V±5%.

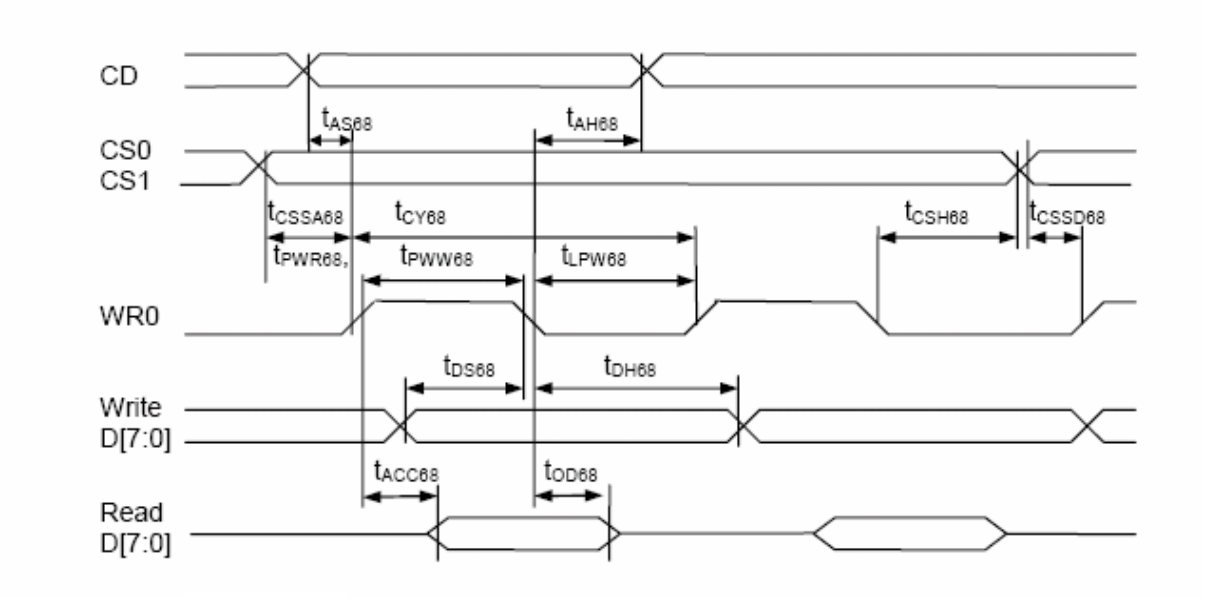

Figure: 5 Parallel Bus Timing Characteristics (for 6800 MCU)

At Ta= 0°C to +50°C,VDD=3V±5%.

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 40	–	nS
t_{CY68}		System cycle time		135	–	nS
t_{PWR68}	WR1	Pulse width (read)		65	–	nS
t_{PWW68}		Pulse width (write)		65	–	nS
t_{LPW68}		Low pulse width		65	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 15	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 10	50 50	nS
T_{CSSA68} T_{CSSD68} T_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		nS

Serial Bus Timing Characteristics (for S8)

At Ta= 0°C to +50°C,VDD=3V±5%.

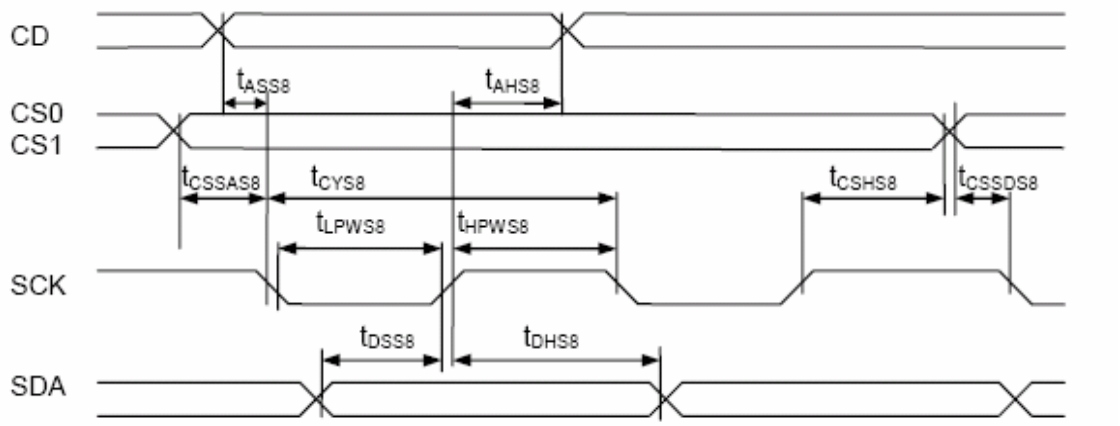

Figure: 6 Serial Bus Timing Characteristics (for S8)

At Ta= 0°C to +50°C,VDD=3V±5%.

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		40	–	nS
t_{CYS8}	SCK	System cycle time		135	–	nS
t_{LPWS8}		Low pulse width		65	–	nS
t_{HPWS8}		High pulse width		65	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 15	–	nS
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 10 20		nS

Serial bus timing characteristics (for S9)

At Ta= 0°C to +50°C,VDD=3V±5%.

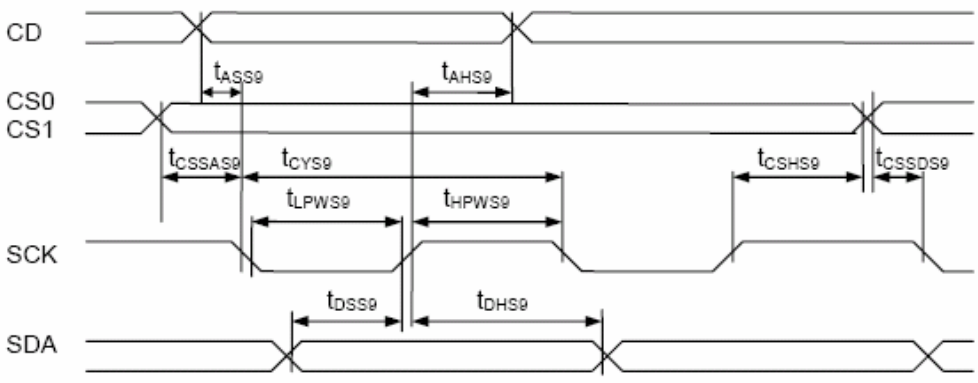

Figure: 7 Serial Bus Timing Characteristics (for S9)

At Ta= 0°C to +50°C,VDD=3V±5%.

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS9}	CD	Address setup time		0	–	nS
t_{AHS9}		Address hold time		40	–	nS
t_{CYS9}	SCK	System cycle time		135	–	nS
t_{LPWS9}		Low pulse width		65	–	nS
t_{HPWS9}		High pulse width		65	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 15	–	nS
t_{CSSAS9} t_{CSSDS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10 20		nS

Reset characteristics

At Ta= 0°C to +50°C,VDD=3V±5%.

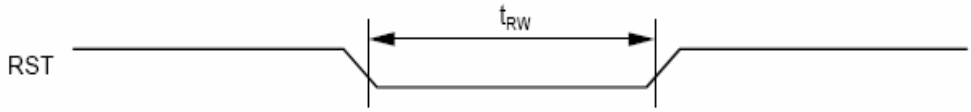

Figure: 8 Reset Characteristics

At Ta= 0°C to +50°C,VDD=3V±5%

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		1	–	µS

6. LCD Cosmetic Conditions

a.) Reference document follow VL-QUA-012B.

b.) LCD size of the product is small.

7. Remark:

a.) Identification labels will be stuck on the module without obstructing the viewing area of display,

b.) Data Modul does not responsible for any polarizer defect after the protective film has been removed from the display.

c.) The stiffener on FPC/FFC/COF must not be bent during or after assembly.