

## **NTE3882 Integrated Circuit NMOS, Counter Timer Control (CTC)**

### **Description:**

The NTE3882 Counter Timer Circuit (CTC) is a programmable, four channel device in a 28-Lead DIP type package that provides counting and timing functions for the NTE3880. The NTE3880 configures the NTE3882's four independent channels to operate under various modes and conditions as required.

The internal structure of the NTE3882 consists of an NTE3880 bus interface, internal control logic, four counter channels, and interrupt control logic. Each channel has an interrupt vector for automatic interrupt vectoring, and interrupt priority is determined by channel number with channel 0 having the highest priority.

The channel logic is composed of 2 registers, 2 counters and control logic. The registers include an 8-bit time constant register and an 8-bit channel control register. The counters include an 8-bit readable down counter and an 8-bit prescaler. The prescaler may be programmed to divide the system clock by either 16 or 256.

### **Structure:**

- N-Channel Silicon Gate Depletion Load Technology
- Single 5V Supply
- Single Phase 5V Clock
- Four Independent Programmable 8-Bit Counter/16-Bit Timer Channels

### **Features:**

- Each Channel may be Selected to Operate in Either a Counter Mode or Timer Mode
- Programmable Interrupts on Counter or Timer States
- A Time Constant Register Automatically Reloads, the Down Counter at Zero and the Cycle is Repeated
- Readable Down Counter Indicates Number of Counts-to-Go until Zero
- Selectable 16 or 256 Clock Prescaler for Each Timer Channel
- Selectable Positive or Negative Trigger may Initiate Timer Operation
- Three Channels have Zero Count/Timeout Outputs capable of Driving Darlington Transistors
- Daisy Chain Priority Interrupt Logic Included to Provide for Automatic Interrupt Vectoring without External Logic
- All Inputs and Outputs Fully TTL Compatible

**Absolute Maximum Ratings:**

Temperature Under Bias ..... 0° to +70°C  
 Storage Temperature Range ..... –65° to +150°C  
 Voltage On Any Pin With Respect to GND ..... –0.3V to +7V  
 Power Dissipation ..... 0.8W

Note 1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC Characteristics:** ( $T_A = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Input Low Voltage	$V_{ILC}$		–0.3	–	0.45	V
Clock Input High Voltage	$V_{IHC}$		$V_{CC}-0.6$	–	$V_{CC}+3$	V
Input Low Voltage	$V_{IL}$		–0.3	–	0.8	V
Input High Voltage	$V_{IH}$		2.0	–	$V_{CC}$	V
Output Low Voltage	$V_{OL}$	$I_{OL} = 2\text{mA}$	–	–	0.4	V
Output High Voltage	$V_{OH}$	$I_{OH} = -250\mu\text{A}$	2.4	–	–	V
Power Supply Current	$I_{CC}$	$T_C = 250\text{ns}$	–	–	120	mA
Input Leakage Current	$I_{L1}$	$V_{IN} = 0$ to $V_{CC}$	–	–	10	$\mu\text{A}$
Tri-State Output Leakage Current in Float	$I_{LOH}$	$V_{OUT} = 2.4$ to $V_{CC}$	–	–	10	$\mu\text{A}$
Tri-State Output Leakage Current in Float	$I_{LOL}$	$V_{OUT} = 0.4\text{V}$	–	–	–10	$\mu\text{A}$
Darlington Drive Current	$I_{OHD}$	$V_{OH} = 1.5\text{V}$ , $R_{EXT} = 390\Omega$	–1.5	–	–	mA

**Capacitance:** ( $T_A = +25^\circ\text{C}$ ,  $f = 1\text{MHz}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Capacitance	$C_\phi$	Unmeasured Pins Returned to GND	–	–	20	pF
Input Capacitance	$C_{IN}$		–	–	5	pF
Output Capacitance	$C_{OUT}$		–	–	10	pF

**AC Characteristics:** ( $T_A = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Cycle Time	$T_{cC}$		400	–	Note 2	ns
Clock Width (High)	$T_{wCH}$		170	–	2000	ns
Clock Width (Low)	$T_{wCL}$		170	–	2000	ns
Clock Fall Time	$T_{fC}$		–	–	30	ns
Clock Rise Time	$T_{rC}$		–	–	30	ns
All Hold Times	$T_h$		0	–	–	ns
CS to Clock $\uparrow$ Setup Time	$T_{sCS}(C)$		250	–	–	ns
$\overline{CE}$ to Clock $\uparrow$ Setup Time	$T_{sCE}(C)$		200	–	–	ns
$\overline{IORQ}$ $\downarrow$ to Clock $\uparrow$ Setup Time	$T_{sIO}(C)$		250	–	–	ns
$\overline{RD}$ to Clock $\uparrow$ Setup Time	$T_{sRD}(C)$		240	–	–	ns

Note 2.  $T_{cC} = T_{wCH} + T_{wCL} + T_{cC} + T_{rC}$ .

**AC Characteristics (Cont'd):** ( $T_A = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock $\downarrow$ to Data Out Delay	$T_{dC}(\text{DO})$	Note 3	–	–	240	ns
Clock $\uparrow$ to Data Out Float Delay	$T_{dC}(\text{DOz})$		–	–	230	ns
Data In to Clock $\uparrow$ Setup Time	$T_{sDI}(\text{C})$		60	–		ns
$\overline{\text{M1}}$ to Clock $\uparrow$ Setup Time (INTA or M1 Cycle)	$T_{sM1}(\text{C})$		210	–	–	ns
$\overline{\text{M1}}$ $\downarrow$ to IEO $\downarrow$ Delay (Interrupt Immediately Preceding M1)	$T_{dM1}(\text{IEO})$	Note 4, Note 5	–	–	300	ns
$\overline{\text{IORQ}}$ $\downarrow$ to Data Out Delay (INTA Cycle)	$T_{dIO}(\text{DOT})$	Note 3	–	–	340	ns
IEI $\downarrow$ to IEO $\downarrow$ Delay	$T_{dIEI}(\text{IEOf})$	Note 4	–	–	190	ns
IEI $\uparrow$ to IEO $\uparrow$ Delay (After ED Decode)	$T_{dIEI}(\text{IEOr})$	Note 4	–	–	220	ns
Clock $\uparrow$ to $\overline{\text{INT}}$ $\downarrow$ Delay	$T_{dC}(\text{INT})$	Timer Mode	–	–	$T_{cT} + 220$	ns
CLR/TRG $\uparrow$ to $\overline{\text{INT}}$ $\downarrow$ ( $T_{sCTR}(\text{C})$ Satisfied)	$T_{dCTK}(\text{INT})$	Counter Mode	–	–	$T_{cC} + 230$	ns
CLR/TRG $\uparrow$ to $\overline{\text{INT}}$ $\downarrow$ ( $T_{sCTR}(\text{C})$ Not Satisfied)			–	–	$2T_{cC} + 530$	ns
CLK Cycle Time	$T_{cCTR}$	Counter Mode	$2T_{cC}$	–	–	ns
CLK/TRG Rise Time	$T_{rCTR}$		–	–	50	ns
CLK/TRG Fall Time	$T_{fCTR}$		–	–	50	ns
CLK/TRG Width (Low)	$T_{wCTRL}$		200	–	–	ns
CLK/TRG Width (High)	$T_{wCTRH}$		200	–	–	ns
CLK $\uparrow$ to Clock $\uparrow$ Setup Time for Immediate Count	$T_{sCTR}(\text{Cc})$	Counter Mode	300	–	–	ns
TRG $\uparrow$ to Clock $\uparrow$ Setup Time for Enabling of Prescaler on Following Clock $\uparrow$	$T_{sCTR}(\text{Ct})$	Timer Mode	210	–	–	ns
Clock $\uparrow$ to ZC/TO $\uparrow$ Delay	$T_{dC}(\text{ZCTOr})$		260	–	–	ns
Clock $\downarrow$ to ZC/TO $\downarrow$ Delay			190	–	–	ns

Note 3. Increase delay by 10ns for each 50pF increase in loading, 200pF maximum for data lines and 100pF for control lines.

Note 4. Increase delay by 10ns for each 10pF increase in loading, 100pF maximum.

Note 5.  $2.5 T_{cC} > (N-2) T_{dIEI}(\text{IEOF}) + T_{dIM1}(\text{IEO}) + T_{sIEI}(\text{IO})$ .

Note 6.  $\overline{\text{RESET}}$  must be active for a minimum of 3 clock cycles.



