1 28M-bit (×16/×32) Dual-Operation Flash Memory with Page Mode
MBM29PDL1280F

This flash memory can simultaneously read/program/erase data with a single 3V power supply. It possesses fast access performance with an initial access time of 70ns/80ns and a page access time of 25ns/30ns under low voltage.

Product Overview

As an industry first, FUJITSU has developed a 128M-bit dual-operation page mode flash memory with 32-bit data transfer width for use in applications such as mobile phones, laser printers, and car navigation systems.

Remarkably, the faster speed is needed and the functionality and density of electronic devices have been increased, as seen in the new generation of faster/larger-density mobile phones, faster laser printers, and improved map-searching and communicative functions in car navigation. Speedup in the microprocessors mounted in these devices is inevitable, and their data transfer width is shifting from a conventional ×8/×16-bit to ×16/×32-bit or even 64-bit. At the same time, speedup, enlarged data transfer width, and larger density are also demanded in the flash memory for these devices.

This product was developed with the focus on fast access speed, and achieves a high-speed loading of 25ns-the fastest page mode access currently available. Furthermore, by enlarging the data transfer width from a conventional ×8/×16-bit to ×16/×32-bit, the consistency of the microprocessor at system is improved and huge amounts of data can be transacted at one time and at high speed. Using a dual-operation memory capable of simultaneously reading/programming/erasing data, the apparent memory operation time can also be shortened. This device also has a Hi-ROM function to prevent large-scale illegal copying, write hardware protection for the boot block
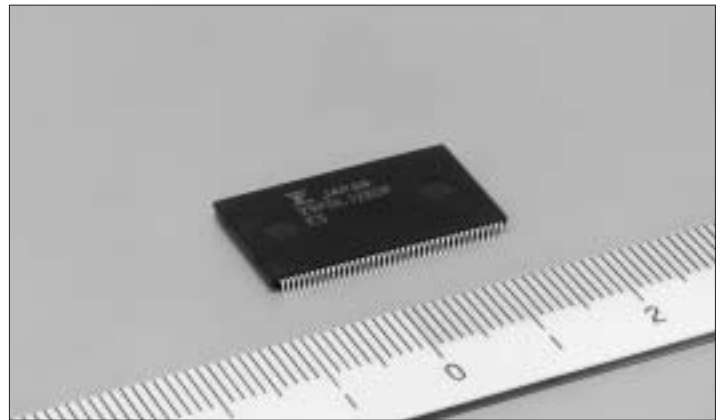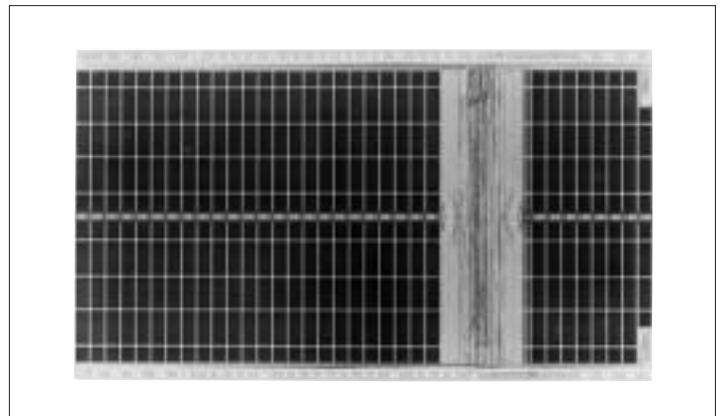
Photo 1 External View

Photo 2 Chip

that stores the system program, and an acceleration function that enables high-speed programming at system.

Product Features

■ High-Speed Read Operation
Fig.1 shows the page read mode.

The page mode reads an optional page (8 words or 4 double-words) initially by selecting high-order addresses (A21 to A2). Then, data within the page can be read at high speed in single- or double-words unit by selecting low-order addresses (A1 to A-1, or A1 to A0).

This product is available with initial access time of 70ns or 80ns, with corresponding page access time of 25ns or 30ns,

respectively.

Fig.2 shows the power supply voltage dependency of the access time, and **Fig.3** shows the power supply voltage dependency of the page read access time.

■ Dual-Operation Function
The address space is divided into 4 regions called "Bank" (Bank A, B, C and D). For example, data can be read from a sector in the bank B, C or D while programming/erasing data on a sector in Bank A.

■ Single 3V Power Supply Operation
Data can be read/programmed/erased with a single 3V power supply. Since no 12V power supply is needed, the system can be configured without using a voltage converter or
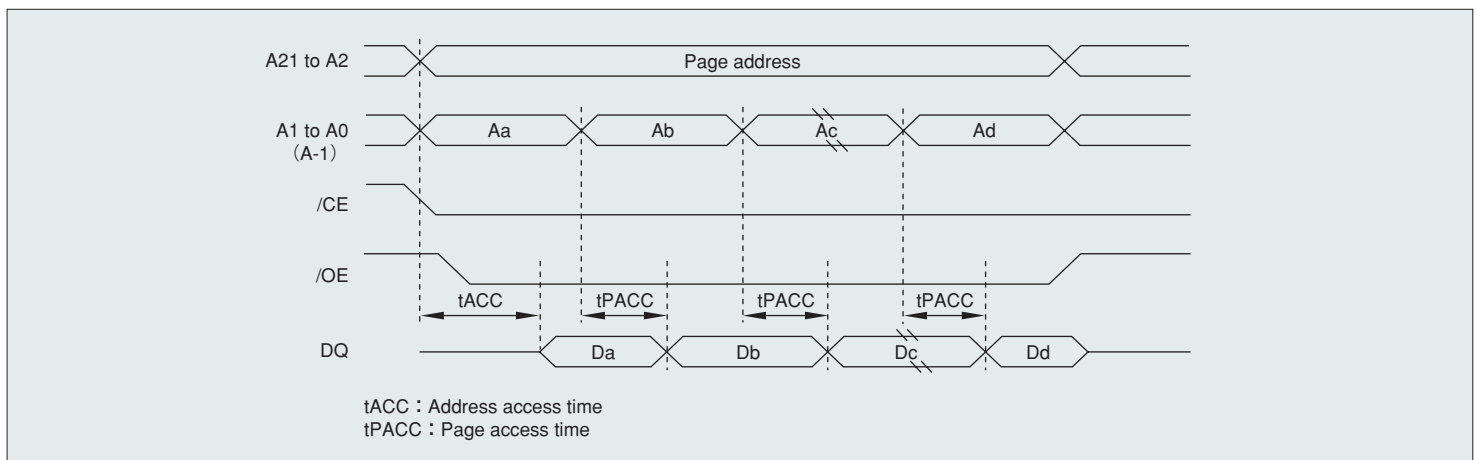
Figure 1 Page Read Mode

tACC : Address access time
tPACC : Page access time

Figure 2 Power Supply Voltage Dependency of Access Time

Figure 3 Power Supply Voltage Dependency of Page Read Access Time

other additional parts.

■ Compatibility with Conventional Products

The command of program/erase is the same sequence as that of the single 3V power supply flash memory already commercialized.

■ ×16-bit or ×32-bit Configuration

When the DW/$\overline{\text{W}}$ pin is set to "H" the device operates in double-words mode to read/program data through DQ31-DQ0. When the DW/$\overline{\text{W}}$ pin is set to "L", the device operates in word mode. In this mode, DQ31/A-1 will be the lowest address bit and data is read/programmed through DQ0-DQ15, with DQ16-DQ30 being ignored.

Fig.4 and **5** show the pin assignment.

■ Hi-ROM Function

In addition to the normal memory region, a special 256bytes region is offered as an area where data can be programmed only once. Programming special data (for example, unique ID number) provides a highly advanced security function by the combination with an application.

■ Write Protection Function

This function is easily realized by the hardware method.

Write Protection Function provides the protection of the 2 outmost 8Kbytes sector on both end of boot sectors by setting the $\overline{\text{WP}}$ pin to "L", regardless of whether normal sector protection is used.

■ Acceleration Function

This function is effective when a large amount of flash memory embedded into the system are programmed at shipment. When a high voltage (VHH) is applied to the ACC pin, the device enters the Acceleration mode, which enables faster programming than the normal mode. With this function, the programming time can be shortened 60% as much as that of the normal mode.

Table 1 shows the product line up.

Advantages and Effects

No External ROM/RAM Required

Since this product offers a dual-operation function, erase/program on itself is possible while executing a program for reprogramming directly from itself without loading in other memories. Therefore, the cost, mounting area, and power consumption of the system can be drastically reduced.

Figure 4 Pin Assignment (FBGA-96)

（TOP VIEW）

| A11 N.C. | B11 N.C. | C11 N.C. | | | | | | | | | | P11 N.C. | Q11 N.C. | R11 N.C. |

| | | | E10 DQ30 | F10 Vcc/Vccq | G10 DQ13 | H10 DQ12 | J10 DQ27 | K10 DQ26 | L10 Vcc/Vccq | M10 DQ9 | | |

| D9 $\overline{\text{CE}}$ | E9 VSS | F9 DQ15 | G9 DQ29 | H9 DQ28 | J9 DQ11 | K9 VSS | L9 DQ24 | M9 VCC | N9 A19 |

| D8 A20 | E8 DW/$\overline{\text{W}}$ | F8 $\overline{\text{OE}}$ | G8 DQ14 | H8 VSS | J8 DQ10 | K8 DQ25 | L8 A18 | M8 A17 | N8 A16 |

| D7 $\overline{\text{WE}}$ | E7 N.C. | F7 A21 | G7 DQ31/A-1 | H7 N.C. | J7 N.C. | K7 DQ8 | L7 A15 | M7 A14 | N7 A13 |

| D6 $\overline{\text{RESET}}$ | E6 ACC | F6 $\overline{\text{WP}}$ | G6 RY/$\overline{\text{BY}}$ | H6 N.C. | J6 N.C. | K6 N.C. | L6 N.C. | M6 N.C. | N6 N.C. |

| D5 A1 | E5 A2 | F5 A3 | G5 A0 | H5 DQ2 | J5 N.C. | K5 A12 | L5 A11 | M5 A9 | N5 A10 |

| D4 A4 | E4 A5 | F4 DQ0 | G4 DQ16 | H4 DQ18 | J4 DQ5 | K4 DQ21 | L4 A8 | M4 A6 | N4 A7 |

| | E3 VCC | F3 DQ1 | G3 Vss | H3 DQ19 | J3 DQ4 | K3 DQ6 | L3 DQ7 | M3 DQ23 | N3 VSS |

| | | F2 DQ17 | G2 Vcc/Vccq | H2 DQ3 | J2 DQ20 | K2 Vss | L2 Vcc/Vccq | M2 DQ22 | |

| A1 N.C. | B1 N.C. | C1 N.C. | | | | | | | | | | P1 N.C. | Q1 N.C. | R1 N.C. |

Effective Use of Programming Time and Erasing Time

When addresses are changed to those of other Bank while erase/program in one sector, the system can be read the stored data at the address without canceling the erase/program operation. Changing the addresses of a Bank to those of other releases the data bus from the status information and enables it to output the data stored in the memory. Therefore, the apparent programming/erasing time can be reduced to almost 0 by the smart design of software, which improves the process speed of the products mounted the dual-operation flash memory.

Purpose

The followings are sample applications for 128M-bit dual-operation page mode flash memory with the above characteristics.
- A system requiring a large-density flash memory due to high functionality or complex functions
- High-performance, external memory for a high-performance ×32/×64-bit micro-controller
- A system in which program/code is upgraded

Future Development

This article introduced a new product, MBM29PDL1280F, to meet the new demands for high speed and high functionality mainly in mobile phones, laser printers, and car navigation devices.

To meet customer's demands, FUJITSU will provide its lineup of families which realize multi-functionality, high functionality and larger density. ✳
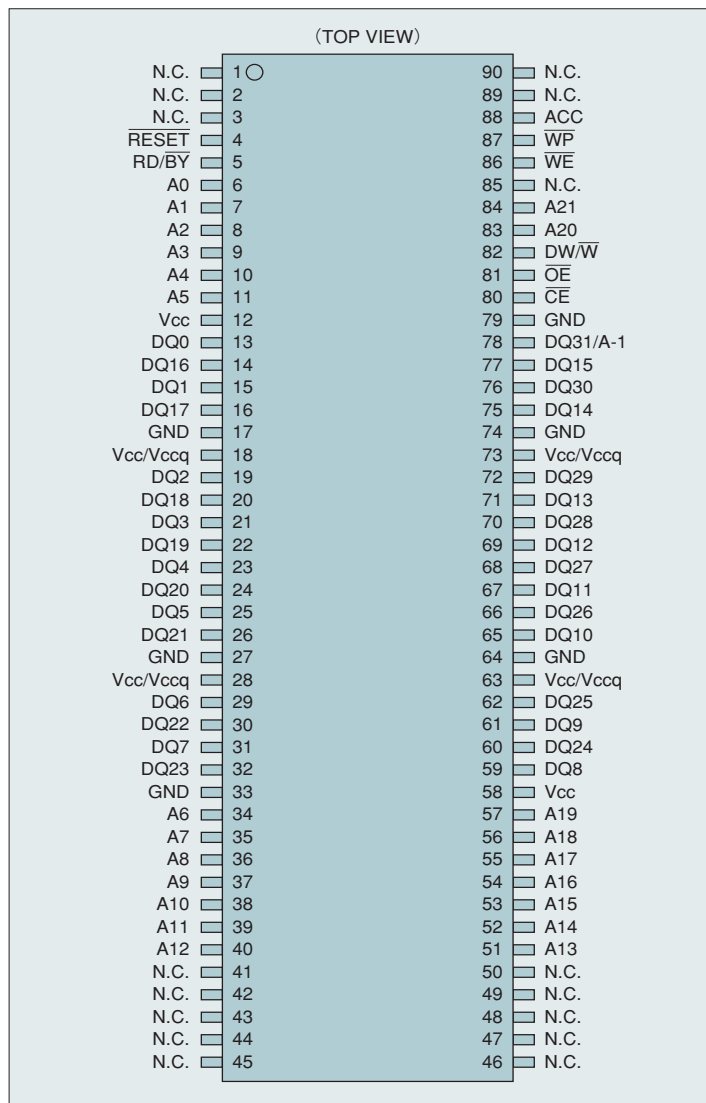
Figure 5 Pin Assignment (SSOP-90)

（TOP VIEW）

Left	Pin		Pin	Right
N.C.	1		90	N.C.
N.C.	2		89	N.C.
N.C.	3		88	ACC
$\overline{RESET}$	4		87	$\overline{WP}$
RD/$\overline{BY}$	5		86	$\overline{WE}$
A0	6		85	N.C.
A1	7		84	A21
A2	8		83	A20
A3	9		82	DW/$\overline{W}$
A4	10		81	$\overline{OE}$
A5	11		80	$\overline{CE}$
Vcc	12		79	GND
DQ0	13		78	DQ31/A-1
DQ16	14		77	DQ15
DQ1	15		76	DQ30
DQ17	16		75	DQ14
GND	17		74	GND
Vcc/Vccq	18		73	Vcc/Vccq
DQ2	19		72	DQ29
DQ18	20		71	DQ13
DQ3	21		70	DQ28
DQ19	22		69	DQ12
DQ4	23		68	DQ27
DQ20	24		67	DQ11
DQ5	25		66	DQ26
DQ21	26		65	DQ10
GND	27		64	GND
Vcc/Vccq	28		63	Vcc/Vccq
DQ6	29		62	DQ25
DQ22	30		61	DQ9
DQ7	31		60	DQ24
DQ23	32		59	DQ8
GND	33		58	Vcc
A6	34		57	A19
A7	35		56	A18
A8	36		55	A17
A9	37		54	A16
A10	38		53	A15
A11	39		52	A14
A12	40		51	A13
N.C.	41		50	N.C.
N.C.	42		49	N.C.
N.C.	43		48	N.C.
N.C.	44		47	N.C.
N.C.	45		46	N.C.

Table 1 Product Line Up

Part number			MBM29PDL1280F	
Speed option			70	80
Bank architecture			4-bank architecture Bank A: 16Mb, Bank B: 48Mb Bank C: 48Mb, Bank D: 16Mb	
Access time	Initial		70ns	80ns
	Page		25ns	30ns
Power supply voltage			2.7V to 3.6V	
Power consumption (Max.)	Read	Word	252mW	
	Erase/program in progress		126mW	
	CMOS standby		18 μW	
Erase time (Typ.)[1]			0.2s/sector	
Programming time (Typ.)[2]	Word		6 μs	
	Double Word		12 μs	
Package			SSOP-90，FBGA-96	

[1]：Ta＝25℃，Vcc＝2.9V　[2]：Ta＝25℃，Vcc＝2.9V　programming data is checker.