

## HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

### FEATURES

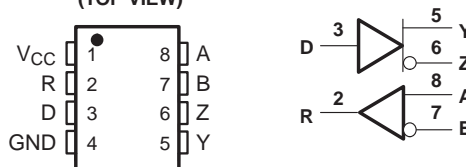
- Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995 Standard
- Full-Duplex Signaling Rates up to 100 Mbps (See Table 1)
- Bus-Terminal ESD Exceeds 12 kV
- Operates From a Single 3.3-V Supply
- Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV and a 100-Ω Load
- Propagation Delay Times
  - Driver: 1.7 ns Typ
  - Receiver: 3.7 ns Typ
- Power Dissipation at 200 MHz
  - Driver: 25 mW Typical
  - Receiver: 60 mW Typical
- LVTTTL Input Levels Are 5-V Tolerant
- Receiver Maintains High Input Impedance With  $V_{CC} < 1.5\text{ V}$
- Receiver Has Open-Circuit Fail Safe

### DESCRIPTION

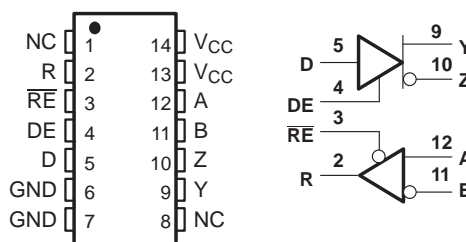
The SN65LVDS179, SN65LVDS180, SN65LVDS050, and SN65LVDS051 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps (see the *Application Information* section). The TIA/EIA-644 standard compliant electrical interface provides a minimum differential output voltage magnitude of 247 mV into a 100-Ω load and receipt of 50-mV signals with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer depends on the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics).

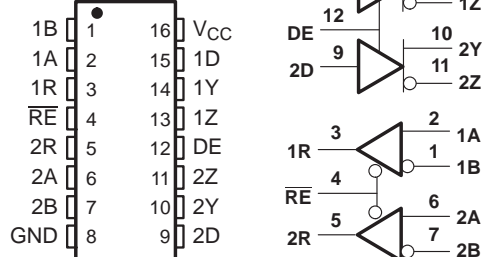
SN65LVDS179D (Marked as DL179 or LVD179)  
SN65LVDS179DGK (Marked as S79)  
(TOP VIEW)



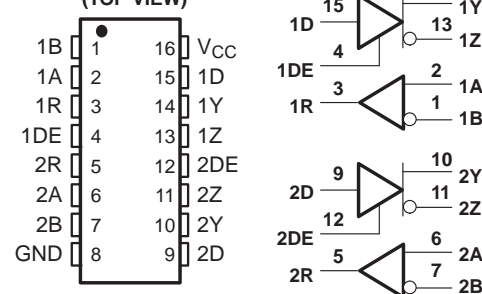
SN65LVDS180D (Marked as LVDS180)  
SN65LVDS180PW (Marked as LVDS180)  
(TOP VIEW)



SN65LVDS050D (Marked as LVDS050)  
SN65LVDS050PW (Marked as LVDS050)  
(TOP VIEW)



SN65LVDS051D (Marked as LVDS051)  
SN65LVDS051PW (Marked as LVDS051)  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

These devices offer various driver, receiver, and enabling combinations in industry-standard footprints. Because these devices are intended for use in simplex or distributed simplex bus structures, the driver enable function does not put the differential outputs into a high-impedance state but rather disconnects the input and reduces the quiescent power used by the device. (For these functions with a high-impedance driver output, see the SN65LVDM series of devices.) All devices are characterized for operation from -40°C to 85°C.

**Table 1. Maximum Recommended Operating Speeds**

Part Number	All Buffers Active	Rx Buffer Only	Tx Buffer Only
SN65LVDS179	150 Mbps	150 Mbps	400 Mbps
SN65LVDS180	150 Mbps	150 Mbps	400 Mbps
SN65LVDS050	100 Mbps	100 Mbps	400 Mbps
SN65LVDS051	100 Mbps	100 Mbps	400 Mbps

### AVAILABLE OPTIONS<sup>(1)</sup>

PACKAGE		
SMALL OUTLINE (D)	SMALL OUTLINE (DGK)	SMALL OUTLINE (PW)
SN65LVDS050D	—	SN65LVDS050PW
SN65LVDS051D	—	SN65LVDS051PW
SN65LVDS179D	SN65LVDS179DGK	—
SN65LVDS180D	—	SN65LVDS180PW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

## FUNCTION TABLES

### SN65LVDS179 RECEIVER

INPUTS	OUTPUT <sup>(1)</sup>
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 50 \text{ mV}$	H
$50 \text{ mV} < V_{ID} < 50 \text{ mV}$	?
$V_{ID} \leq -50 \text{ mV}$	L
Open	H

(1) H = high level, L = low level, ? = indeterminate

### SN65LVDS179 DRIVER<sup>(1)</sup>

INPUT	OUTPUTS	
D	Y	Z
L	L	H
H	H	L
Open	L	H

(1) H = high level, L = low level

**SN65LVDS180, SN65LVDS050, and  
SN65LVDS051 RECEIVER<sup>(1)</sup>**

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 50 \text{ mV}$	L	H
$50 \text{ mV} < V_{ID} < 50 \text{ mV}$	L	?
$V_{ID} \leq -50 \text{ mV}$	L	L
Open	L	H
X	H	Z

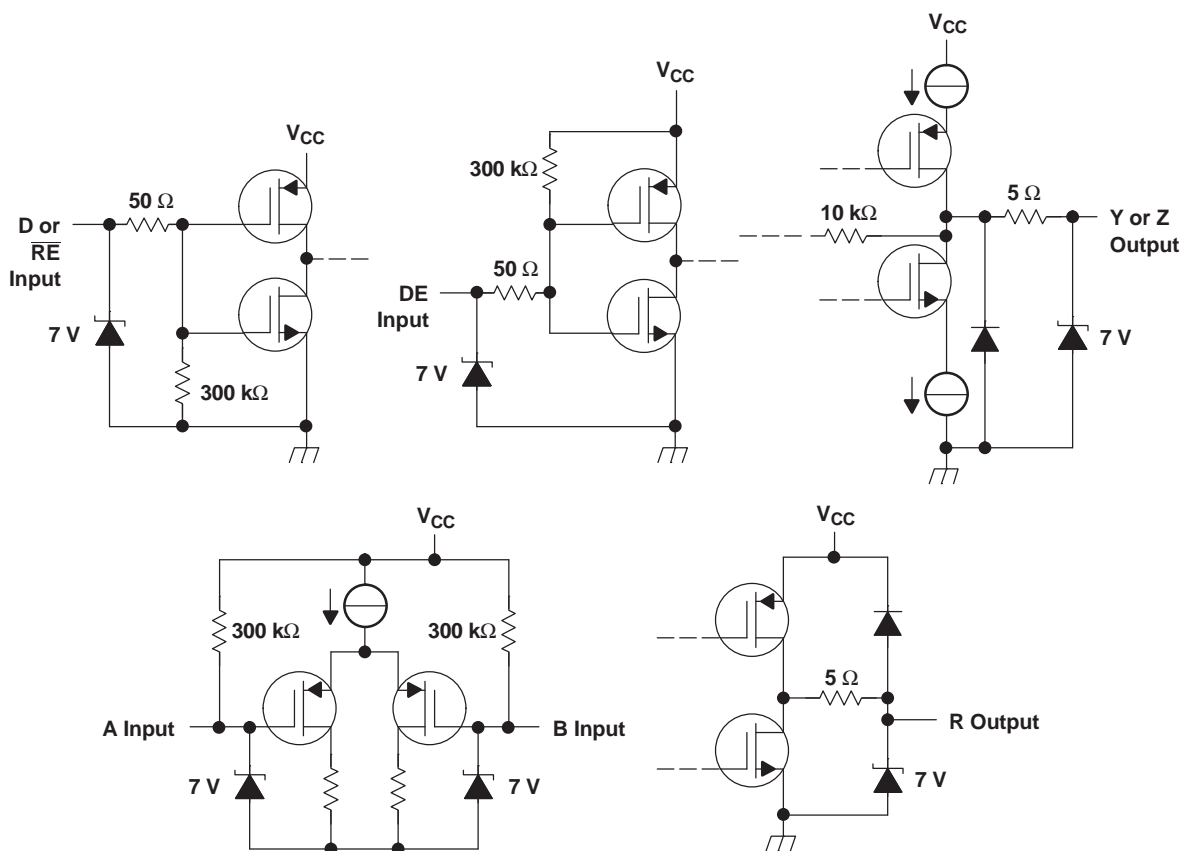
(1) H = high level, L = low level, Z = high impedance, X = don't care, ? = indeterminate

**SN65LVDS180, SN65LVDS050, and  
SN65LVDS051 DRIVER<sup>(1)</sup>**

INPUTS		OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Off	Off

(1) H = high level, L = low level, Z = high impedance, X = don't care, Off = no output

**EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS**



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			UNIT
$V_{CC}$ (see <sup>(2)</sup> )	Supply voltage range		–0.5 V to 4 V
	Voltage range:	D, R, DE, $\overline{RE}$	–0.5 V to 6 V
		Y, Z, A, and B	–0.5 V to 4 V
$ V_{OD} $	Differential output voltage:		1 V
	Electrostatic discharge:	Y, Z, A, B, and GND (see <sup>(3)</sup> )	Class 3, A:12 kV, B:600 V
		All	Class 3, A:7 kV, B:500 V
	Continuous power dissipation		See Dissipation Rating Table
	Storage temperature range		–65°C to 150°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		250°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
- (3) Tested in accordance with MIL-STD-883C Method 3015.7.

## DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ <sup>(1)</sup>	$T_A = 85^\circ\text{C}$ POWER RATING
PW(14)	736 mW	5.9 mW/°C	383 mW
PW(16)	839 mW	6.7 mW/°C	437 mW
D(8)	635 mW	5.1 mW/°C	330 mW/°C
D(14)	987 mW	7.9 mW/°C	513 mW/°C
D(16)	1110 mW	8.9 mW/°C	577 mW/°C
DGK	424 mW	3.4 mW/°C	220 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no airflow.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	3	3.3	3.6	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$ V_{ID} $	Magnitude of differential input voltage	0.1		0.6	V
$ V_{OD}(\text{dis}) $	Magnitude of differential output voltage with disabled driver			520	mV
$V_{OY}$ or $V_{OZ}$	Driver output voltage	0		2.4	V
$V_{IC}$	Common-mode input voltage (see <a href="#">Figure 5</a> )	$\frac{ V_{ID} }{2}$	$2.4 - \frac{ V_{ID} }{2}$	$V_{CC} - 0.8$	V
$T_A$	Operating free-air temperature	–40		85	°C

## DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
I <sub>CC</sub>	Supply current	SN65LVDS179	No receiver load, driver R <sub>L</sub> = 100 Ω		9	12	mA
		SN65LVDS180	Driver and receiver enabled, no receiver load, driver R <sub>L</sub> = 100 Ω		9	12	mA
	Driver enabled, receiver disabled, R <sub>L</sub> = 100 Ω		5	7			
	Driver disabled, receiver enabled, no load		1.5	2			
	Disabled		0.5	1			
	SN65LVDS050	Drivers and receivers enabled, no receiver loads, driver R <sub>L</sub> = 100 Ω		12	20	mA	
		Drivers enabled, receivers disabled, R <sub>L</sub> = 100 Ω		10	16		
		Drivers disabled, receivers enabled, no loads		3	6		
		Disabled		0.5	1		
	SN65LVDS051	Drivers enabled, No receiver loads, driver R <sub>L</sub> = 100 Ω		12	20	mA	
		Drivers disabled, no loads		3	6		

(1) All typical values are at 25°C and with a 3.3-V supply.

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OD} $	Differential output voltage magnitude	$R_L = 100\ \Omega$ , See <a href="#">Figure 3</a> and <a href="#">Figure 2</a>	247	340	454	mV
$\Delta V_{OD} $	Change in differential output voltage magnitude between logic states		-50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See <a href="#">Figure 3</a>	1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
$I_{IH}$	High-level input current	DE	$V_{IH} = 5\ V$	-0.5	-20	$\mu A$
		D		2	20	
$I_{IL}$	Low-level input current	DE	$V_{IL} = 0.8\ V$	-0.5	-10	$\mu A$
		D		2	10	
$I_{OS}$	Short-circuit output current	$V_{OY}$ or $V_{OZ} = 0\ V$		3	10	mA
		$V_{OD} = 0\ V$		3	10	
$I_{O(OFF)}$	Off-state output current	DE = OV $V_{OY} = V_{OZ} = OV$	-1		1	$\mu A$
		DE = $V_{CC}$ $V_{OY} = V_{OZ} = OV$ , $V_{CC} < 1.5\ V$				
$C_{IN}$	Input capacitance			3		pF

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IT+</sub> Positive-going differential input voltage threshold	See Figure 5 and Table 2			50	mV
V <sub>IT-</sub> Negative-going differential input voltage threshold		-50			
V <sub>OH</sub> High-level output voltage	I <sub>OH</sub> = -8 mA	2.4			V
	I <sub>OH</sub> = -4 mA	2.8			
V <sub>OL</sub> Low-level output voltage	I <sub>OL</sub> = 8 mA			0.4	V
I <sub>I</sub> Input current (A or B inputs)	V <sub>I</sub> = 0	-2	-11	-20	μA
	V <sub>I</sub> = 2.4 V	-1.2	-3		
I <sub>I(OFF)</sub> Power-off input current (A or B inputs)	V <sub>CC</sub> = 0			±20	μA
I <sub>IH</sub> High-level input current (enables)	V <sub>IH</sub> = 5 V			±10	μA
I <sub>IL</sub> Low-level input current (enables)	V <sub>IL</sub> = 0.8 V			±10	μA
I <sub>OZ</sub> High-impedance output current	V <sub>O</sub> = 0 or 5 V			±10	μA
C <sub>I</sub> Input capacitance			5		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 10 pF, See Figure 2		1.7	2.7	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output			1.7	2.7	ns
t <sub>r</sub> Differential output signal rise time			0.8	1	ns
t <sub>f</sub> Differential output signal fall time			0.8	1	ns
t <sub>sk(p)</sub> Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  ) <sup>(2)</sup>			300		ps
t <sub>sk(o)</sub> Channel-to-channel output skew <sup>(3)</sup>			150		ps
t <sub>en</sub> Enable time	See Figure 4		4.3	10	ns
t <sub>dis</sub> Disable time			3.1	10	ns

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) t<sub>sk(p)</sub> is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

(3) t<sub>sk(o)</sub> is the magnitude of the time difference between the outputs of a single device with all of their inputs connected together.

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

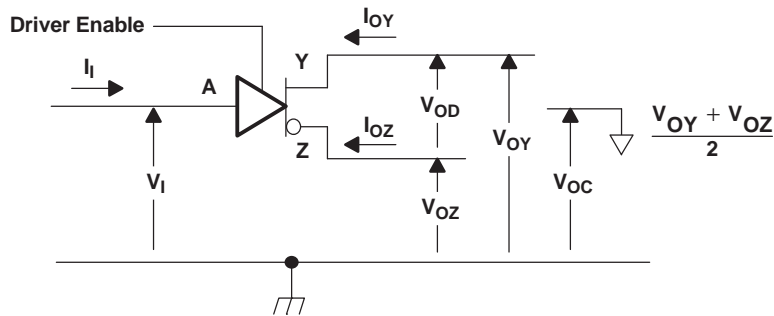
PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	C <sub>L</sub> = 10 pF, See Figure 6		3.7	4.5	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output			3.7	4.5	ns
t <sub>sk(p)</sub> Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  ) <sup>(2)</sup>			0.3		ns
t <sub>r</sub> Output signal rise time			0.7	1.5	ns
t <sub>f</sub> Output signal fall time			0.9	1.5	ns
t <sub>PZH</sub> Propagation delay time, high-impedance-to-high-level output	See Figure 7		2.5		ns
t <sub>PZL</sub> Propagation delay time, high-impedance-to-low-level output			2.5		ns
t <sub>PHZ</sub> Propagation delay time, high-level-to-high-impedance output			7		ns
t <sub>PLZ</sub> Propagation delay time, low-level-to-high-impedance output			4		ns

(1) All typical values are at 25°C and with a 3.3-V supply.

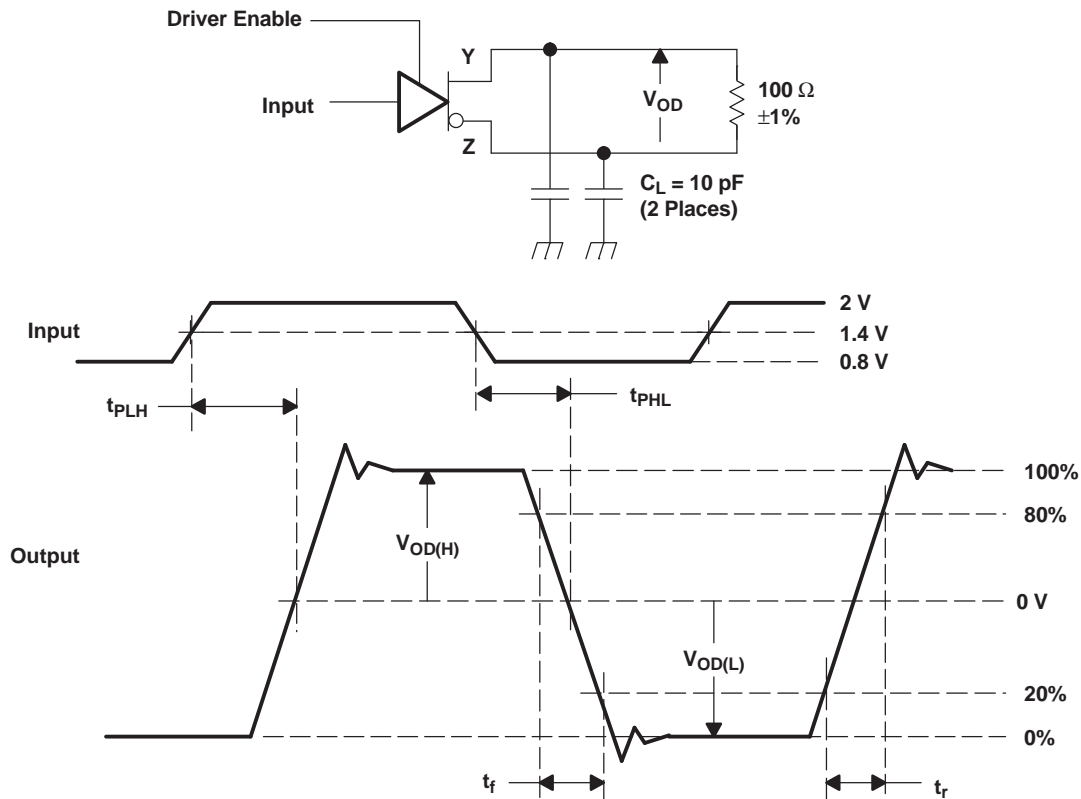
(2) t<sub>sk(p)</sub> is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

## PARAMETER MEASUREMENT INFORMATION

### DRIVER



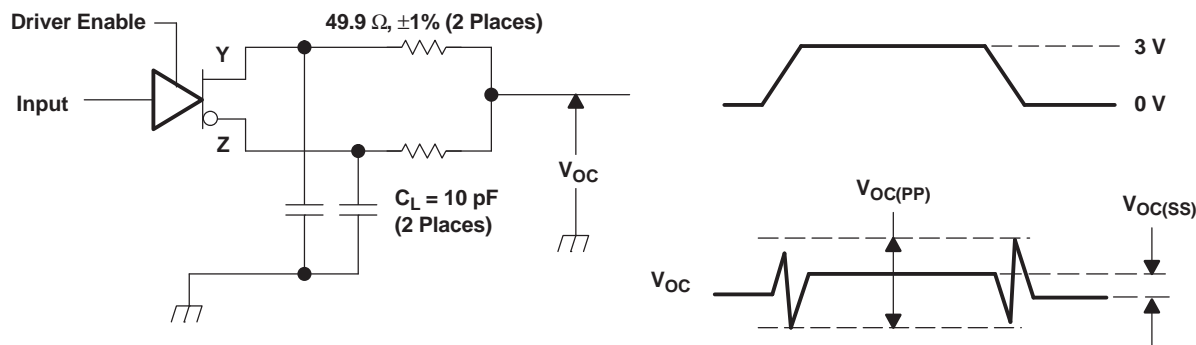
**Figure 1. Driver Voltage and Current Definitions**



- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse repetition rate (PRR) = 50 Mpps, pulse width =  $10 \pm 0.2$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

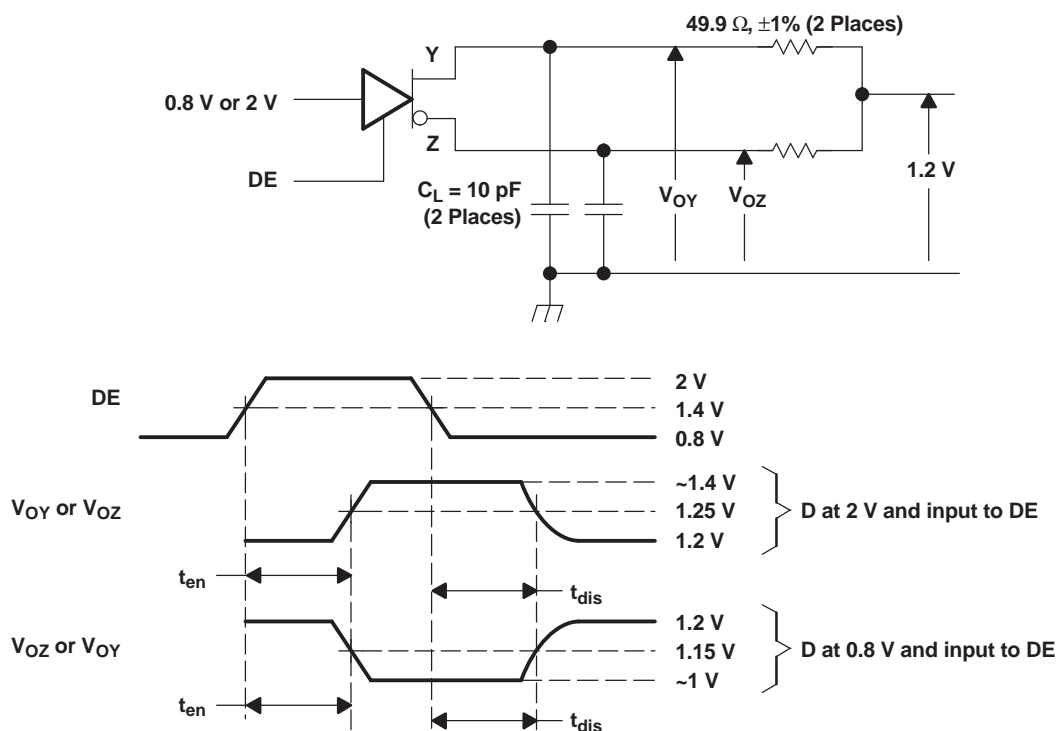
**Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal**

## PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse repetition rate (PRR) = 50 Mpps, pulse width =  $10 \pm 0.2$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T. The measurement of  $V_{OC(PP)}$  is made on test equipment with a -3-dB bandwidth of at least 300 MHz.

**Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage**



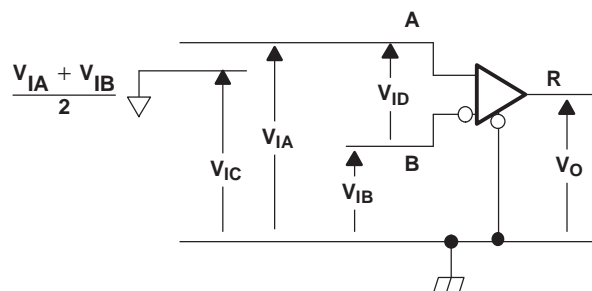
- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width =  $500 \pm 10$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T.

**Figure 4. Enable and Disable Time Circuit and Definitions**



## PARAMETER MEASUREMENT INFORMATION (continued)

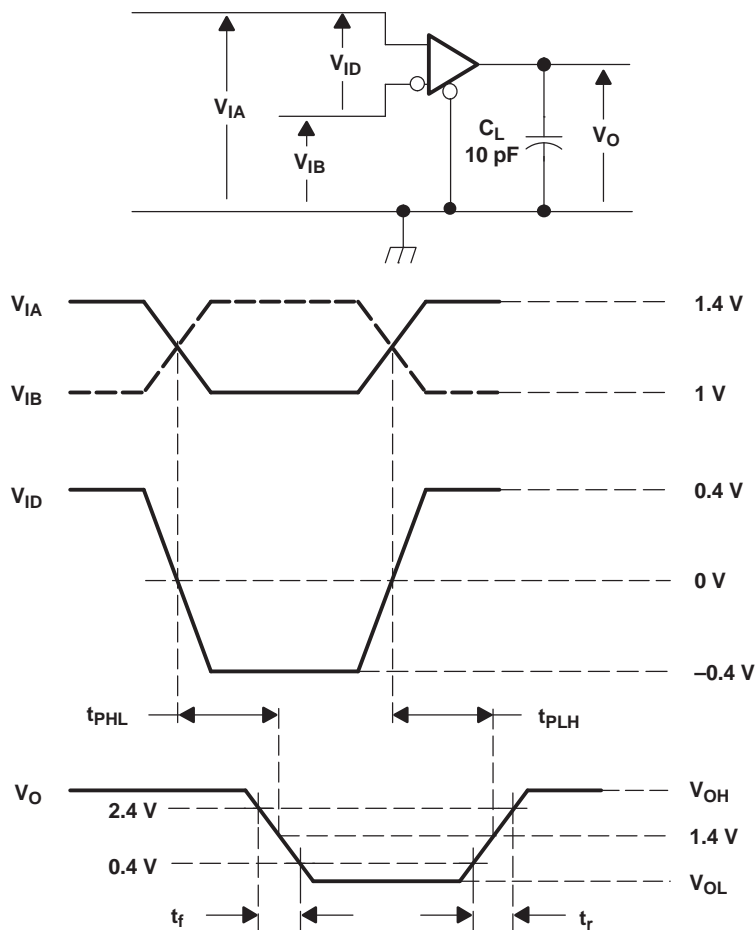
### RECEIVER



**Figure 5. Receiver Voltage Definitions**

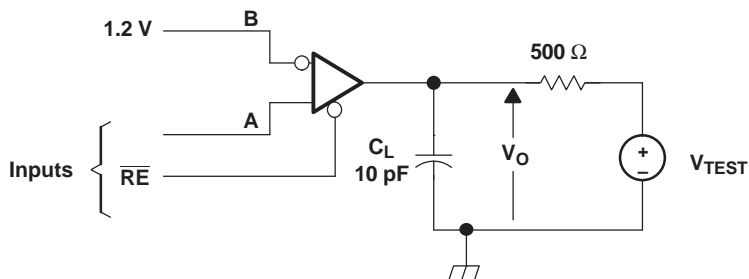
**Table 2. Receiver Minimum and Maximum Input Threshold Test Voltages**

APPLIED VOLTAGES (V)		RESULTING DIFFERENTIAL INPUT VOLTAGE (mV)	RESULTING COMMON-MODE INPUT VOLTAGE (V)
$V_{IA}$	$V_{IB}$	$V_{ID}$	$V_{IC}$
1.25	1.15	100	1.2
1.15	1.25	–100	1.2
2.4	2.3	100	2.35
2.3	2.4	–100	2.35
0.1	0	100	0.05
0	0.1	–100	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3

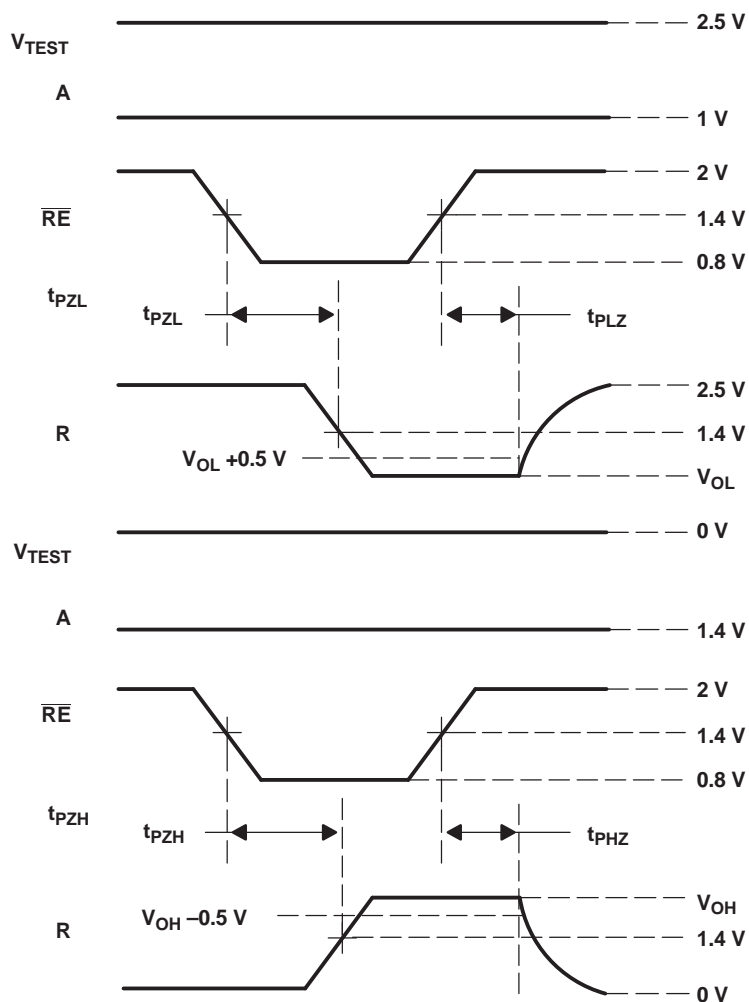


- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1 \text{ ns}$ , pulse repetition rate (PRR) = 50 Mpps, pulse width =  $10 \pm 0.2 \text{ ns}$ .  $C_L$  includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

**Figure 6. Timing Test Circuit and Waveforms**



- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width =  $500 \pm 10$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.



**Figure 7. Enable/Disable Time Test Circuit and Waveforms**

**TYPICAL CHARACTERISTICS**

**DISABLED DRIVER OUTPUT CURRENT**

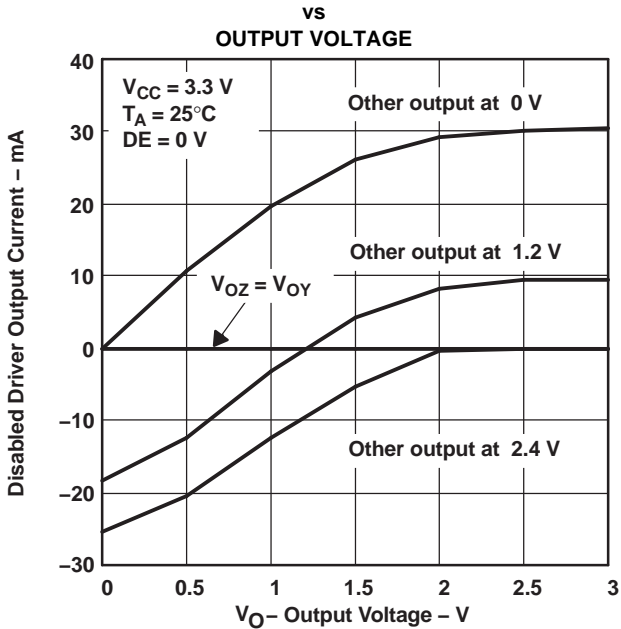


Figure 8.

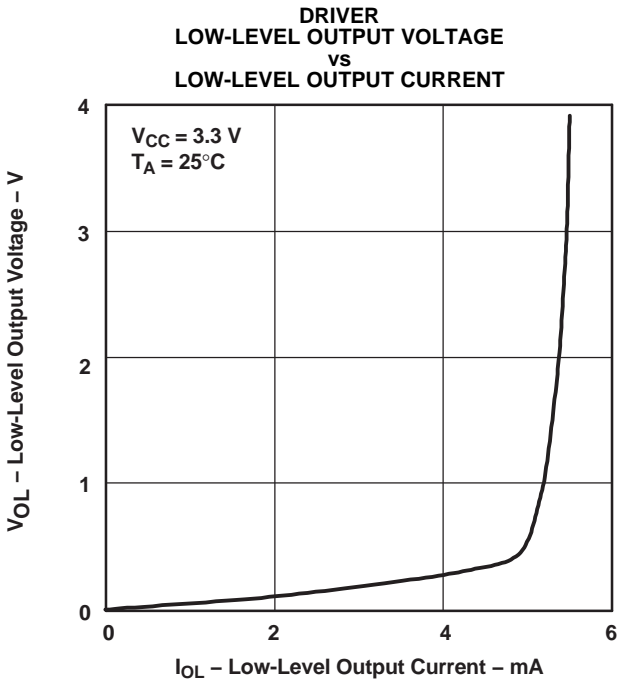


Figure 9.

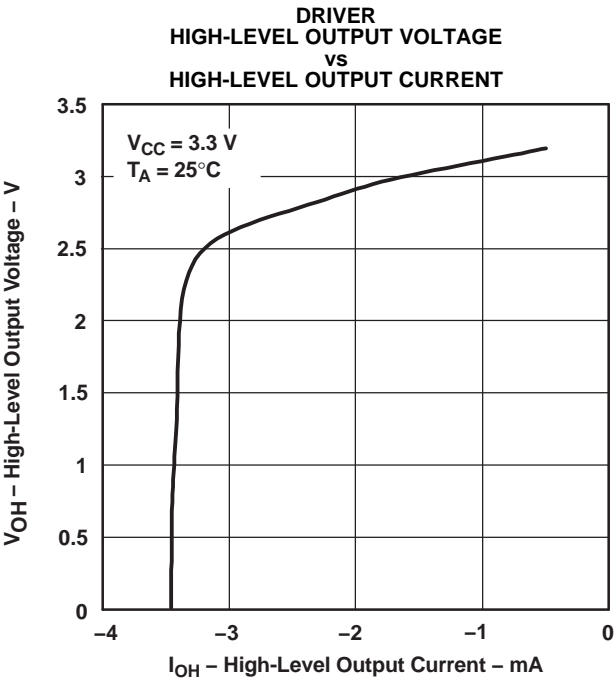


Figure 10.

## TYPICAL CHARACTERISTICS (continued)

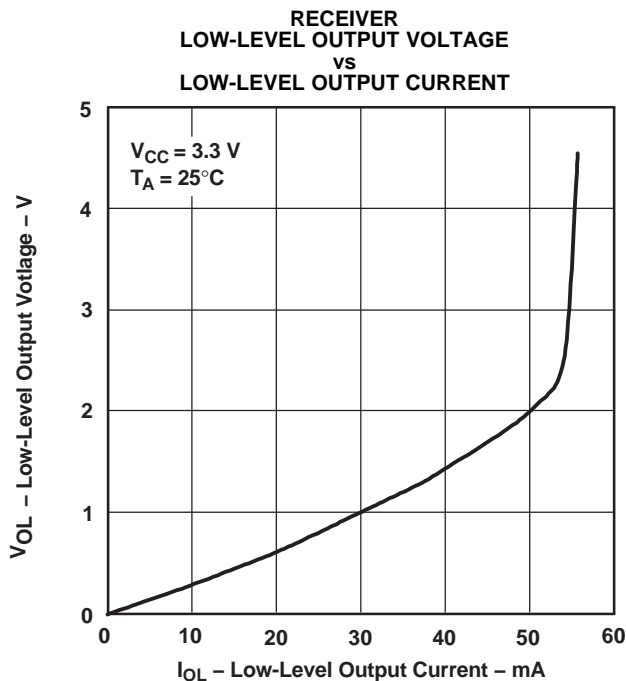


Figure 11.

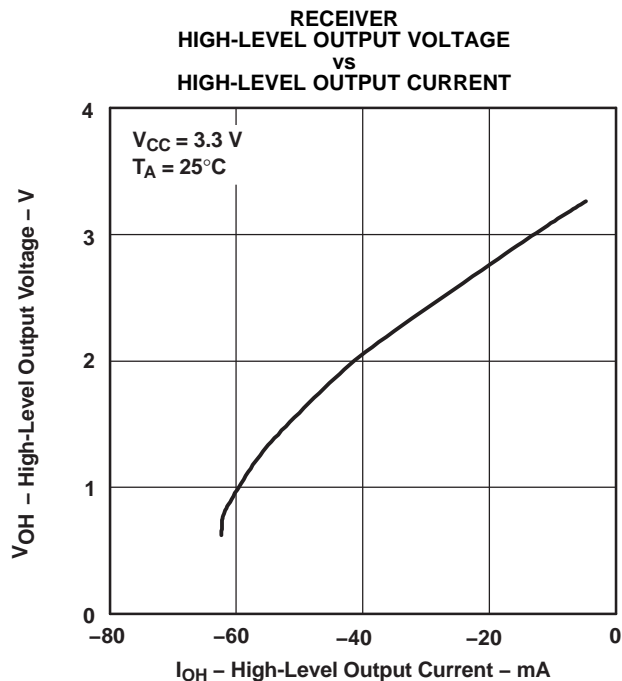


Figure 12.

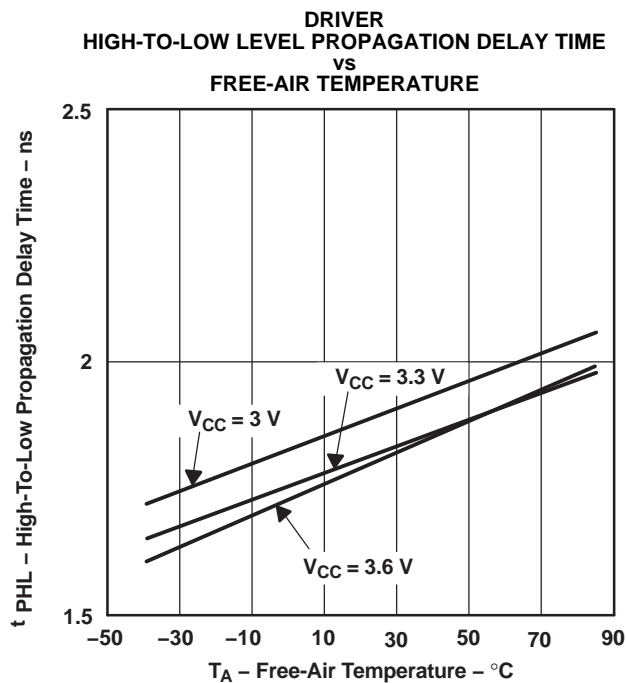


Figure 13.

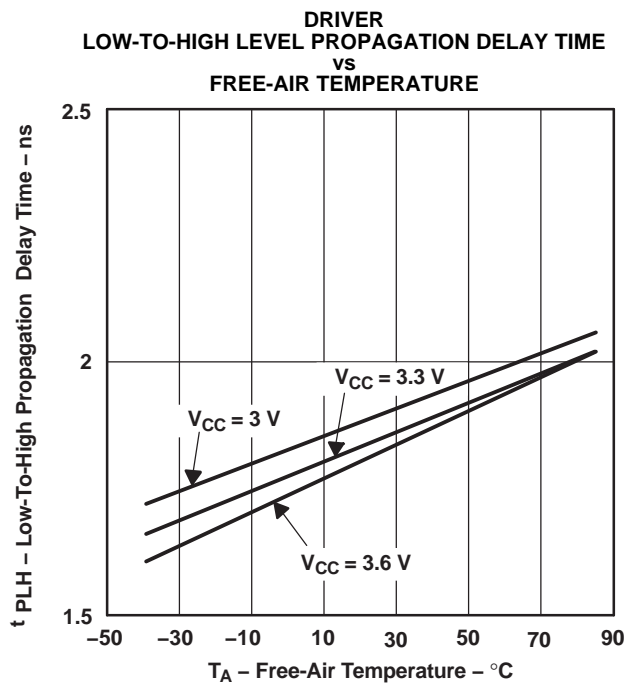


Figure 14.

## TYPICAL CHARACTERISTICS (continued)

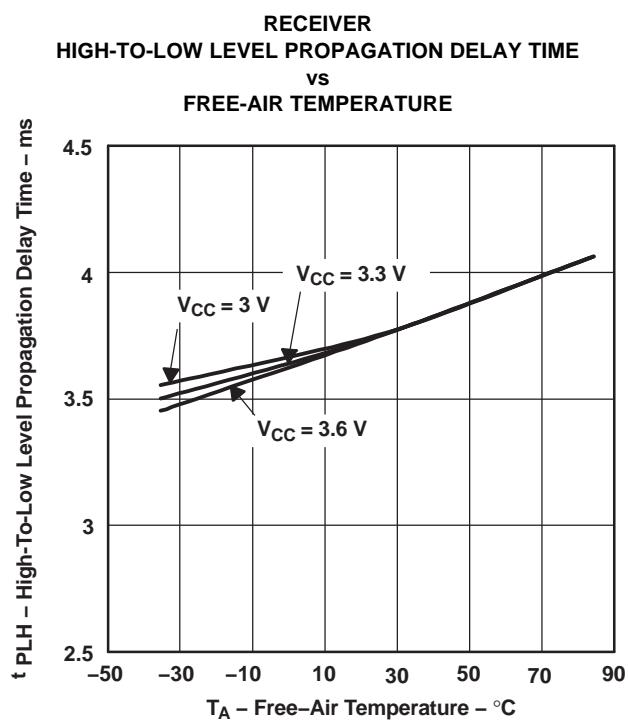


Figure 15.

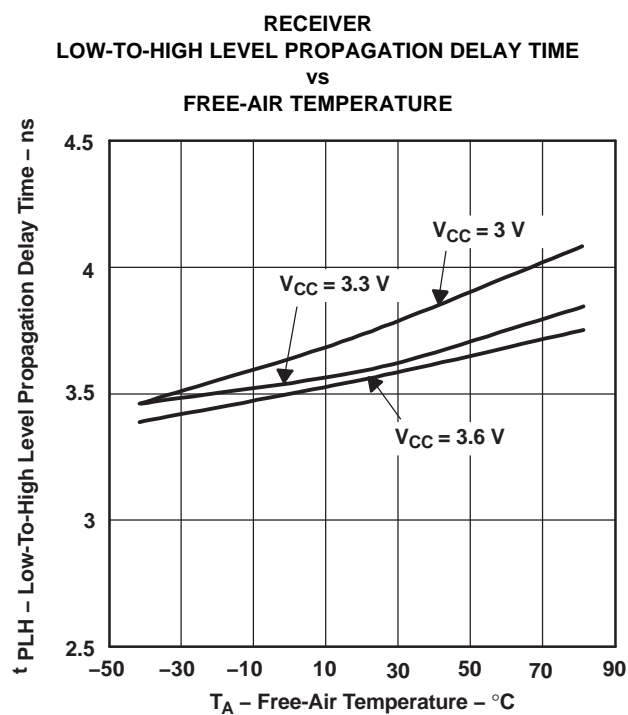
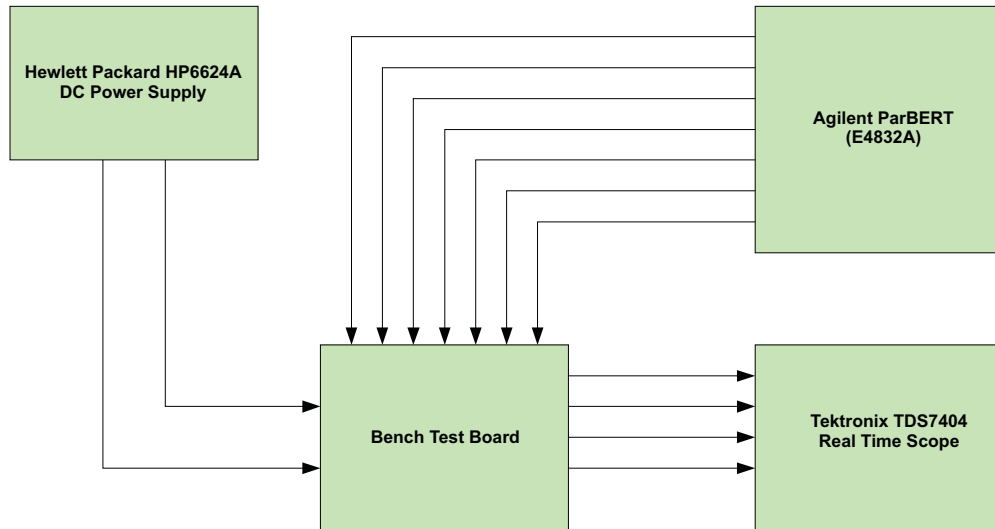


Figure 16.

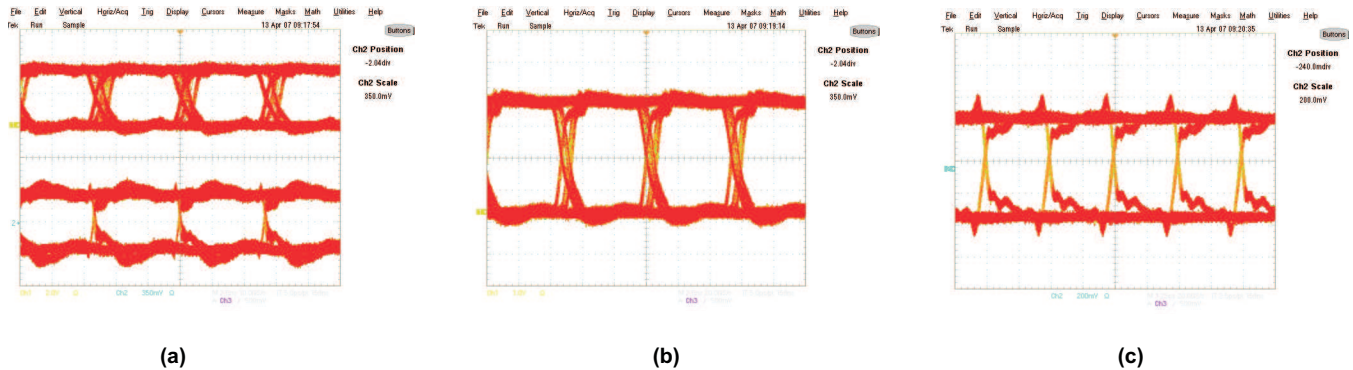
## APPLICATION INFORMATION

### Equipment

- Hewlett Packard HP6624A DC power supply
- Tektronix TDS7404 Real Time Scope
- Agilent ParBERT E4832A

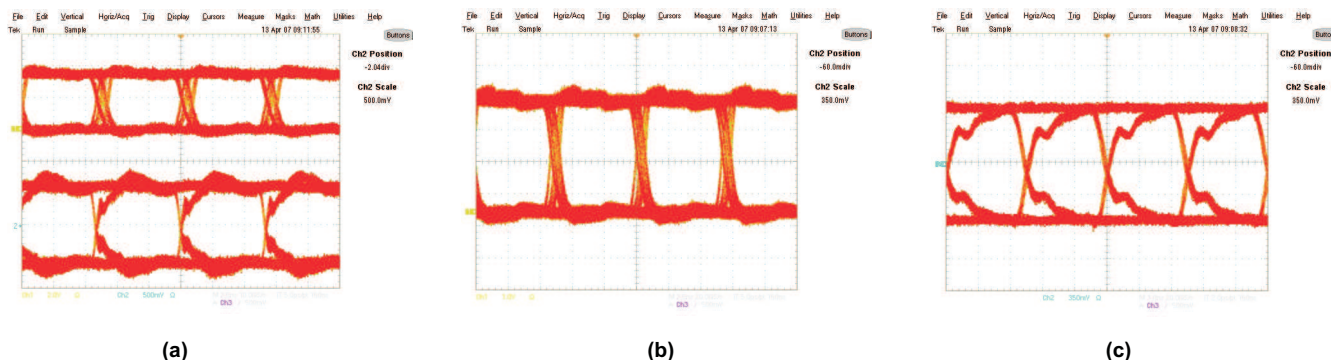


**Figure 17. Equipment Setup**



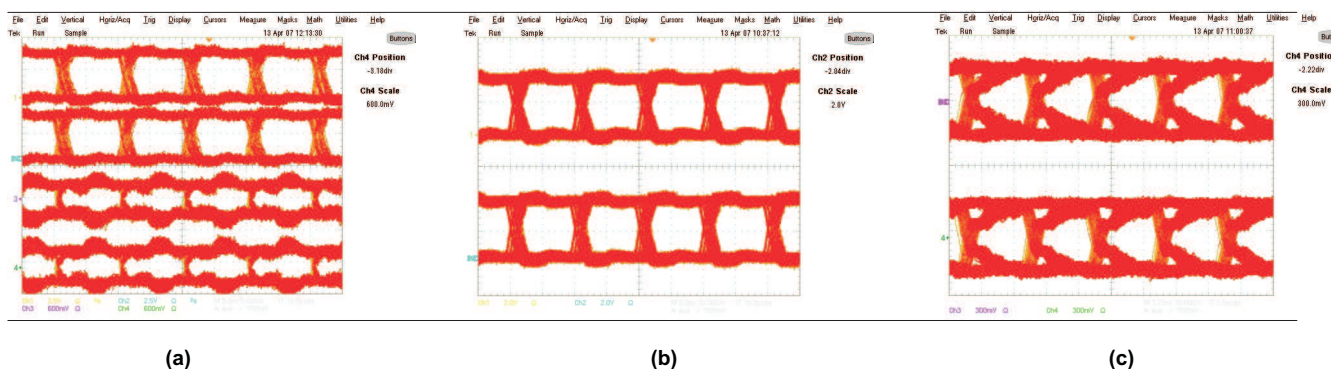
- Tx + Rx running at 150 Mbps; Channel 1: R, Channel 2: Y-Z
- Rx only running at 150 Mbps; Channel 1: R
- Tx only running at 400 Mbps; Channel 1: Y-Z

**Figure 18. Typical Eye Patterns SN65LVDS179: (T = 25°C; V<sub>CC</sub> = 3.6 V; PRBS = 2<sup>23-1</sup>)**



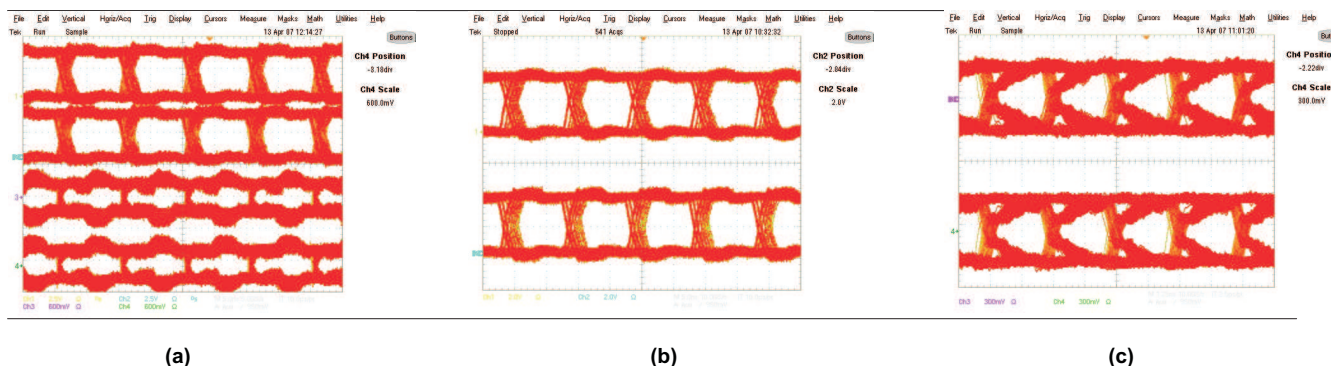
- Tx + Rx running at 150 Mbps; Channel 1: R, Channel 2: Y-Z
- Rx only running at 150 Mbps; Channel 1: R
- Tx only running at 400 Mbps; Channel 1: Y-Z

**Figure 19. Typical Eye Patterns SN65LVDS180: ( $T = 25^{\circ}\text{C}$ ;  $V_{CC} = 3.6\text{ V}$ ; PRBS =  $2^{23-1}$ )**



- All buffers running at 100 Mbps; Channel 1: R, Channel 2: 2R, Channel 3: 1Y-1Z, Channel 4: 2Y-2Z,
- Rx buffers only running at 100 Mbps; Channel 1: R, Channel 2: 2R
- Tx buffers only running at 400 Mbps; Channel 3: 1Y-1Z, Channel 4: 2Y-2Z,

**Figure 20. Typical Eye Patterns SN65LVDS050: ( $T = 25^{\circ}\text{C}$ ;  $V_{CC} = 3.6\text{ V}$ ; PRBS =  $2^{23-1}$ )**

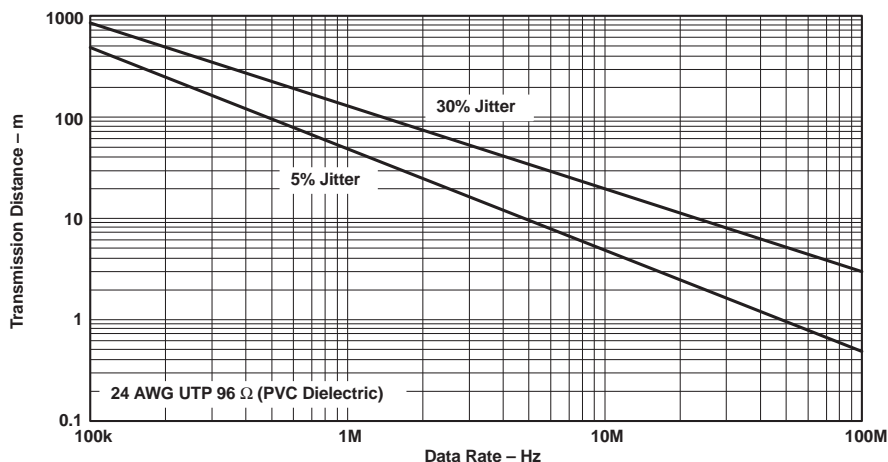


- All buffers running at 100 Mbps; Channel 1: R, Channel 2: 2R, Channel 3: 1Y-1Z, Channel 4: 2Y-2Z,
- Rx buffers only running at 100 Mbps; Channel 1: R, Channel 2: 2R
- Tx buffers only running at 400 Mbps; Channel 3: 1Y-1Z, Channel 4: 2Y-2Z,

**Figure 21. Typical Eye Patterns SN65LVDS051: ( $T = 25^{\circ}\text{C}$ ;  $V_{CC} = 3.6\text{ V}$ ; PRBS =  $2^{23-1}$ )**



The devices are generally used as building blocks for high-speed point-to-point data transmission. Ground differences are less than 1 V with a low common-mode output and balanced interface for low noise emissions. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers maintain ECL speeds without the power and dual supply requirements.

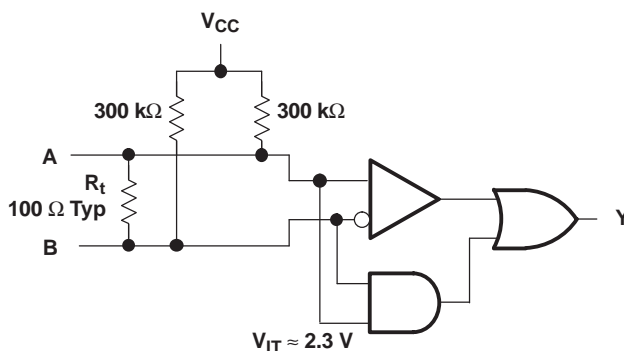


**Figure 22. Data Transmission Distance Versus Rate**

## FAIL SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between -100 mV and 100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near  $V_{CC}$  through 300-k $\Omega$  resistors as shown in Figure 11. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to  $V_{CC} - 0.4$  V to detect this condition and force the output to a high-level regardless of the differential input voltage.



**Figure 23. Open-Circuit Fail Safe of the LVDS Receiver**

It is only under these conditions that the output of the receiver will be valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor,  $R_t$ , does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS050D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS050	<a href="#">Samples</a>
SN65LVDS050DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS050	<a href="#">Samples</a>
SN65LVDS050DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS050	<a href="#">Samples</a>
SN65LVDS050DRG4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN65LVDS050PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LVDS050	<a href="#">Samples</a>
SN65LVDS050PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LVDS050	<a href="#">Samples</a>
SN65LVDS050PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LVDS050	<a href="#">Samples</a>
SN65LVDS050PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LVDS050	<a href="#">Samples</a>
SN65LVDS051D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051	<a href="#">Samples</a>
SN65LVDS051DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051	<a href="#">Samples</a>
SN65LVDS051DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051	<a href="#">Samples</a>
SN65LVDS051DRG4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN65LVDS051PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051	<a href="#">Samples</a>
SN65LVDS051PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051	<a href="#">Samples</a>
SN65LVDS051PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051	<a href="#">Samples</a>
SN65LVDS051PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051	<a href="#">Samples</a>
SN65LVDS179D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL179	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS179DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL179	<a href="#">Samples</a>
SN65LVDS179DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	S79	<a href="#">Samples</a>
SN65LVDS179DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	S79	<a href="#">Samples</a>
SN65LVDS179DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	S79	<a href="#">Samples</a>
SN65LVDS179DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	S79	<a href="#">Samples</a>
SN65LVDS179DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL179	<a href="#">Samples</a>
SN65LVDS179DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL179	<a href="#">Samples</a>
SN65LVDS180D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180	<a href="#">Samples</a>
SN65LVDS180DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180	<a href="#">Samples</a>
SN65LVDS180DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180	<a href="#">Samples</a>
SN65LVDS180DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180	<a href="#">Samples</a>
SN65LVDS180PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180	<a href="#">Samples</a>
SN65LVDS180PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180	<a href="#">Samples</a>
SN65LVDS180PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180	<a href="#">Samples</a>
SN65LVDS180PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN65LVDS050, SN65LVDS051, SN65LVDS179, SN65LVDS180 :**

● Automotive: [SN65LVDS050-Q1](#), [SN65LVDS051-Q1](#), [SN65LVDS180-Q1](#)

● Enhanced Product: [SN65LVDS179-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- 
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS050DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS050PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS051DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS179DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDS179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDS180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65LVDS180PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS050DR	SOIC	D	16	2500	367.0	367.0	38.0
SN65LVDS050PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN65LVDS051DR	SOIC	D	16	2500	367.0	367.0	38.0
SN65LVDS051PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN65LVDS179DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65LVDS179DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65LVDS180DR	SOIC	D	14	2500	367.0	367.0	38.0
SN65LVDS180PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

## DGK (S-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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