

## **TPS43331EVM**

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## 1 Introduction

The Texas Instruments TPS43331EVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS43331 Switch Mode Power Supply – Multiple-output voltage regulator.

**Table 1. Device and Package Configurations**

CONVERTER	IC	PACKAGE
U4	TPS43331QDAPRQ1	DAP-38

## 2 Setup

This section describes the jumpers and connectors on the EVM as well and how to properly connect, set up and use the TPS43331EVM.

### 2.1 2.1. Input/Output Connector Descriptions

**J1 – Input** is the power input terminal for the EVM. The terminal block provides a power (VIN) and ground (GND) connection.

**J2 – Output** is the output terminal for the TPS43331 Standby Linear. The terminal block provides a power (VSTBY) and ground (GND) connection.

**J3 – Output** is the output terminal for the TPS43331 Switched Linear Regulator. The terminal block provides a power (VLR) and ground (GND) connection.

**J4 – Output** is the regulated output voltage for converter 1 on the TPS43331. The terminal block provides a power (VOUT1) and ground (GND) connection.

**J5 – Output** is the regulated output voltage for converter 2 on the TPS43331. The terminal block provides a power (VOUT2) and ground (GND) connection.

**J6 – Output** is the output terminal for the TPS43331 high-side driver switch. The terminal block provides a power (HSD) and ground (GND) connection.

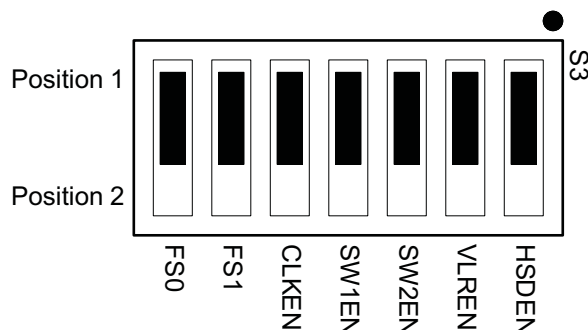
**J7 – Input** is the input terminal to apply an external I<sup>2</sup>C interface to the TPS43331. The terminal block provides SCL, SDA, and GND connections. The SCL and SDA jumpers should be removed if the external I<sup>2</sup>C interface is used.

**J8 – Input** is the input terminal to program the MSP430 controller device. The user should not need to use this connector.

#### Test Points

- EN – Enable input for Switcher 1
- CLK – External clock input
- GND (x6) – Ground
- HSD – High-side driver
- PH1 – Switcher 1 phase pin
- PH2 – Switcher 2 phase pin
- $\overline{\text{RST}}$  – Reset warning output
- VBAT – Power Input
- VBATW – Vbat warning output
- VIN – Power input after the reverse battery protection diode
- VLR – Switched linear regulator output
- VOUT1 – Switcher 1 output
- VOUT2 – Switcher 2 output
- VSTBY – Standby linear regulator output

**S3 – Control Switch** is a seven position DIP switch used to set the operating frequency, enable the external clock and control Switcher 1, Switcher 2, the switched linear regulator, and the high-side switch.



**Figure 1. Control Switch Diagram**

**FS0, FS1, and CLKEN** – Set the frequency and to enable the preprogrammed external clock from the MSP430 to the TPS43331 Synch input. The TPS43331 internal clock source is also used if the No Clock setting is selected. The user can also apply an optional user defined external clock to the CLK test point, if the User Defined setting is selected.

**Table 2. SYNCH Frequency Select and Enable Switch Settings**

Clock Frequency	FS0	FS1	CLKEN
No Clock	Position 2	Position 2	Don't care
250 kHz	Position 1	Position 2	Position 2
333 kHz	Position 2	Position 1	Position 2
400 kHz	Position 1	Position 1	Position 2
User Defined	Don't care	Don't care	Position 1

The frequency is set when power is applied to the EVM and cannot be changed after power-up. Set the switch to the desired frequency before applying power to the EVM.

The jumpers can also be used to disable the MSP430 during EMC testing. The procedure to disable the MSP430 is:

1. Set FS0 and FS1 to the No Clock setting before power up.
2. Apply power to the EVM.
3. Set the regulator conditions on the TPS43331 to be tested.
4. Set FS0 and FS1 to Position 1 to disable the MSP430.

**NOTE:** Power must be cycled to the EVM to turn the MSP430 back on and send new commands to the TPS43331 after EMC testing has been completed.

**SW1EN** – Used to control Switched Regulator 1 on the TPS43331. The switch can be moved at any time after power has been applied to the EVM. All regulators (except for the standby regulator) are disabled if Switcher 1 is disabled.

**Table 3. Switched Regulator 1 Switch Setting**

Switcher 1	SW1EN
Disabled	Position 1
Enabled	Position 2

**SW2EN** – Used to control Switched Regulator 2 on the TPS43331. The switch can be moved at any time after power has been applied to the EVM.

**Table 4. Switched Regulator 2 Switch Setting**

Switcher 2	SW2EN
Disabled	Position 1
Enabled	Position 2

**VLREN** – Used to control the switched linear regulator on the TPS43331. The switch can be moved at any time after power has been applied to the EVM.

**Table 5. Switched Linear Regulator Switch Setting**

Switched Linear	VLREN
Disabled	Position 1
Enabled	Position 2

**HSDEN** – Used to control the high-side switch on the TPS43331. The switch can be moved at any time after power has been applied to the EVM.

**Table 6. High-Side Driver Switch Setting**

High-Side Driver	HSDEN
Disabled	Position 1
Enabled	Position 2

**JP1 – Zener Bypass** is the jumper used to bypass the reverse battery protection diode.



**JP1**

*active*



**JP1**

*shorted*

**Figure 2. Reverse Battery Protection Diode Bypass Jumper Settings**

**JP2 – MSP430 Power** is the jumper used to enable the power supply to the MSP430. Power must be enabled to the MSP430 to control the TPS43331. The MSP430 can be disabled and maintain the state of the its outputs for EMC testing using the procedure listed under the SYNCH jumper settings, but power must be supplied to the MSP430.



**JP2**

*enabled*



**JP2**

*disabled*

**Figure 3. MSP430 Regulator Jumper Settings**

**SCL, SDA** – Jumpers used to disconnect the MSP430 from the I<sup>2</sup>C Interface on the TPS43331. External I<sup>2</sup>C interface signals can be applied using J8.



**Figure 4. I<sup>2</sup>C Interface Jumper Settings**

## 2.2 Setup

The input voltage range for the converter is 2 V to 30 V.

## 2.3 Operation

For proper operation of the TPS43331, S3, JP1, JP2, SCL and SDA should be properly configured. The following are the recommended settings, using the switch and shorting blocks:

- FS0 250 kHz
- FS1 250 kHz
- CLKEN enabled
- SW1EN disabled
- SW2EN disabled
- VLREN disabled
- HSDEN disabled
- JP1 active
- JP2 enabled
- SCL to MSP430
- SDA to MSP430

In this configuration, the regulators do not turn on when power is applied. Enable regulators using S3 after power has been applied to the EVM.

FS0 and FS1 select the frequency of the clock input to the SYNCH pin: 400 kHz, 333 kHz, 250 kHz, or no clock. CLKEN connects the clock signal to the SYNCH pin on the TPS43331. SW1EN turns switcher 1 on or off, disabled or enabled. SW2EN turns switcher 2 on or off, disabled or enabled. VLREN turns the switched linear regulator on or off, disabled or enabled. HSDEN turns high-side driver switch on or off, disabled. or enabled. JP1 removes the reverse battery protection diode from the circuit, active or shorted. JP2 controls the power to the MSP430, disabled or enabled. SCL / SDA connect the I<sup>2</sup>C interface of the MSP430 to the I<sup>2</sup>C interface of the TPS43331, external or MSP430.

### Regulator Configuration

- Switcher 1: 5.0 V
- Switcher 2: 3.3 V
- VLR: 8.0 V
- VSTBY: 2.5 V

## 3 Board Layout

Figure 5, Figure 6, Figure 7, Figure 8, Figure 9, and Figure 10 show the board layout for the TPS43331EVM PWB.

The TPS43331 is high efficiency but does dissipate power. The PowerPAD™ package offers an exposed thermal pad to enhance thermal performance. This must be soldered to the copper landing on the PCB for optimal performance. The PCB provides 1-oz copper planes on the top and bottom to dissipate heat.

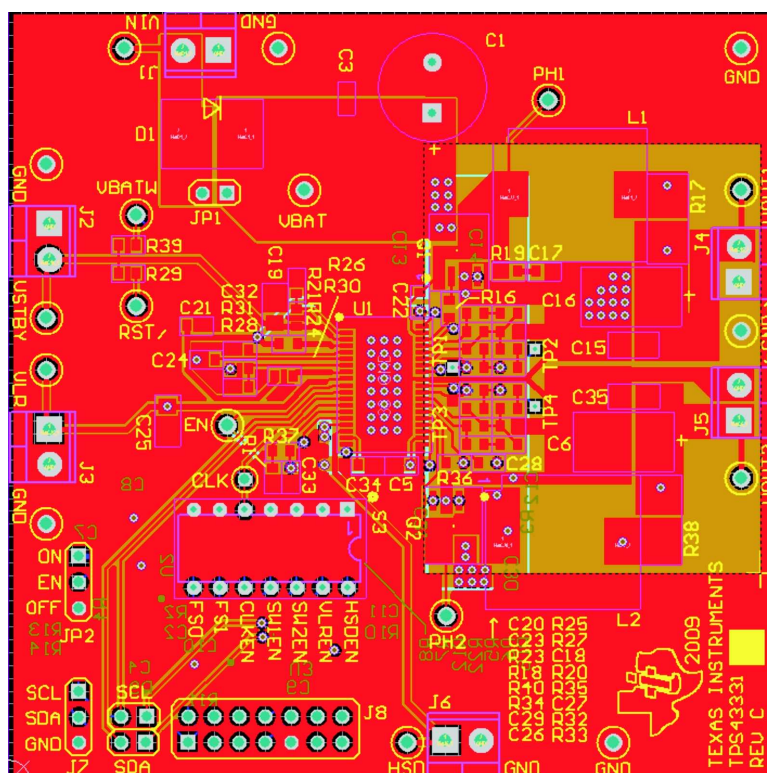


Figure 5. Top Assembly Layer

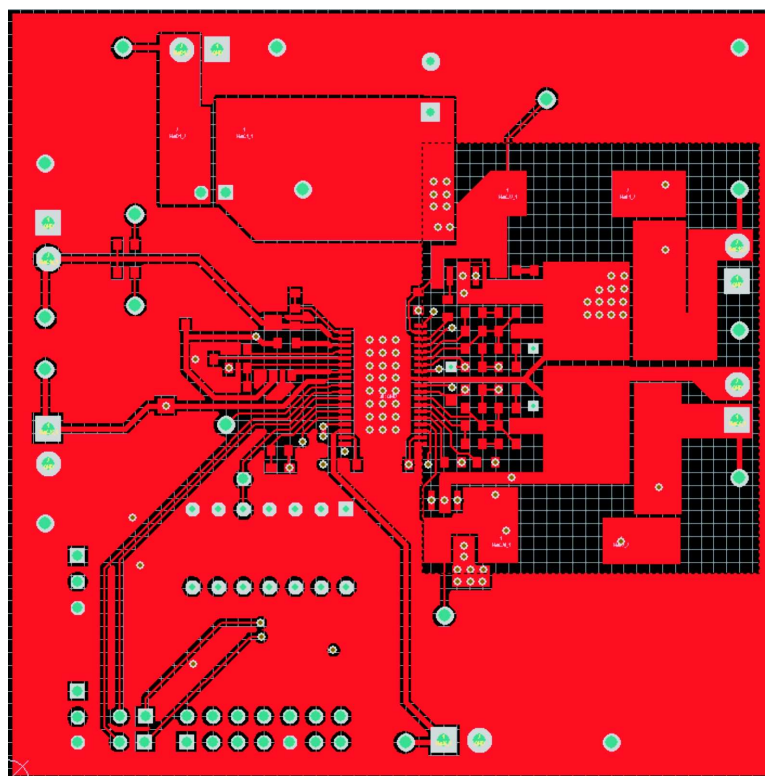
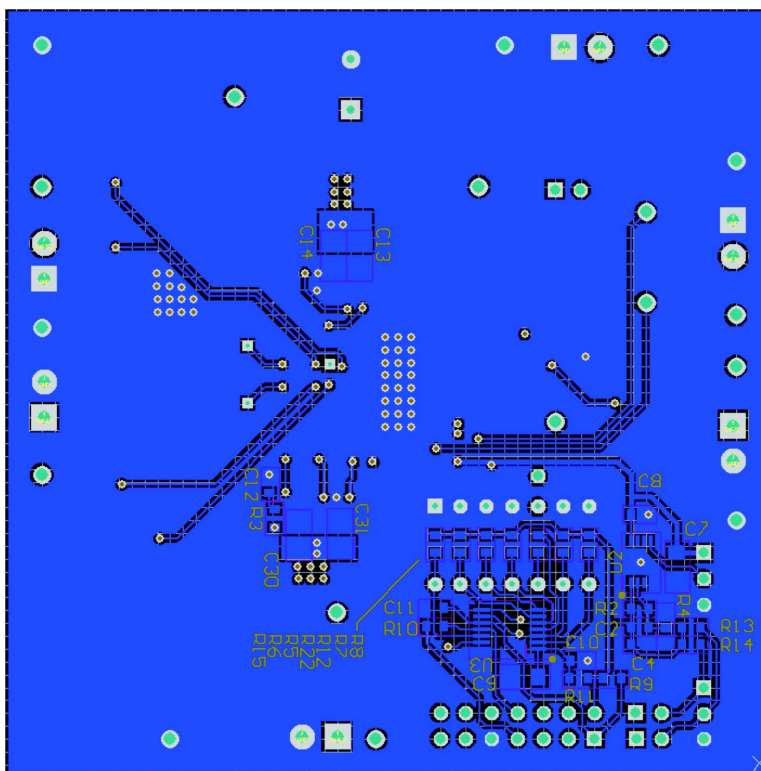
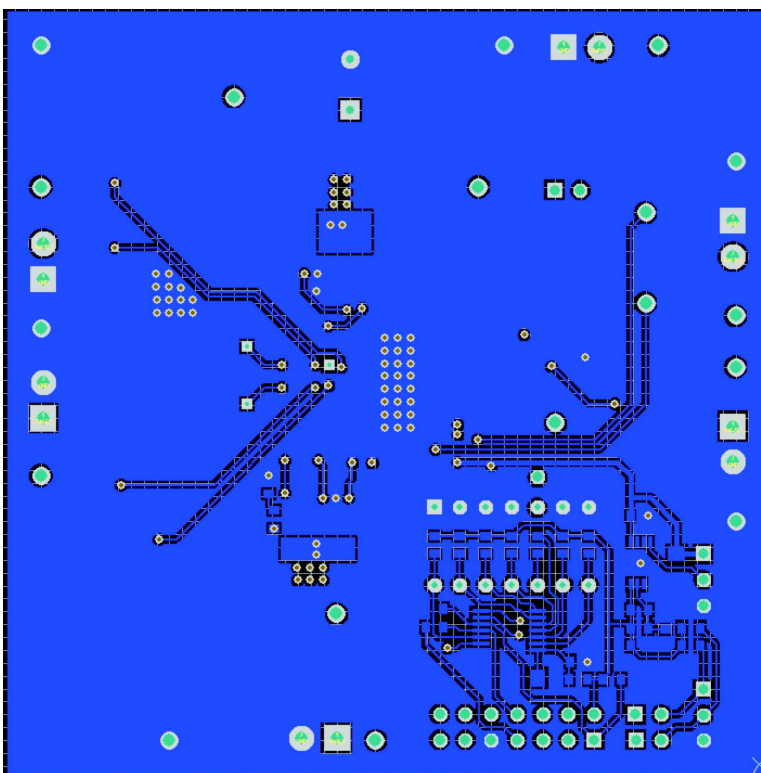


Figure 6. Top Layer Routing

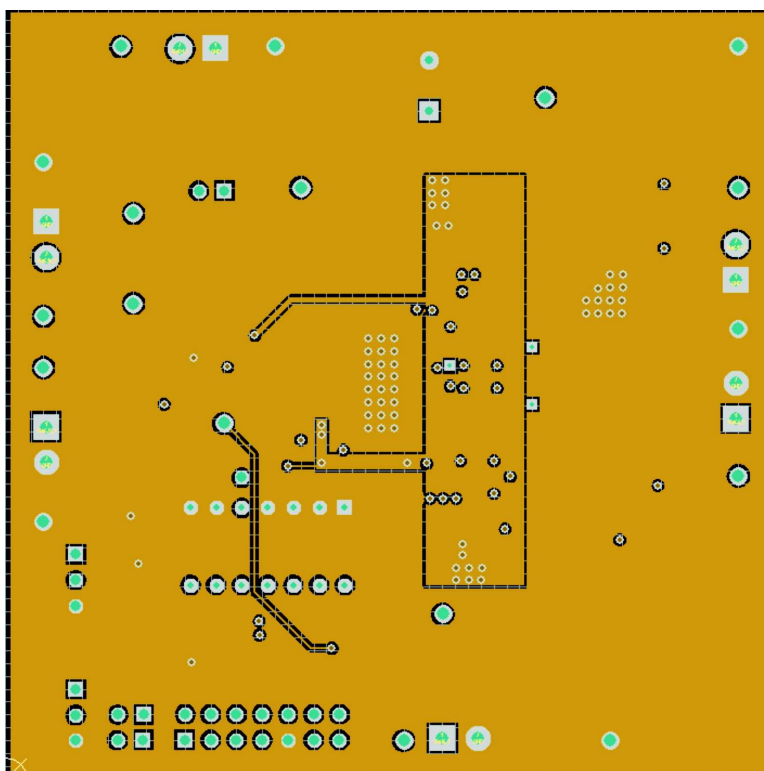


**Figure 7. Bottom Assembly Layer**

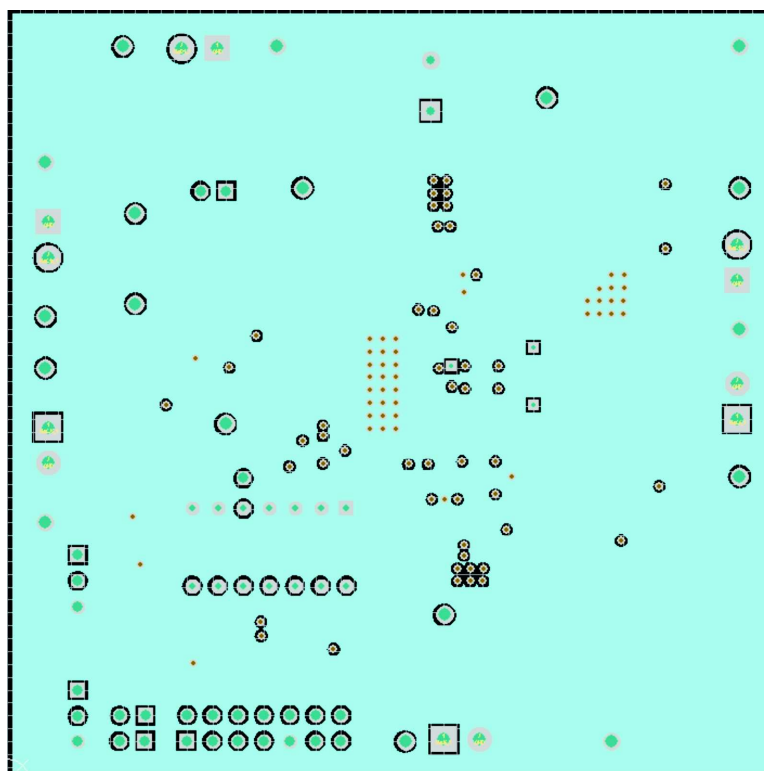


**Figure 8. Bottom Layer Routing**





**Figure 9. Internal Power Plane Layer**



**Figure 10. Internal Ground Plane Layer**



## 4 Schematics and Bill of Materials

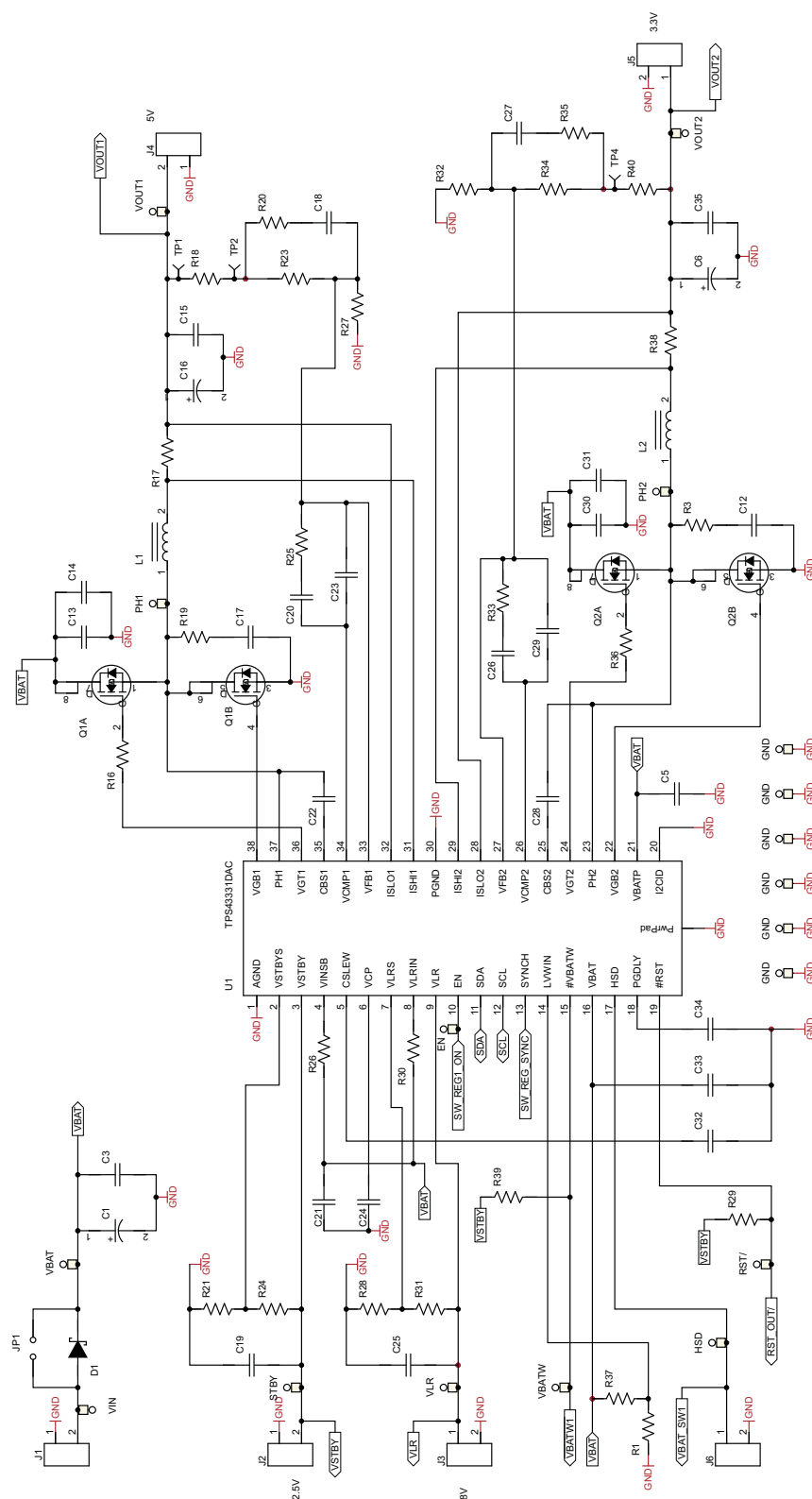


Figure 11. TPS43331EVM Schematic



**Table 7. TPS43331EVM Bill of Materials**

COUNT	REF DES	DESCRIPTION	SIZE	MFR	PART NUMBER
1	C1	Capacitor, electrolytic, 470mF, 50V, 20%	10mm x 20mm	Panasonic	ECA-1HHG471
2	C2, C11	Capacitor, ceramic, 100pF, 50V, 5%	603	muRata	GRM1885C1H101JA01D
9	C3, C5, C8, C10, C21, C22, C24, C28, C33	Capacitor, ceramic, 0.1mF, 50V, 10%	603	muRata	GRM188R71H104KA93D
1	C4	Capacitor, ceramic, 1mF, 16V, 10%	603	muRata	GRM185R61C105KE44B
2	C6, C16	Capacitor, ceramic, 100mF, 16V, 10%	7343-31	AVX	TPSD107M016R0060
1	C7	Capacitor, ceramic, 1mF, 50V, 10%	1206	muRata	GRM31CR71H105KA61L
3	C9, C19, C25	Capacitor, ceramic, 10mF, 16V, 10%	1206	muRata	GRM31CR61C106KC31L
4	C12, C17, C32, C34	Capacitor, ceramic, 1000pF, 50V, 10%	603	muRata	GRM188R71H102KA01D
4	C13, C14, C30, C31	Capacitor, ceramic, 4.7mF, 50V, 20%	1206	muRata	GRM31CF51H475ZA01L
2	C15, C35	Capacitor, ceramic, 2.2mF, 50V, 10%	1206	muRata	GRM31CR71H225KA88L
2	C18, C27	Capacitor, ceramic, 1200pF, 50V, 10%	603	muRata	GRM188R71H122KA01D
2	C20, C26	Capacitor, ceramic, 3300pF, 50V, 10%	603	muRata	GRM188R71H332KA01D
1	C23, C29	Capacitor, ceramic, 220pF, 50V, 10%	603	muRata	GRM188R71H221KA01D
1	D1	Diode, Schottky, 3A, 100V	SMC	IR	30BQ100
6	J1, J2, J3, J4, J5, J6	Terminal block, 2-pin, 6A, 3.5mm	0.25 x 0.27	OST	ED555/2DS
3	JP1, SCL, SDA	Header, 2-pin, 100-mil spacing, 36-pin strip	0.100 x 2	Sullins	PEC02SAAN
2	J7, JP2	Header, 3-pin, 100-mil spacing, 36-pin strip	0.100 x 3	Sullins	PEC03SAAN
1	J8	Dual row Header, 14-pin, 100-mil spacing, 72-pin strip	0.100 x 7	Sullins	PEC14DAAN
4	JP1, JP2, SCL, SDA,	Connector jumper, shorting, 100-mil spacing	0.1	Sullins	SPC02SYAN
2	L1, L2	Inductor, SMT, 22-uH, 5.44A, 52-mW	12.3mm x 12.3mm	Coilcraft	MSS1278T-223MLB
2	Q1, Q2	MOSFET, Dual N-Channel 60-V	SO8	Vishay	SI4946EY-T1-E3
1	R1	Resistor, chip, 1-M $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF1004V
1	R2	Resistor, chip, 158-k $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF1583V
4	R3, R16, R19, R36	Resistor, chip, 10- $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF10R0V
5	R4, R21, R28, R29, R39	Resistor, chip, 100-k $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF1003V
7	R5, R6, R7, R8, R15, R22, R27	Resistor, chip, 10-k $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF1002V
1	R9	Resistor, chip, 49.9-k $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF4992V
1	R10	Resistor, chip, 332- $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF3320V
3	R11, R26, R30	Resistor, chip, 0- $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3GEY0R00V
1	R12	Resistor, chip, 100- $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF1000V
2	R13, R14	Resistor, chip, 2.2-k $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF2201V
2	R17, R38	Resistor, chip, 0.03- $\Omega$ , 1W, 1%	2512	Vishay	WSL2512R0300FEA
2	R18, R40	Resistor, chip, 49.9- $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF49R9V
2	R20, R35	Resistor, chip, 1.1-k $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF1101V
2	R23, R34	Resistor, chip, 40.2-k $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF4022V

**Table 7. TPS43331EVM Bill of Materials (continued)**

COUNT	REF DES	DESCRIPTION	SIZE	MFR	PART NUMBER
1	R24	Resistor, chip, 150-k $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF1503V
2	R25, R33	Resistor, chip, 29.4-k $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF2942V
1	R31	Resistor, chip, 698-k $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF6983V
1	R32	Resistor, chip, 17.4-k $\Omega$ , 1/10W, 1%	603	Panasonic	ERJ-3EKF1742V
1	R37	Resistor, chip, 4.7-M $\Omega$ , 1/10W, 5%	603	Panasonic	ERJ-3GEYJ475V
1	S3	DIP Switch, 7 position	2.54mm pitch	C&K	BD07
19	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19	Test point, 52-mil	0.052	Kobiconn	151-103-RC
1	U2	IC, TPS79801DGN		TI	TPS79801QDGNRQ1
1	U3	IC, MSP430F2013PW		TI	MSP430F2013IPWR
1	U1	IC, TPS43331DAP		TI	TPS43331QDAPRQ1
1	-	PCB, 3-inch x 3-inch x 0.062		Any	TPS43331, REV C

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It is important to operate this EVM within the input voltage range of -0.3 V to 30 V and the output voltage range of 1.2 V to 10 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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