



# 5 V Low Power EIA RS-485 Transceiver

## ADM485

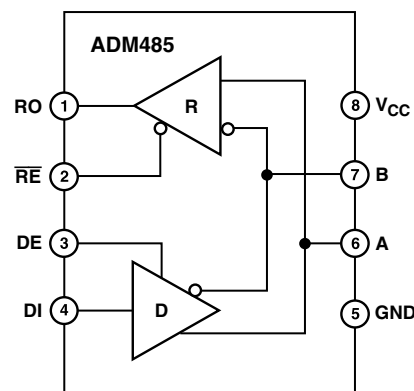
### FEATURES

- Meets EIA RS-485 Standard
- 5 Mbps Data Rate
- Single 5 V Supply
- 7 V to +12 V Bus Common-Mode Range
- High Speed, Low Power BiCMOS
- Thermal Shutdown Protection
- Short-Circuit Protection
- Driver Propagation Delay: 10 ns
- Receiver Propagation Delay: 15 ns
- High Z Outputs with Power Off
- Superior Upgrade for LTC485

### APPLICATIONS

- Low Power RS-485 Systems
- DTE-DCE Interface
- Packet Switching
- Local Area Networks
- Data Concentration
- Data Multiplexers
- Integrated Services Digital Network (ISDN)

### FUNCTIONAL BLOCK DIAGRAM



### GENERAL DESCRIPTION

The ADM485 is a differential line transceiver suitable for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced data transmission and complies with EIA Standards RS-485 and RS-422. The part contains a differential line driver and a differential line receiver. Both the driver and the receiver may be enabled independently. When disabled, the outputs are three-stated.

The ADM485 operates from a single 5 V power supply. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if during fault conditions a significant temperature increase is detected in the internal driver circuitry.

Up to 32 transceivers may be connected simultaneously on a bus, but only one driver should be enabled at any time. It is important, therefore, that the remaining disabled drivers do not load the bus. To ensure this, the ADM485 driver features high output impedance when disabled and when powered down.

This minimizes the loading effect when the transceiver is not being used. The high impedance driver output is maintained over the entire common-mode voltage range from -7 V to +12 V.

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM485 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology. All inputs and outputs contain protection against ESD; all driver outputs feature high source and sink current capability. An epitaxial layer is used to guard against latch-up.

The ADM485 features extremely fast switching speeds. Minimal driver propagation delays permit transmission at data rates up to 5 Mbps while low skew minimizes EMI interference.

The part is fully specified over the commercial and industrial temperature range and is available in PDIP, SOIC, and small footprint MSOP packages.

### REV. E

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.  
Tel: 781/329-4700 [www.analog.com](http://www.analog.com)  
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# ADM485—SPECIFICATIONS (V<sub>CC</sub> = 5 V ± 5%. All specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

| Parameter                                              | Min  | Typ | Max  | Unit | Test Conditions/Comments                                 |
|--------------------------------------------------------|------|-----|------|------|----------------------------------------------------------|
| <b>DRIVER</b>                                          |      |     |      |      |                                                          |
| Differential Output Voltage, V <sub>OD</sub>           |      |     | 5.0  | V    | R = ∞, Test Circuit 1                                    |
|                                                        | 2.0  |     | 5.0  | V    | V <sub>CC</sub> = 5 V, R = 50 Ω (RS-422), Test Circuit 1 |
|                                                        | 1.5  |     | 5.0  | V    | R = 27 Ω (RS-485), Test Circuit 1                        |
| V <sub>OD3</sub>                                       | 1.5  |     | 5.0  | V    | V <sub>TST</sub> = -7 V to +12 V, Test Circuit 2         |
| Δ V <sub>OD</sub>   for Complementary Output States    |      |     | 0.2  | V    | R = 27 Ω or 50 Ω, Test Circuit 1                         |
| Common-Mode Output Voltage, V <sub>OC</sub>            |      |     | 3    | V    | R = 27 Ω or 50 Ω, Test Circuit 1                         |
| Δ V <sub>OD</sub>   for Complementary Output States    |      |     | 0.2  | V    | R = 27 Ω or 50 Ω                                         |
| Output Short-Circuit Current (V <sub>OUT</sub> = High) | 35   |     | 250  | mA   | -7 V ≤ V <sub>O</sub> ≤ +12 V                            |
| Output Short-Circuit Current (V <sub>OUT</sub> = Low)  | 35   |     | 250  | mA   | -7 V ≤ V <sub>O</sub> ≤ +12 V                            |
| CMOS Input Logic Threshold Low, V <sub>INL</sub>       |      |     | 0.8  | V    |                                                          |
| CMOS Input Logic Threshold High, V <sub>INH</sub>      | 2.0  |     |      | V    |                                                          |
| Logic Input Current (DE, DI)                           |      |     | ±1.0 | μA   |                                                          |
| <b>RECEIVER</b>                                        |      |     |      |      |                                                          |
| Differential Input Threshold Voltage, V <sub>TH</sub>  | -0.2 |     | +0.2 | V    | -7 V ≤ V <sub>CM</sub> ≤ +12 V                           |
| Input Voltage Hysteresis, ΔV <sub>TH</sub>             |      | 70  |      | mV   | V <sub>CM</sub> = 0 V                                    |
| Input Resistance                                       | 12   |     |      | kΩ   | -7 V ≤ V <sub>CM</sub> ≤ +12 V                           |
| Input Current (A, B)                                   |      |     | 1    | mA   | V <sub>IN</sub> = 12 V                                   |
|                                                        |      |     | -0.8 | mA   | V <sub>IN</sub> = -7 V                                   |
| CMOS Input Logic Threshold Low, V <sub>INL</sub>       |      |     | 0.8  | V    |                                                          |
| CMOS Input Logic Threshold High, V <sub>INH</sub>      | 2.0  |     |      | V    |                                                          |
| Logic Enable Input Current ( $\overline{RE}$ )         |      |     | ±1   | μA   |                                                          |
| CMOS Output Voltage Low, V <sub>OL</sub>               |      |     | 0.4  | V    | I <sub>OUT</sub> = +4.0 mA                               |
| CMOS Output Voltage High, V <sub>OH</sub>              | 4.0  |     |      | V    | I <sub>OUT</sub> = -4.0 mA                               |
| Short-Circuit Output Current                           | 7    |     | 85   | mA   | V <sub>OUT</sub> = GND or V <sub>CC</sub>                |
| Three-State Output Leakage Current                     |      |     | ±1.0 | μA   | 0.4 V ≤ V <sub>OUT</sub> ≤ 2.4 V                         |
| <b>POWER SUPPLY CURRENT</b>                            |      |     |      |      |                                                          |
| I <sub>CC</sub> (Outputs Enabled)                      |      | 1.0 | 2.2  | mA   | Digital Inputs = GND or V <sub>CC</sub>                  |
| I <sub>CC</sub> (Outputs Disabled)                     |      | 0.6 | 1    | mA   | Digital Inputs = GND or V <sub>CC</sub>                  |

Specifications subject to change without notice.

## TIMING SPECIFICATIONS (V<sub>CC</sub> = 5 V ± 5%. All specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

| Parameter                                                                   | Min | Typ | Max | Unit | Test Conditions/Comments                                                              |
|-----------------------------------------------------------------------------|-----|-----|-----|------|---------------------------------------------------------------------------------------|
| <b>DRIVER</b>                                                               |     |     |     |      |                                                                                       |
| Propagation Delay Input to Output t <sub>PLH</sub> , t <sub>PHL</sub>       | 2   | 10  | 15  | ns   | R <sub>LDIFF</sub> = 54 Ω, C <sub>L1</sub> = C <sub>L2</sub> = 100 pF, Test Circuit 3 |
| Driver O/P to $\overline{O/P}$ , t <sub>SKEW</sub>                          |     | 1   | 5   | ns   | R <sub>LDIFF</sub> = 54 Ω, C <sub>L1</sub> = C <sub>L2</sub> = 100 pF, Test Circuit 3 |
| Driver Rise/Fall Time, t <sub>R</sub> , t <sub>F</sub>                      |     | 8   | 15  | ns   | R <sub>LDIFF</sub> = 54 Ω, C <sub>L1</sub> = C <sub>L2</sub> = 100 pF, Test Circuit 3 |
| Driver Enable to Output Valid                                               |     | 10  | 25  | ns   | R <sub>L</sub> = 110 Ω, C <sub>L</sub> = 50 pF, Test Circuit 4                        |
| Driver Disable Timing                                                       |     | 10  | 25  | ns   | R <sub>L</sub> = 110 Ω, C <sub>L</sub> = 50 pF, Test Circuit 4                        |
| Matched Enable Switching                                                    |     | 0   | 2   | ns   | R <sub>L</sub> = 110 Ω, C <sub>L</sub> = 50 pF, Test Circuit 4*                       |
| t <sub>AZH</sub> - t <sub>BZL</sub>  ,  t <sub>BZH</sub> - t <sub>AZL</sub> |     |     |     |      |                                                                                       |
| Matched Disable Switching                                                   |     | 0   | 2   | ns   | R <sub>L</sub> = 110 Ω, C <sub>L</sub> = 50 pF, Test Circuit 4*                       |
| t <sub>AHZ</sub> - t <sub>BLZ</sub>  ,  t <sub>BHZ</sub> - t <sub>ALZ</sub> |     |     |     |      |                                                                                       |
| <b>RECEIVER</b>                                                             |     |     |     |      |                                                                                       |
| Propagation Delay Input to Output, t <sub>PLH</sub> , t <sub>PHL</sub>      | 8   | 15  | 30  | ns   | C <sub>L</sub> = 15 pF, Test Circuit 5                                                |
| Skew  t <sub>PLH</sub> - t <sub>PHL</sub>                                   |     |     | 5   | ns   | C <sub>L</sub> = 15 pF, Test Circuit 5                                                |
| Receiver Enable, t <sub>EN1</sub>                                           |     | 5   | 20  | ns   | C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ, Test Circuit 6                         |
| Receiver Disable, t <sub>EN2</sub>                                          |     | 5   | 20  | ns   | C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ, Test Circuit 6                         |
| Tx Pulse Width Distortion                                                   |     | 1   |     | ns   |                                                                                       |
| Rx Pulse Width Distortion                                                   |     | 1   |     | ns   |                                                                                       |

\*Guaranteed by characterization.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS\*

(T<sub>A</sub> = 25°C, unless otherwise noted.)

|                                                    |                                   |
|----------------------------------------------------|-----------------------------------|
| V <sub>CC</sub> .....                              | –0.3 V to +7 V                    |
| Inputs                                             |                                   |
| Driver Input (DI) .....                            | –0.3 V to V <sub>CC</sub> + 0.3 V |
| Control Inputs (DE, $\overline{\text{RE}}$ ) ..... | –0.3 V to V <sub>CC</sub> + 0.3 V |
| Receiver Inputs (A, B) .....                       | –9 V to +14 V                     |
| Outputs                                            |                                   |
| Driver Outputs (A, B) .....                        | –9 V to +14 V                     |
| Receiver Output .....                              | –0.5 V to V <sub>CC</sub> + 0.5 V |
| Power Dissipation 8-Lead MSOP .....                | 900 mW                            |
| θ <sub>JA</sub> , Thermal Impedance .....          | 206°C/W                           |
| Power Dissipation 8-Lead PDIP .....                | 500 mW                            |
| θ <sub>JA</sub> , Thermal Impedance .....          | 130°C/W                           |
| Power Dissipation 8-Lead SOIC .....                | 450 mW                            |
| θ <sub>JA</sub> , Thermal Impedance .....          | 170°C/W                           |
| Operating Temperature Range                        |                                   |
| Commercial (J Version) .....                       | 0°C to 70°C                       |
| Industrial (A Version) .....                       | –40°C to +85°C                    |
| Storage Temperature Range .....                    | –65°C to +150°C                   |
| Lead Temperature (Soldering, 10 sec) .....         | 300°C                             |
| Vapor Phase (60 sec) .....                         | 215°C                             |
| Infrared (15 sec) .....                            | 220°C                             |

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

Table I. Transmitting

| Inputs |    | Outputs |   |
|--------|----|---------|---|
| DE     | DI | B       | A |
| 1      | 1  | 0       | 1 |
| 1      | 0  | 1       | 0 |
| 0      | X  | Z       | Z |

Table II. Receiving

| $\overline{\text{RE}}$ | Inputs A–B  | Output RO |
|------------------------|-------------|-----------|
| 0                      | ≥ +0.2 V    | 1         |
| 0                      | ≤ –0.2 V    | 0         |
| 0                      | Inputs Open | 1         |
| 1                      | X           | Z         |

## ORDERING GUIDE

| Model            | Temperature Range | Package Option | Branding |
|------------------|-------------------|----------------|----------|
| ADM485AN         | –40°C to +85°C    | N-8            | M41      |
| ADM485AR         | –40°C to +85°C    | R-8            |          |
| ADM485AR-REEL    | –40°C to +85°C    | R-8            |          |
| ADM485ARZ*       | –40°C to +85°C    | R-8            |          |
| ADM485ARZ-REEL*  | –40°C to +85°C    | R-8            |          |
| ADM485ARM        | –40°C to +85°C    | RM-8           |          |
| ADM485ARM-REEL   | –40°C to +85°C    | RM-8           |          |
| ADM485ARM-REEL7  | –40°C to +85°C    | RM-8           |          |
| ADM485JN         | 0°C to 70°C       | N-8            |          |
| ADM485JR         | 0°C to 70°C       | R-8            |          |
| ADM485JR-REEL    | 0°C to 70°C       | R-8            |          |
| ADM485JR-REEL7   | 0°C to 70°C       | R-8            |          |
| ADM485JRZ*       | 0°C to 70°C       | R-8            |          |
| ADM485JRZ-REEL*  | 0°C to 70°C       | R-8            |          |
| ADM485JRZ-REEL7* | 0°C to 70°C       | R-8            |          |

\*Z = Lead Free.

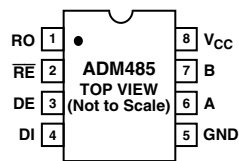
## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM485 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# ADM485

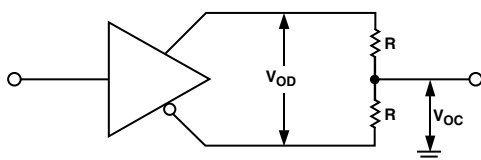
## PIN CONFIGURATION



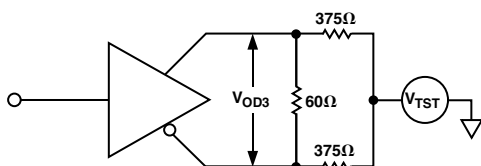
## PIN FUNCTION DESCRIPTIONS

| Pin No. | Mnemonic               | Function                                                                                                                              |
|---------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 1       | RO                     | Receiver Output. When enabled, if A > B by 200 mV, then RO = High. If A < B by 200 mV, then RO = Low.                                 |
| 2       | $\overline{\text{RE}}$ | Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state.                |
| 3       | DE                     | Driver Output Enable. A high level enables the driver differential outputs, A and B. A low level places it in a high impedance state. |
| 4       | DI                     | Driver Input. When the driver is enabled, a Logic Low on DI forces A low and B high while a Logic High on DI forces A high and B low. |
| 5       | GND                    | Ground Connection, 0 V.                                                                                                               |
| 6       | A                      | Noninverting Receiver Input A/Driver Output A.                                                                                        |
| 7       | B                      | Inverting Receiver Input B/Driver Output B.                                                                                           |
| 8       | V <sub>CC</sub>        | Power Supply, 5 V $\pm$ 5%.                                                                                                           |

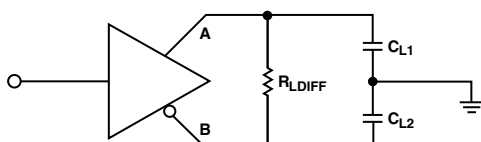
## Test Circuits



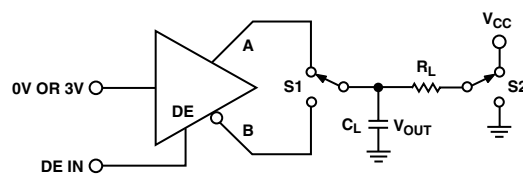
Test Circuit 1. Driver Voltage Measurement



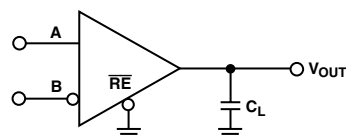
Test Circuit 2. Driver Voltage Measurement



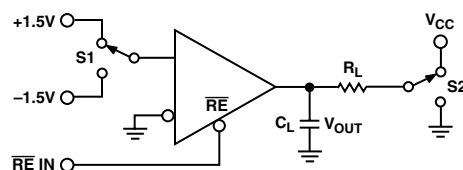
Test Circuit 3. Driver Propagation Delay



Test Circuit 4. Driver Enable/Disable



Test Circuit 5. Receiver Propagation Delay



Test Circuit 6. Receiver Enable/Disable

## Switching Characteristics

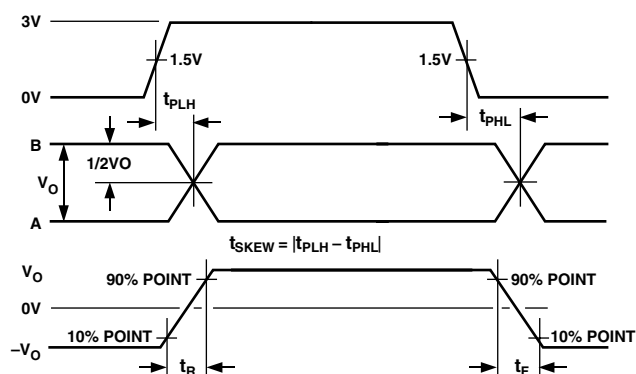


Figure 1. Driver Propagation Delay, Rise/Fall Timing

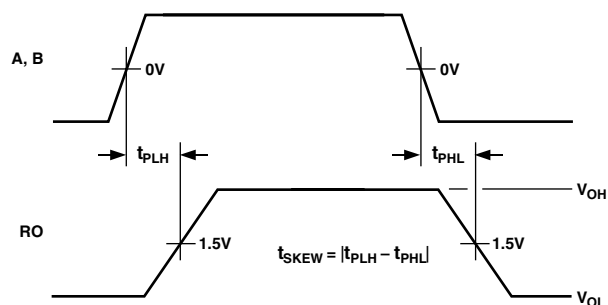


Figure 3. Receiver Propagation Delay

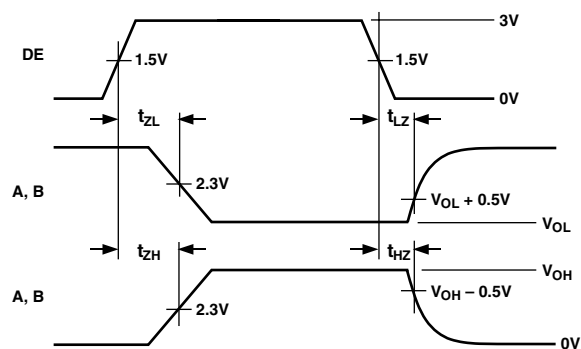


Figure 2. Driver Enable/Disable Timing

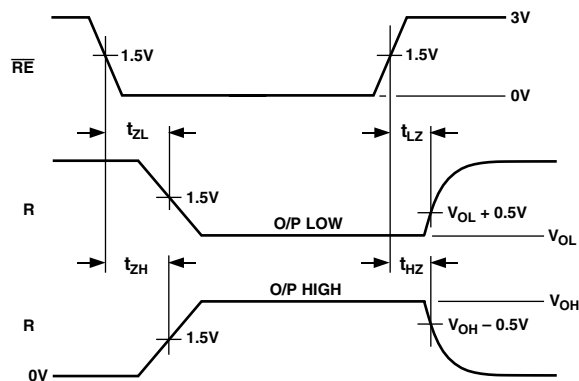
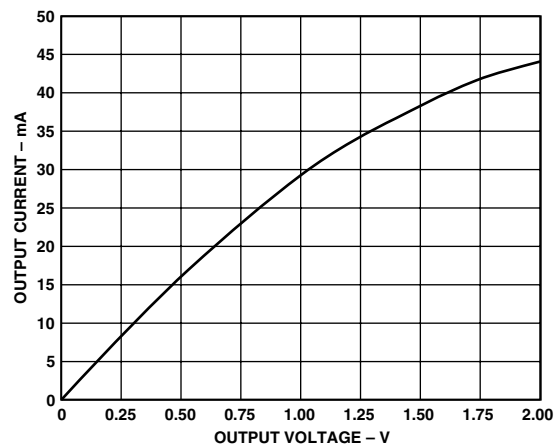
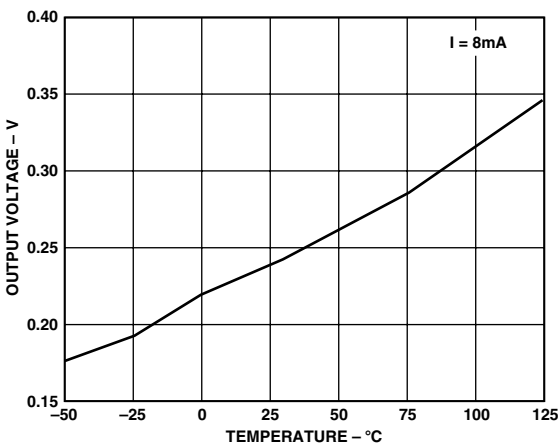


Figure 4. Receiver Enable/Disable Timing

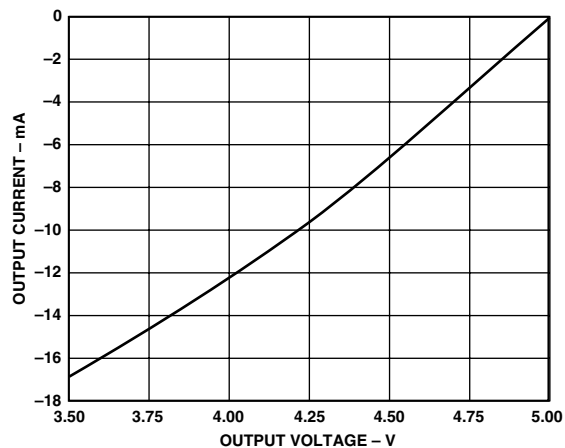
# ADM485—Typical Performance Characteristics



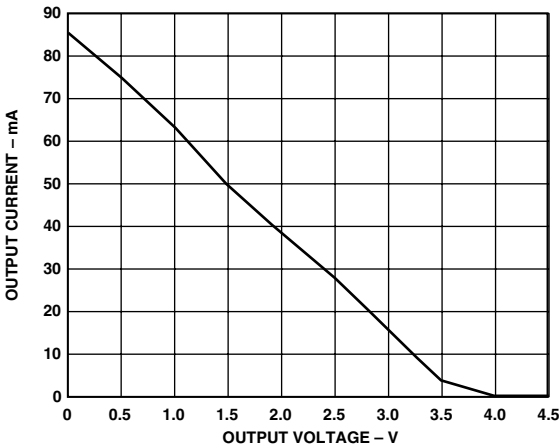
TPC 1. Output Current vs. Receiver Output Low Voltage



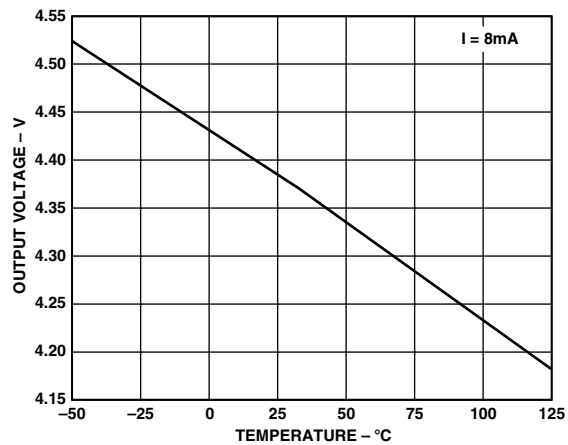
TPC 4. Receiver Output Low Voltage vs. Temperature



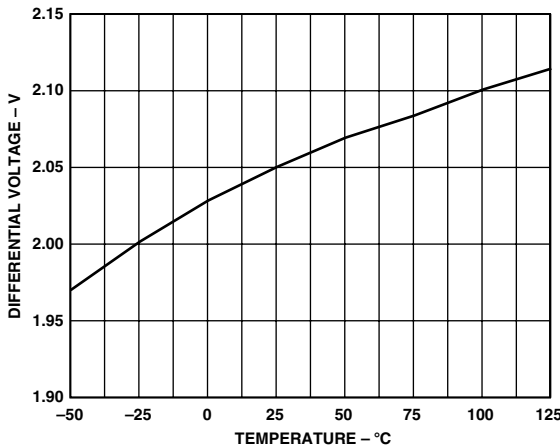
TPC 2. Output Current vs. Receiver Output High Voltage



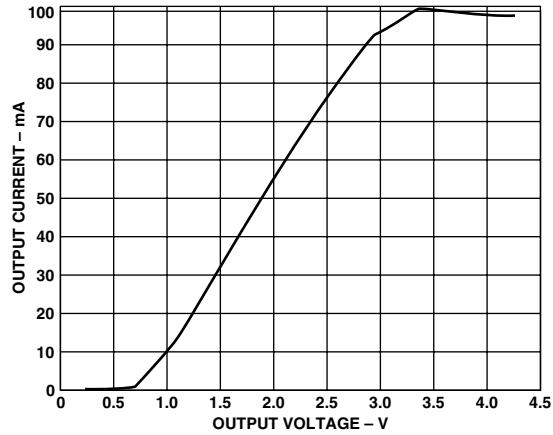
TPC 5. Output Current vs. Driver Differential Output Voltage



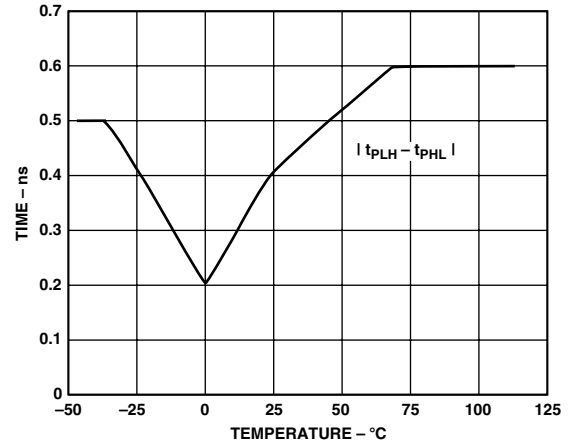
TPC 3. Receiver Output High Voltage vs. Temperature



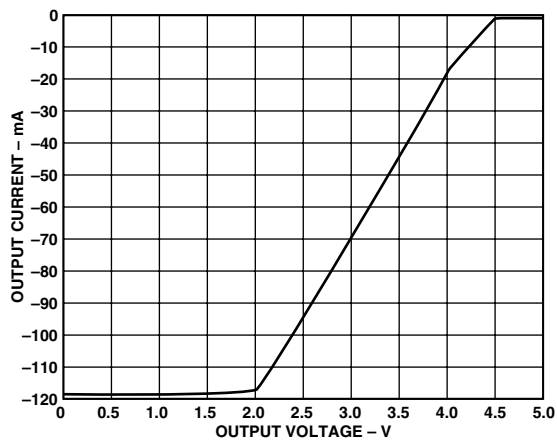
TPC 6. Driver Differential Output Voltage vs. Temperature,  $R_L = 26.8\ \Omega$



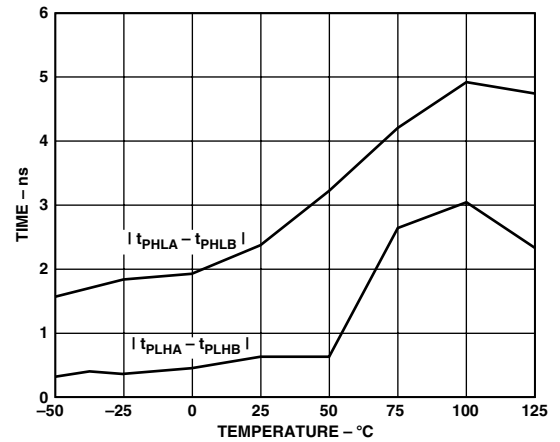
TPC 7. Output Current vs. Driver Output Low Voltage



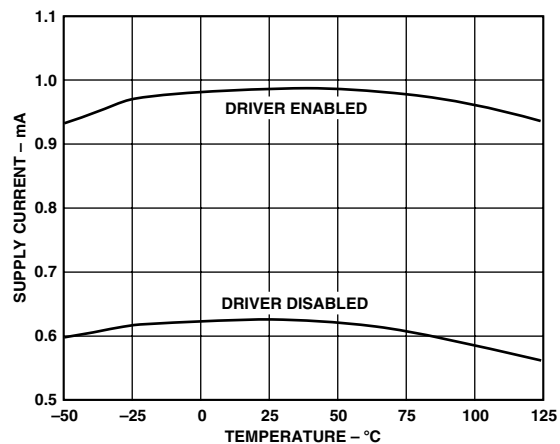
TPC 10. Rx Skew vs. Temperature



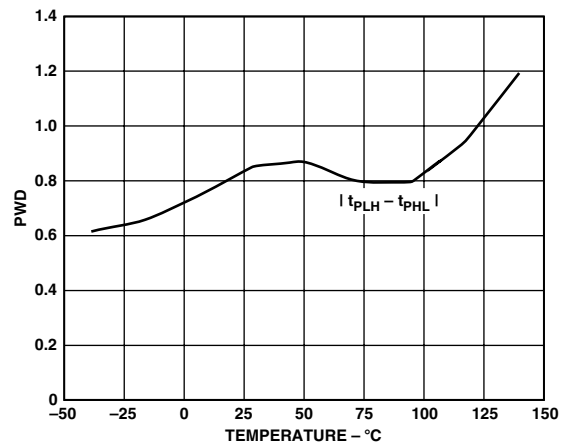
TPC 8. Output Current vs. Driver Output High Voltage



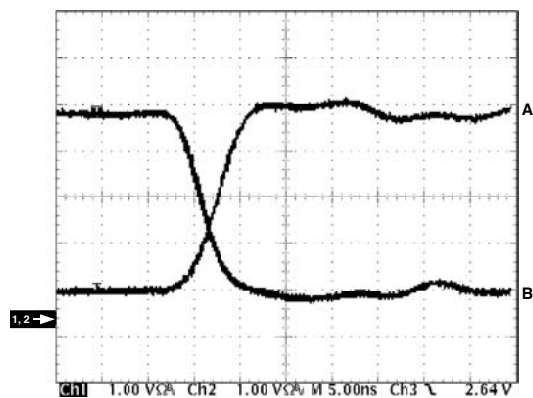
TPC 11. Tx Skew vs. Temperature



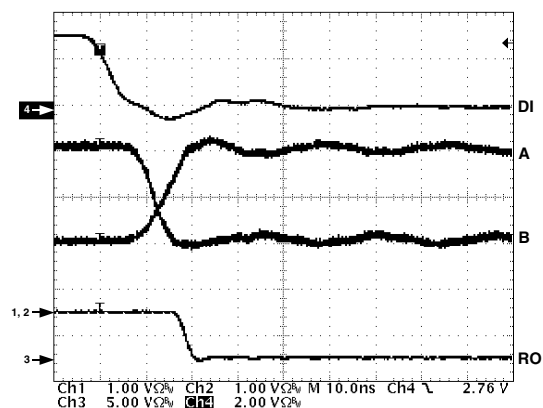
TPC 9. Supply Current vs. Temperature



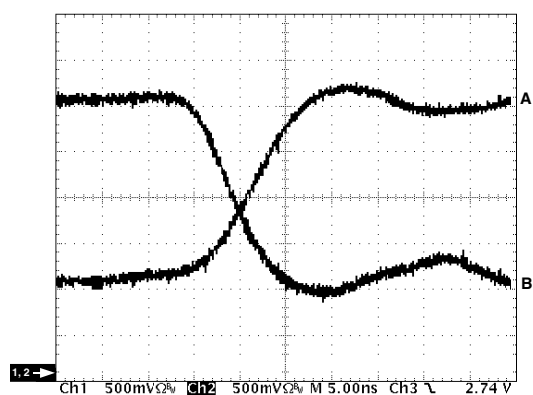
TPC 12. Tx Pulse Width Distortion



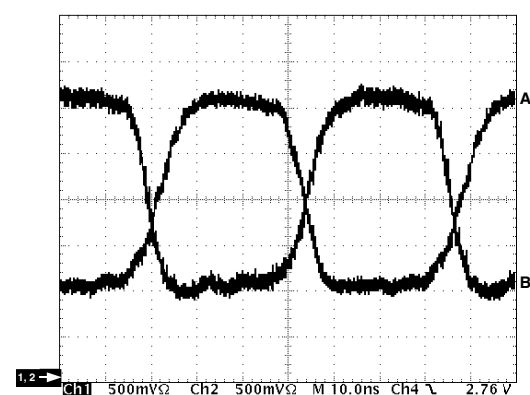
TPC 13. Unloaded Driver Differential Outputs



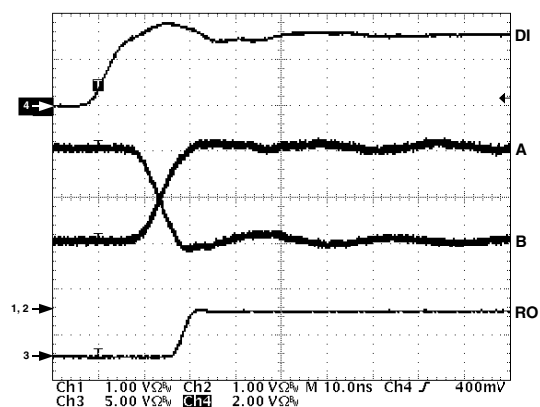
TPC 16. Driver/Receiver Propagation Delays High to Low



TPC 14. Loaded Driver Differential Outputs



TPC 17. Driver Output at 30 Mbps



TPC 15. Driver/Receiver Propagation Delays Low to High

## APPLICATION INFORMATION

### Differential Data Transmission

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals that appear as common-mode voltages on the line. There are two main standards approved by the Electronics Industries Association (EIA) that specify the electrical characteristics of transceivers used in differential data transmission.

The RS-422 standard specifies data rates up to 10 Mbaud and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.

In order to cater for true multipoint communications, the RS-485 standard was defined. This standard meets or exceeds all the requirements of RS-422 but also allows for up to 32 drivers and 32 receivers to be connected to a single bus. An extended common-mode range of  $-7\text{ V}$  to  $+12\text{ V}$  is defined. The most significant difference between RS-422 and RS-485 is the fact that the drivers may be disabled, thereby allowing more than one (32 in fact) to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

**Table III. Comparison of RS-422 and RS-485 Interface Standards**

| Specification                     | RS-422                         | RS-485                          |
|-----------------------------------|--------------------------------|---------------------------------|
| Transmission Type                 | Differential                   | Differential                    |
| Maximum Cable Length              | 4000 ft.                       | 4000 ft.                        |
| Minimum Driver Output Voltage     | $\pm 2\text{ V}$               | $\pm 1.5\text{ V}$              |
| Driver Load Impedance             | 100 $\Omega$                   | 54 $\Omega$                     |
| Receiver Input Resistance         | 4 k $\Omega$ min               | 12 k $\Omega$ min               |
| Receiver Input Sensitivity        | $\pm 200\text{ mV}$            | $\pm 200\text{ mV}$             |
| Receiver Input Voltage Range      | $-7\text{ V}$ to $+7\text{ V}$ | $-7\text{ V}$ to $+12\text{ V}$ |
| No. of Drivers/Receivers per Line | 1/10                           | 32/32                           |

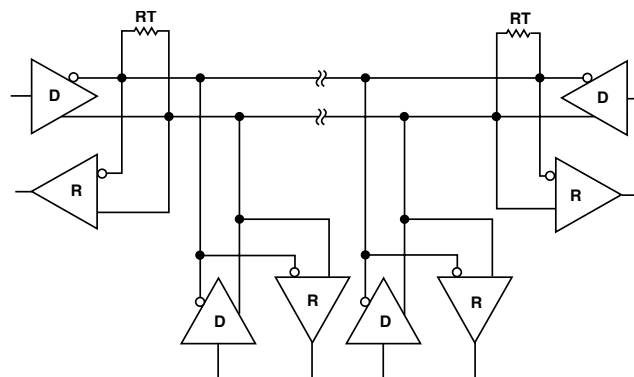
### Cable and Data Rate

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

The ADM485 is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 5. An RS-485 transmission line can have as many as 32 transceivers

on the bus. Only one driver can transmit at a particular time, but multiple receivers may be enabled simultaneously.

As with any transmission line, it is important that reflections be minimized. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.



**Figure 5. Typical RS-485 Network**

### Thermal Shutdown

The ADM485 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature and disables the driver outputs. The thermal sensing circuitry is designed to disable the driver outputs when a die temperature of  $150^{\circ}\text{C}$  is reached. As the device cools, the drivers are re-enabled at  $140^{\circ}\text{C}$ .

### Propagation Delay

The ADM485 features very low propagation delay, ensuring maximum baud rate operation. The driver is well balanced, ensuring distortion free transmission.

Another important specification is a measure of the skew between the complementary outputs. Excessive skew impairs the noise immunity of the system and increases the amount of electromagnetic interference (EMI).

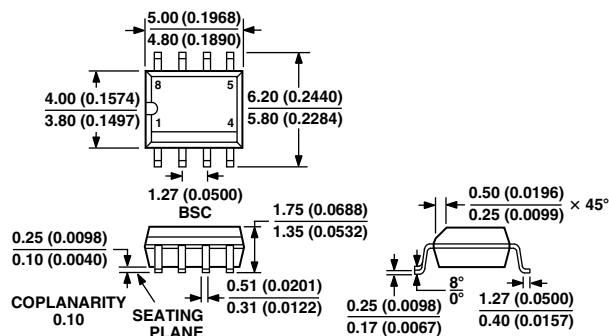
### Receiver Open-Circuit Fail-Safe

The receiver input includes a fail-safe feature that guarantees a Logic High on the receiver when the inputs are open circuit or floating.

## OUTLINE DIMENSIONS

### 8-Lead Standard Small Outline Package [SOIC] (R-8)

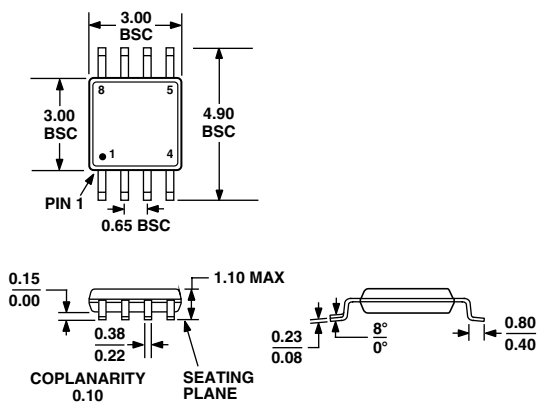
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

### 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

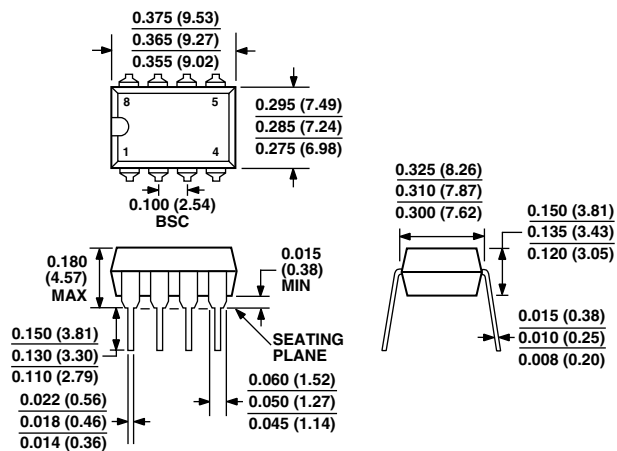


COMPLIANT TO JEDEC STANDARDS MO-187AA

## OUTLINE DIMENSIONS

**8-Lead Plastic Dual In-Line Package [PDIP]**  
**(N-8)**

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

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| Changes to TIMING SPECIFICATIONS .....                 | 2         |
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| <b>7/03—Data Sheet changed from REV. C to REV. D.</b>  |           |
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| <b>1/03—Data Sheet changed from REV. B to REV. C.</b>  |           |
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| <b>12/02—Data Sheet changed from REV. A to REV. B.</b> |           |
| Deleted Q-8 Package .....                              | Universal |
| Edits to FEATURES .....                                | 1         |
| Edits to GENERAL DESCRIPTION .....                     | 1         |
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| Edits, additions to ABSOLUTE MAXIMUM RATINGS .....     | 3         |
| Additions to ORDERING GUIDE .....                      | 3         |
| TPCs updated and reformatted .....                     | 5         |
| Addition of 8-Lead MSOP Package .....                  | 9         |
| Update to OUTLINE DIMENSIONS .....                     | 9         |

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