TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288-WORD BY 16-BIT FULL CMOS STATIC RAM

Lead-Free

DESCRIPTION

The TC55VCM316B, TC55VEM316B, TC55YCM316B and TC55YEM316B is a 8,388,608-bit static random access memory (SRAM) organized as 524,288 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.6 V/1.65 to 2.2 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 2 mA/MHz and a minimum cycle time of 45 ns. It is automatically placed in low-power mode at 0.6 μA standby current (at V_{DD} = 3 V, Ta = 25°C, typical) when chip enable ($\overline{CE1}$) is asserted high or (CE2) is asserted low. There are three control inputs. $\overline{CE1}$ and CE2 are used to select the device and for data retention control, and output enable ($\overline{OE}$) provides fast memory access. Data byte control pin ($\overline{LB}$, $\overline{UB}$) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating extreme temperature range of −40° to 85°C, the TC55VCM316B, TC55VEM316B, TC55YCM316B and TC55YEM316B can be used in environments exhibiting extreme temperature conditions. The TC55VCM316BTGN/BSGN, TC55YCM316BTGN/BSGN is available in a plastic 48-pin thin-small-outline package (TSOP). The TC55VEM316BXGN, TC55YEM316BXGN is available in a plastic 48-ball BGA.

FEATURES

- Low-power dissipation
  Operating: 6 mW/MHz (typical)
- Power down features using $\overline{CE1}$ and CE2
- Wide operating temperature range of −40° to 85°C
- Lead-Free

Part Number	Operating Supply Voltage	Package	Access time (MAX)		Supply Current		At Data Retention
			Supply Voltage 2.7~3.6 V	Supply Voltage 2.3~3.6 V	At Operating (MAX)	At Standby (MAX)	
TC55VCM316BTGN45	2.3~3.6 V	48-pin Plastic TSOP(I) (12×20mm) (0.5mm pin pitch) (Normal bent)	45 ns	55 ns	20 mA	10 μA	1.5~3.6 V
TC55VCM316BTGN55			55 ns	70 ns			
TC55VCM316BSGN45		48-pin Plastic TSOP(I) (12×14mm) (0.5mm pin pitch) (Normal bent)	45 ns	55 ns			
TC55VCM316BSGN55			55 ns	70 ns			
TC55VEM316BXGN45		48-ball BGA (6×7mm) (0.75mm ball pitch)	45 ns	55 ns			
TC55VEM316BXGN55			55 ns	70 ns			

Part Number	Operating Supply Voltage	Package	Access time (MAX)		Supply Current		At Data Retention
			Supply Voltage 1.8~2.2 V	Supply Voltage 1.65~2.2 V	At Operating (MAX)	At Standby (MAX)	
TC55YCM316BTGN55	1.65~2.2 V	48-pin Plastic TSOP(I) (12×20mm) (0.5mm pin pitch) (Normal bent)	55 ns	70 ns	12 mA	10 μA	1.0~2.2 V
TC55YCM316BTGN70			70 ns	85 ns			
TC55YCM316BSGN55		48-pin Plastic TSOP(I) (12×14mm) (0.5mm pin pitch) (Normal bent)	55 ns	70 ns			
TC55YCM316BSGN70			70 ns	85 ns			
TC55YEM316BXGN55		48-ball BGA (6×7mm) (0.75mm ball pitch)	55 ns	70 ns			
TC55YEM316BXGN70			70 ns	85 ns			

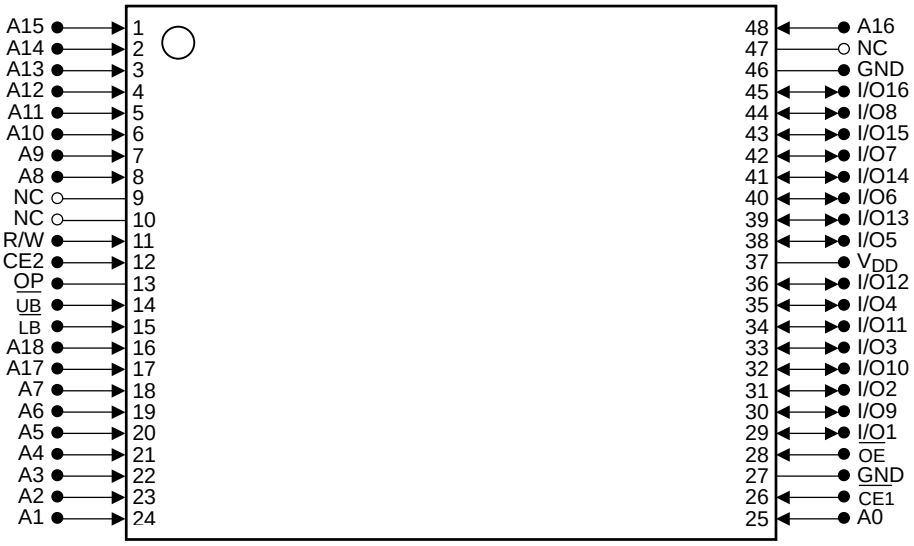
PIN ASSIGNMENT (TOP VIEW)

48-pin Plastic TSOP(I) (12×20mm) (0.5mm pin pitch) (Normal bent)

TC55VCM316BTGN
TC55YCM316BTGN

48-pin Plastic TSOP(I) (12×14mm) (0.5mm pin pitch) (Normal bent)

TC55VCM316BSGN
TC55YCM316BSGN



48-ball BGA (6×7mm) (0.75mm ball pitch)

TC55VEM316BXGN
TC55YEM316BXGN

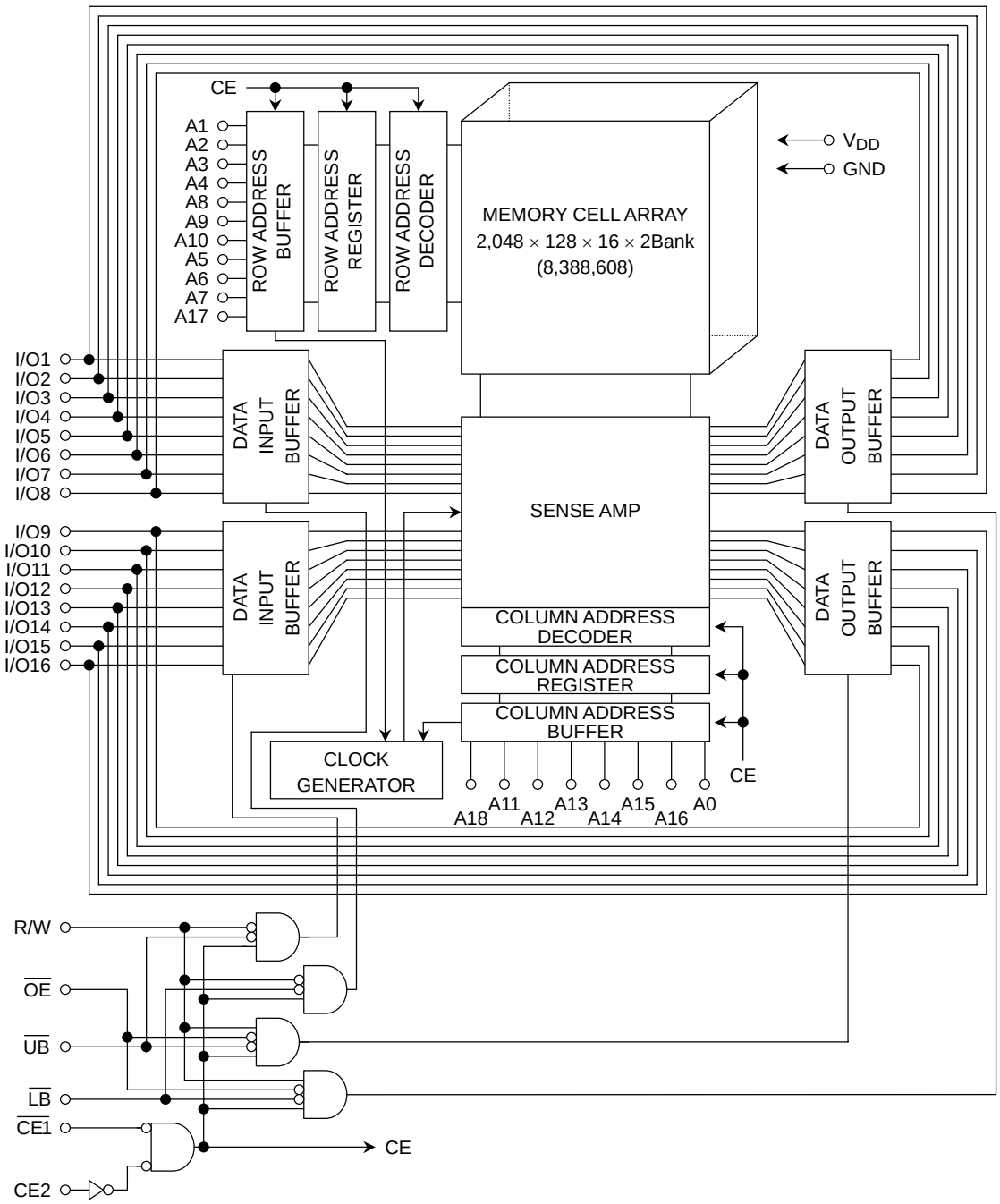
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CE2
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CE1}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	GND	I/O12	A17	A7	I/O4	V_{DD}
E	V_{DD}	I/O13	OP	A16	I/O5	GND
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	NC	A12	A13	R/W	I/O8
H	A18	A8	A9	A10	A11	NC

PIN NAMES

A0~A18	Address Inputs
$\overline{CE1}$, CE2	Chip Enable
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{LB}$, $\overline{UB}$	Data Byte Control
I/O1~I/O16	Data Inputs/Outputs
V_{DD}	Power
GND	Ground
NC	No Connection
OP*	Option

*: OP pin must be open or connected to GND.

BLOCK DIAGRAM



OPERATING MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1~I/O8	I/O9~I/O16	POWER
Read	L	H	L	H	L	L	Output	Output	I_{DDO}
	L	H	L	H	H	L	High-Z	Output	I_{DDO}
	L	H	L	H	L	H	Output	High-Z	I_{DDO}
Write	L	H	*	L	L	L	Input	Input	I_{DDO}
	L	H	*	L	H	L	High-Z	Input	I_{DDO}
	L	H	*	L	L	H	Input	High-Z	I_{DDO}
Output Deselect	L	H	H	H	L	L	High-Z	High-Z	I_{DDO}
	L	H	H	H	H	L	High-Z	High-Z	I_{DDO}
	L	H	H	H	L	H	High-Z	High-Z	I_{DDO}
Standby	H	*	*	*	*	*	High-Z	High-Z	I_{DDS}
	*	L	*	*	*	*	High-Z	High-Z	I_{DDS}

* = don't care
H = logic high
L = logic low

MAXIMUM RATINGS

SYMBOL	RATING		VALUE		UNIT
			TC55VCM316BTGN TC55VCM316BSGN TC55VEM316BXGN	TC55YCM316BTGN TC55YCM316BSGN TC55YEM316BXGN	
V_{DD}	Power Supply Voltage		−0.3~4.2	−0.3~2.5	V
V_{IN}	Input Voltage		−0.3[*1]~4.2	−0.3[*1]~2.5	V
$V_{I/O}$	Input/Output Voltage		−0.5~V_{DD} + 0.5	−0.5~V_{DD} + 0.5	V
P_D	Power Dissipation		0.6	0.6	W
T_{solder}	Soldering Temperature (10s)		260	260	°C
T_{stg}	Storage Temperature	TSOP type	−55~150	−55~150	°C
		BGA type	−55~125	−55~125	°C
T_a	Operating Ambient Temperature		−40~85	−40~85	°C

[*1]: −1.0 V when measured at a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = −40° to 85°C)

SYMBOL	PARAMETER	TEST CONDITION	TC55VCM316BTGN TC55VCM316BSGN TC55VEM316BXGN		TC55YCM316BTGN TC55YCM316BSGN TC55YEM316BXGN		UNIT
			MIN	MAX	MIN	MAX	
V_{DD}	Power Supply Voltage	—	2.3	3.6	1.65	2.2	V
V_{IH}	Input High Voltage	2.3 V ≤ V_{DD} < 2.7 V	2.0	V_{DD} + 0.3	—	—	
		2.7 V ≤ V_{DD} ≤ 3.6 V	2.2	V_{DD} + 0.3	—	—	
		1.65 V ≤ V_{DD} < 1.8 V	—	—	1.4	V_{DD} + 0.3	
		1.8 V ≤ V_{DD} ≤ 2.2 V	—	—	1.6	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	—	−0.3[*2]	V_{DD} × 0.24	−0.3[*2]	V_{DD} × 0.22	
V_{DH}	Data Retention Supply Voltage	—	1.5	3.6	1.0	2.2	

[*2]: −1.0 V when measured at a pulse width of 10ns

DC CHARACTERISTICS (Ta = –40° to 85°C, V_{DD} = 2.3 to 3.6 V/1.65 to 2.2 V)

SYMBOL	PARAMETER	TEST CONDITION			TC55VCM316BTGN TC55VCM316BSGN TC55VEM316BXGN			TC55YCM316BTGN TC55YCM316BSGN TC55YEM316BXGN			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Leakage Current	V_{IN} = 0 V~V_{DD}			—	—	±1.0	—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH} = V_{DD} – 0.5 V			–0.5	—	—	–0.5	—	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V			2.1	—	—	2.1	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{LB}$ = $\overline{UB}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 V~V_{DD}			—	—	±1.0	—	—	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH}, I_{OUT} = 0 mA, Other Input = V_{IH}/V_{IL}	t_{cycle}	MIN	—	—	20	—	—	12	mA
				1 μs	—	—	7	—	—	3	
I_{DDO2}		$\overline{CE1}$ = 0.2 V and CE2 = V_{DD} – 0.2 V and R/W = V_{DD} – 0.2 V, I_{OUT} = 0 mA, Other Input = V_{DD} – 0.2 V/0.2 V	t_{cycle}	MIN	—	—	20	—	—	12	mA
				1 μs	—	—	2	—	—	2	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			—	—	1	—	—	1	mA
I_{DDS2}		1) $\overline{CE1}$ = V_{DD} – 0.2 V, CE2 = V_{DD} – 0.2 V 2) CE2 = 0.2 V	V_{DD} = 2.3~3.6 V	Ta = –40~85°C	—	—	10	—	—	—	μA
			V_{DD} = 3.0 V	Ta = 25°C	—	0.6	0.9	—	—	—	
				Ta = –40~40°C	—	—	2	—	—	—	
			V_{DD} = 1.65~2.2 V	Ta = –40~85°C	—	—	—	—	—	10	
			V_{DD} = 1.8 V	Ta = 25°C	—	—	—	—	0.6	0.9	

Note: In standby mode with $\overline{CE1} \geq V_{DD} - 0.2$ V, these limits are assured for the condition CE2 ≥ V_{DD} – 0.2 V or CE2 ≤ 0.2 V. The other input pins are not restricted of input level.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = –40° to 85°C)

READ CYCLE

SYMBOL	PARAMETER	TC55VCM316BTGN/BSGN TC55VEM316BXGN								UNIT
		V_{DD} = 2.7~3.6 V				V_{DD} = 2.3~3.6 V				
		45		55		45		55		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	45	—	55	—	55	—	70	—	ns
t_{ACC}	Address Access Time	—	45	—	55	—	55	—	70	
t_{CO1}	Chip Enable($\overline{CE1}$) Access Time	—	45	—	55	—	55	—	70	
t_{CO2}	Chip Enable(CE2) Access Time	—	45	—	55	—	55	—	70	
t_{OE}	Output Enable Access Time	—	25	—	30	—	30	—	35	
t_{BA}	Data Byte Control Access Time	—	25	—	30	—	30	—	35	
t_{COE}	Chip Enable Low to Output Active	5	—	5	—	5	—	5	—	
t_{OEE}	Output Enable Low to Output Active	0	—	0	—	0	—	0	—	
t_{BE}	Data Byte Control Low to Output Active	0	—	0	—	0	—	0	—	
t_{OD}	Chip Enable High to Output High-Z	—	20	—	25	—	25	—	30	
t_{ODO}	Output Enable High to Output High-Z	—	20	—	25	—	25	—	30	
t_{BD}	Data Byte Control High to Output High-Z	—	20	—	25	—	25	—	30	
t_{OH}	Output Data Hold Time	10	—	10	—	10	—	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC55VCM316BTGN/BSGN TC55VEM316BXGN								UNIT
		V_{DD} = 2.7~3.6 V				V_{DD} = 2.3~3.6 V				
		45		55		45		55		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	45	—	55	—	55	—	70	—	ns
t_{WP}	Write Pulse Width	30	—	40	—	40	—	50	—	
t_{CW}	Chip Enable to End of Write	35	—	45	—	45	—	55	—	
t_{BW}	Data Byte Control to End of Write	35	—	45	—	45	—	55	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	
t_{ODW}	R/W Low to Output High-Z	—	20	—	25	—	25	—	30	
t_{OEW}	R/W High to Output Active	0	—	0	—	0	—	0	—	
t_{DS}	Data Setup Time	20	—	25	—	25	—	30	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	

Note: t_{OD}, t_{ODO}, t_{BD} and t_{ODW} are specified in time when an output becomes high impedance, and are not judged depending on an output voltage level.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = –40° to 85°C)

READ CYCLE

SYMBOL	PARAMETER	TC55YCM316BTGN/BSGN TC55YEM316BXGN								UNIT
		V_{DD} = 1.8~2.2 V				V_{DD} = 1.65~2.2 V				
		55		70		55		70		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	55	—	70	—	70	—	85	—	ns
t_{ACC}	Address Access Time	—	55	—	70	—	70	—	85	
t_{CO1}	Chip Enable($\overline{CE1}$) Access Time	—	55	—	70	—	70	—	85	
t_{CO2}	Chip Enable(CE2) Access Time	—	55	—	70	—	70	—	85	
t_{OE}	Output Enable Access Time	—	30	—	35	—	35	—	45	
t_{BA}	Data Byte Control Access Time	—	30	—	35	—	35	—	45	
t_{COE}	Chip Enable Low to Output Active	5	—	5	—	5	—	5	—	
t_{OEE}	Output Enable Low to Output Active	0	—	0	—	0	—	0	—	
t_{BE}	Data Byte Control Low to Output Active	0	—	0	—	0	—	0	—	
t_{OD}	Chip Enable High to Output High-Z	—	25	—	30	—	30	—	35	
t_{ODO}	Output Enable High to Output High-Z	—	25	—	30	—	30	—	35	
t_{BD}	Data Byte Control High to Output High-Z	—	25	—	30	—	30	—	35	
t_{OH}	Output Data Hold Time	10	—	10	—	10	—	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC55YCM316BTGN/BSGN TC55YEM316BXGN								UNIT
		V_{DD} = 1.8~2.2 V				V_{DD} = 1.65~2.2 V				
		55		70		55		70		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	55	—	70	—	70	—	85	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	50	—	60	—	
t_{CW}	Chip Enable to End of Write	45	—	55	—	55	—	65	—	
t_{BW}	Data Byte Control to End of Write	45	—	55	—	55	—	65	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	
t_{ODW}	R/W Low to Output High-Z	—	25	—	30	—	30	—	35	
t_{OEW}	R/W High to Output Active	0	—	0	—	0	—	0	—	
t_{DS}	Data Setup Time	25	—	30	—	30	—	35	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	

Note: t_{OD}, t_{ODO}, t_{BD} and t_{ODW} are specified in time when an output becomes high impedance, and are not judged depending on an output voltage level.

AC TEST CONDITIONS (Ta = –40 to 85°C, V_{DD} = 2.3 to 3.6 V/1.65 to 2.2 V)

PARAMETER		TEST CONDITION	
		TC55VCM316BTGN TC55VCM316BSGN TC55VEM316BXGN	TC55YCM316BTGN TC55YCM316BSGN TC55YEM316BXGN
Input pulse level	High	$V_{DD} \times 0.7 + 0.2$ V	$V_{DD} - 0.2$ V
	Low	0.2 V	0.2 V
Input rise and fall time (Fig.1)	t_R	1 V/ns	1 V/ns
	t_F	1 V/ns	1 V/ns
Timing measurements		$V_{DD} \times 0.5$	$V_{DD} \times 0.5$
Reference level		$V_{DD} \times 0.5$	$V_{DD} \times 0.5$
Output load (Fig.2)	V_{TM}	2.3 V	1.65 V
	R1	810 Ω	470 Ω
	R2	1610 Ω	740 Ω
	C_L	30 pF	30 pF

Fig.1 : Input rise and fall time

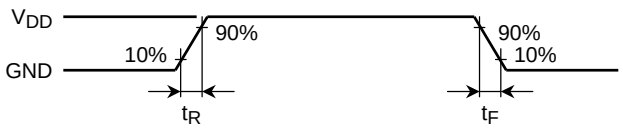
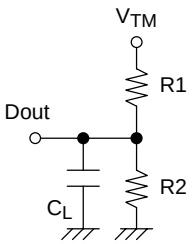
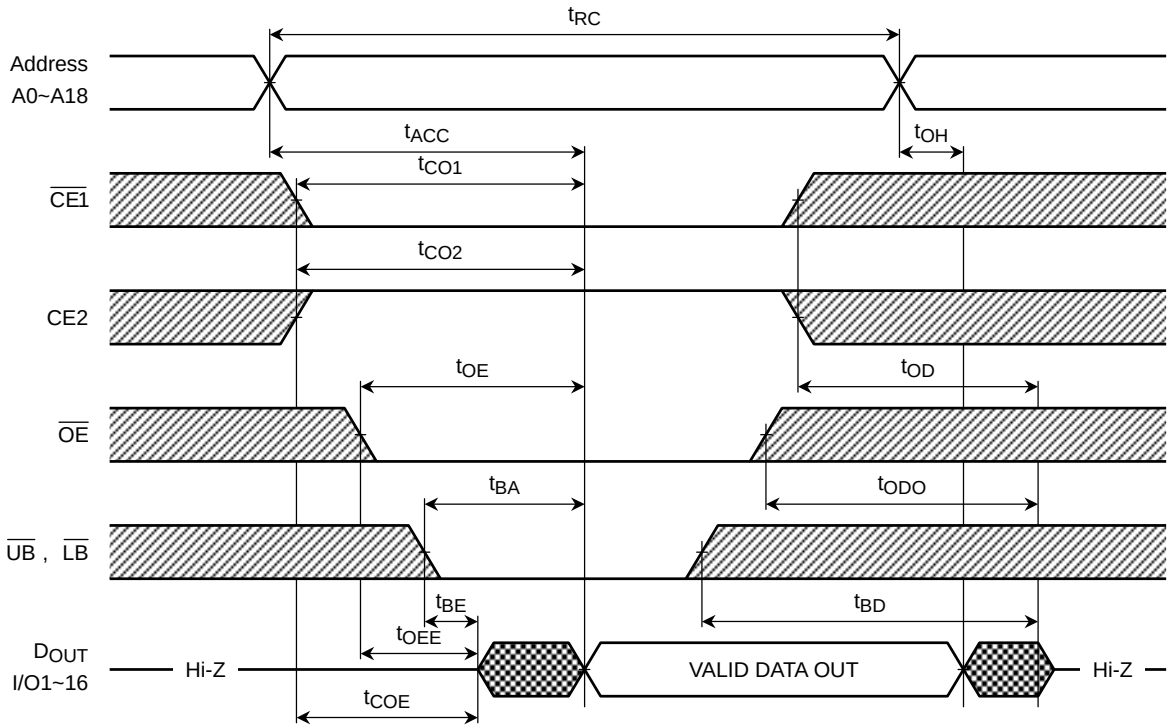


Fig.2 : Output load

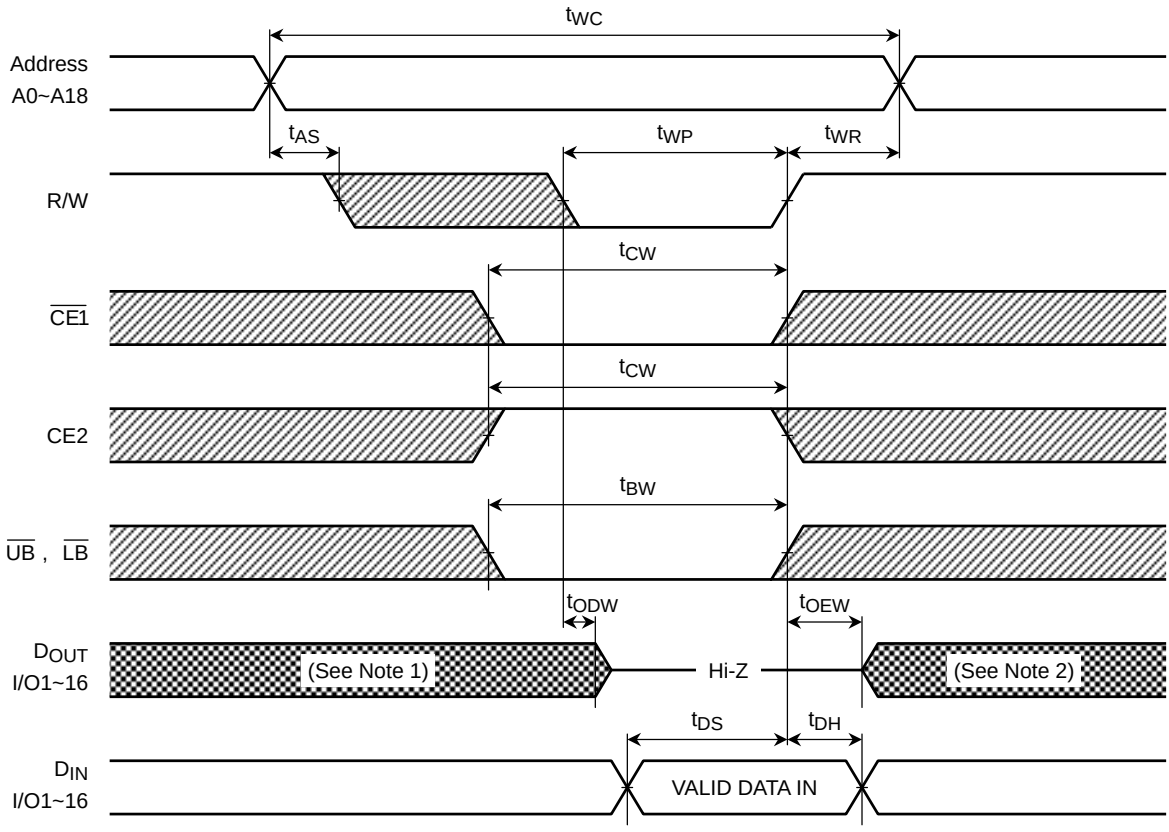


TIMING DIAGRAMS

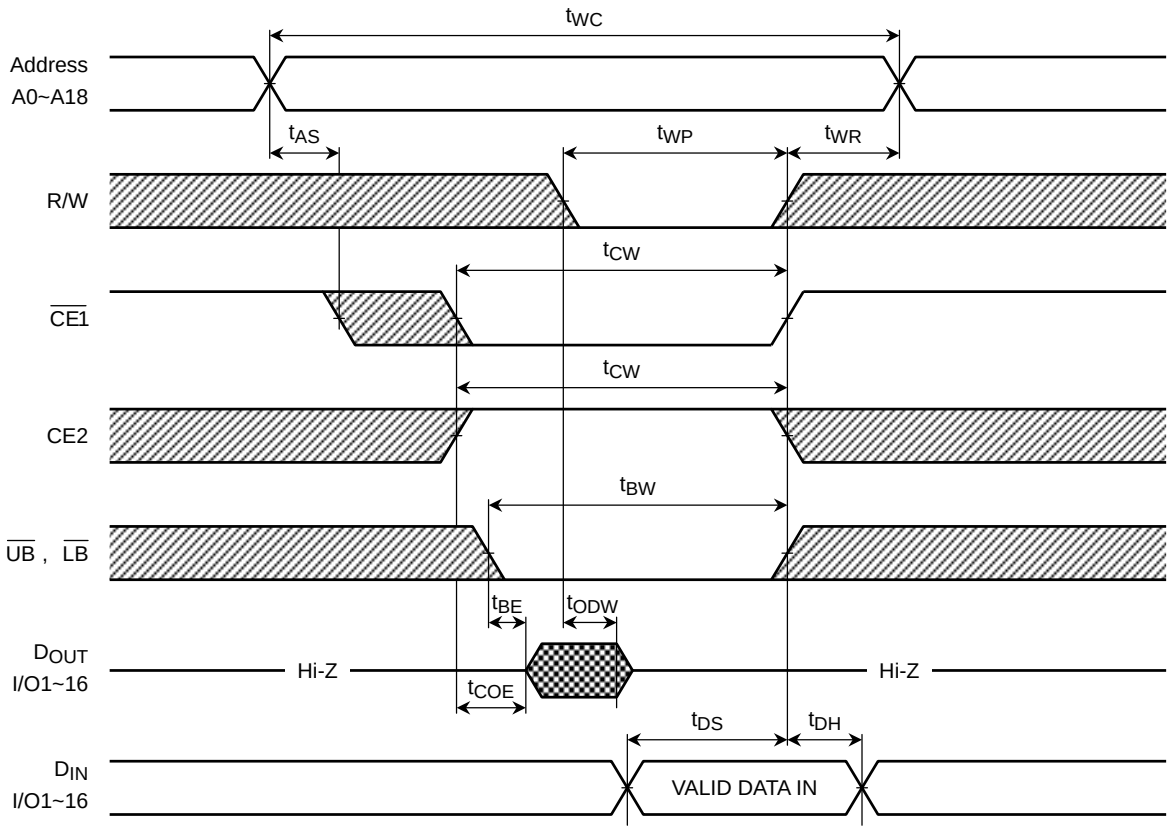
READ CYCLE



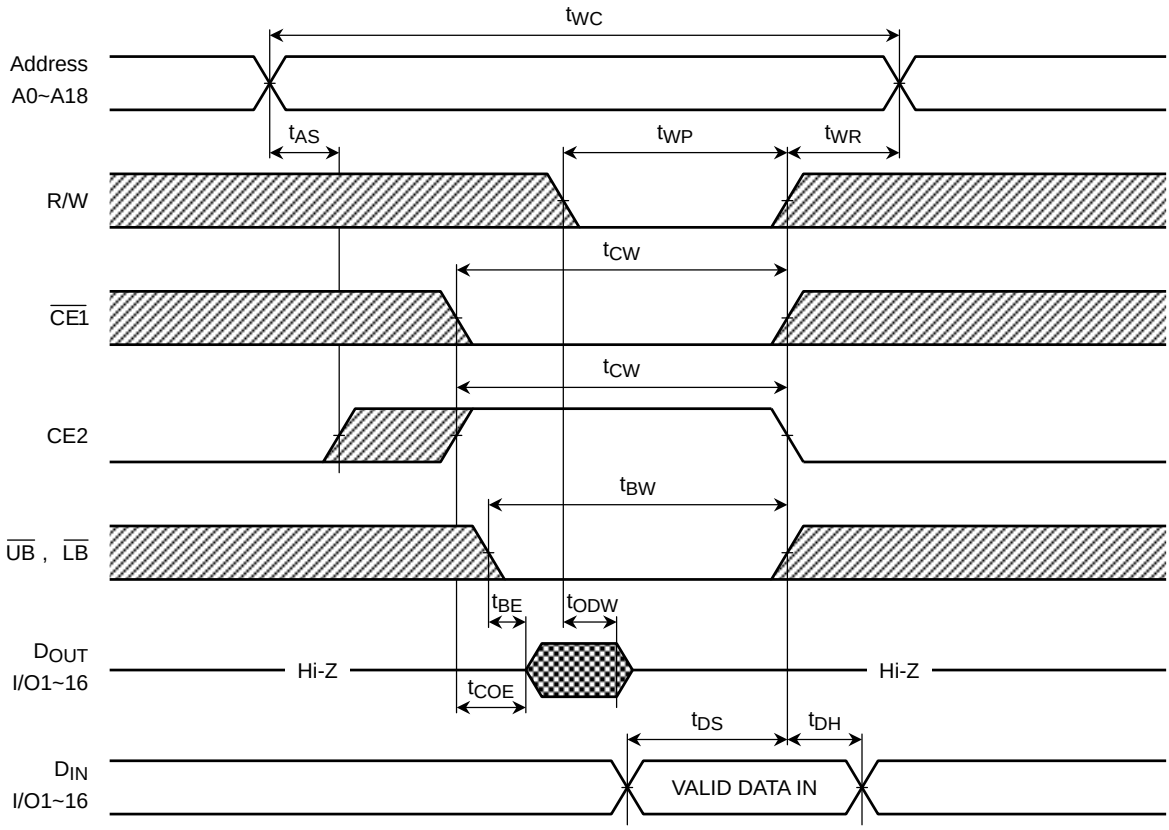
WRITE CYCLE 1 (R/W CONTROLLED)



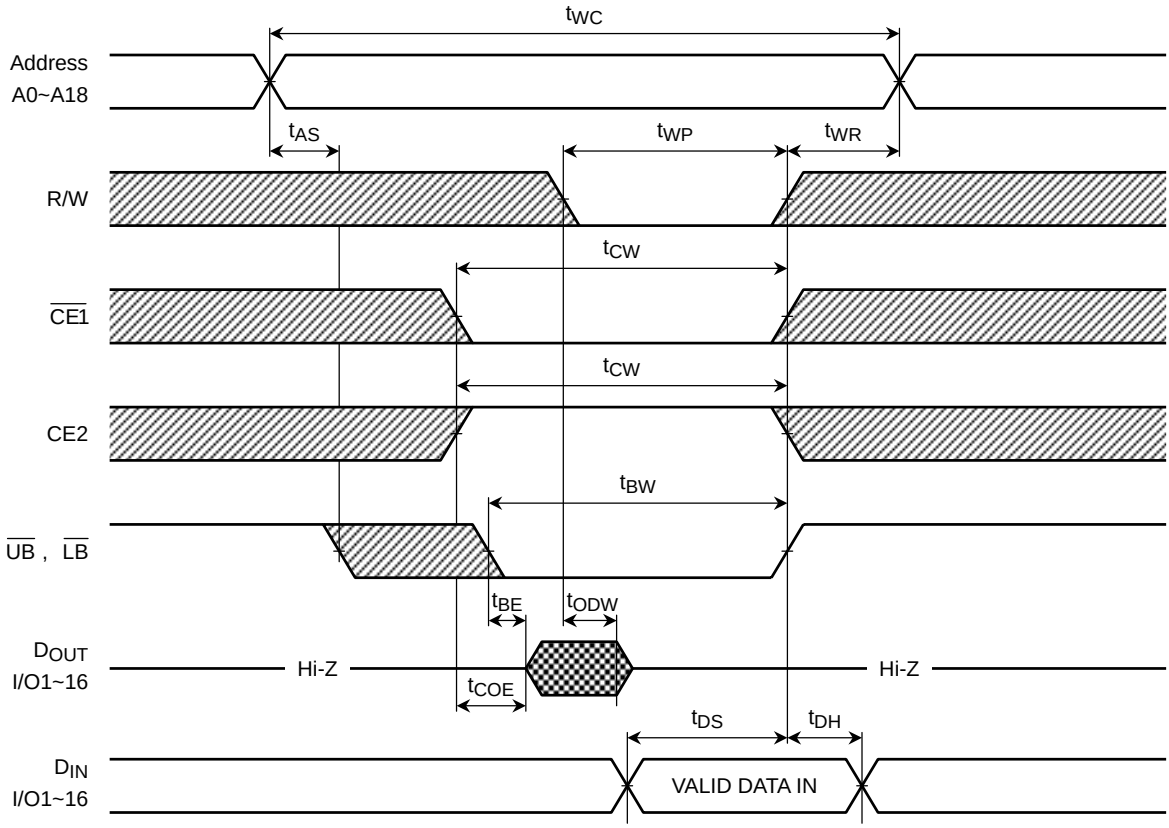
WRITE CYCLE 2 ($\overline{CE1}$ CONTROLLED)



WRITE CYCLE 3 (CE2 CONTROLLED)



WRITE CYCLE 4 ($\overline{UB}$, $\overline{LB}$ CONTROLLED)



Note:

- Read cycle

  R/W remains HIGH for the read cycle.

- Write cycle1

  (1) If $\overline{CE1}$ (or $\overline{UB}$ or $\overline{LB}$) goes LOW(or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.

  (2) If $\overline{CE1}$ (or $\overline{UB}$ or $\overline{LB}$) goes HIGH(or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

  Don't input the same polarity signal as a R/W signal into a $\overline{OE}$ during the write cycle.

- Write cycle1 to 4

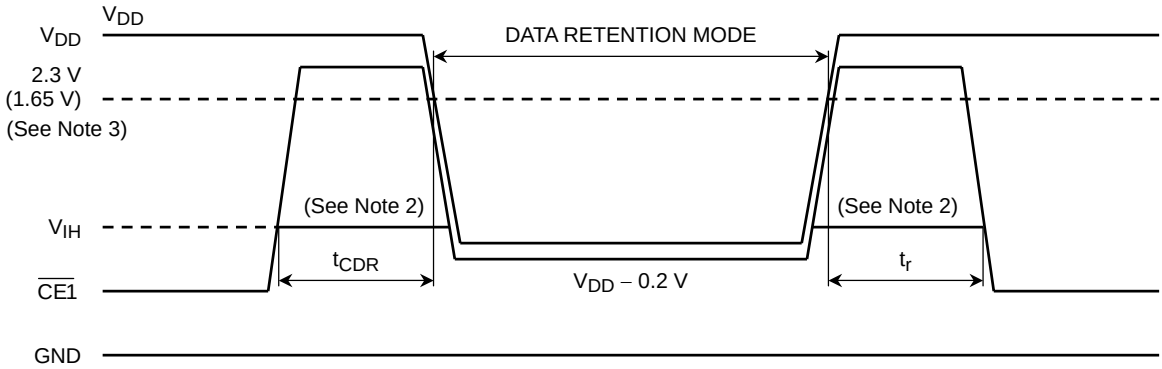
  If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

  Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

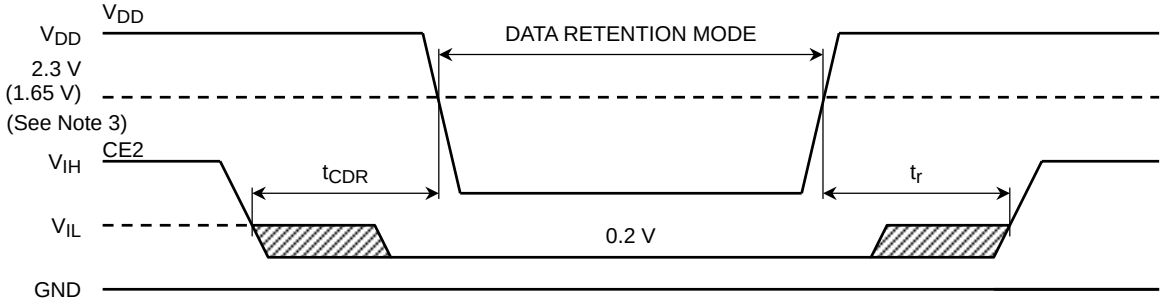
DATA RETENTION CHARACTERISTICS (Ta = –40° to 85°C)

SYMBOL	PARAMETER			TC55VCM316BTGN TC55VCM316BSGN TC55VEM316BXGN		TC55YCM316BTGN TC55YCM316BSGN TC55YEM316BXGN		UNIT
				MIN	MAX	MIN	MAX	
V_{DH}	Data Retention Supply Voltage			1.5	3.6	1.0	2.2	V
I_{DDS2}	Standby Current	V_{DH} = 3.6 V	Ta = –40~85°C	—	10	—	—	μA
		V_{DH} = 3.0 V	Ta = –40~40°C	—	2	—	—	
		V_{DH} = 2.2 V	Ta = –40~85°C	—	—	—	10	
t_{CDR}	Chip Deselect to Data Retention Mode Time			0	—	0	—	ns
t_r	Recovery Time			5	—	5	—	ms

$\overline{CE1}$ CONTROLLED DATA RETENTION MODE (See Note 1)



CE2 CONTROLLED DATA RETENTION MODE (See Note 4)



Note:

(1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is entered when CE2 ≤ 0.2 V or CE2 ≥ V_{DD} – 0.2 V.

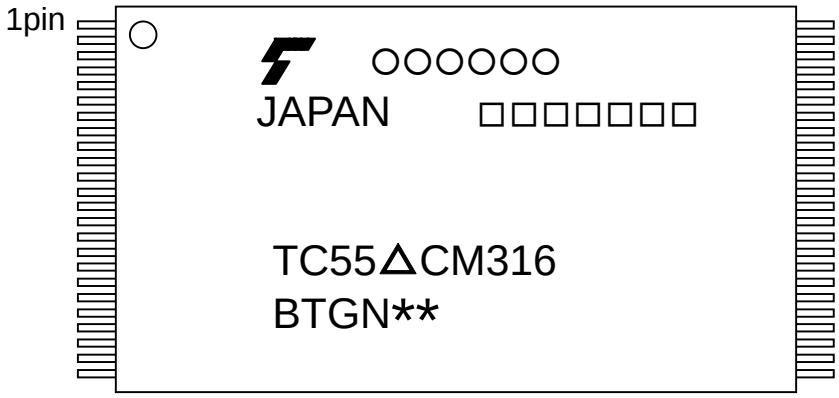
(2) When $\overline{CE1}$ is operating at the V_{IH}(min.) level, the operating current is given by I_{DDS1} during the transition of V_{DD} from 2.3(2.7) to 2.2 V(2.4 V).(TC55VCM316B, TC55VEM316B)

(3) When $\overline{CE1}$ is operating at the V_{IH}(min.) level, the operating current is given by I_{DDS1} during the transition of V_{DD} from 1.65 to 1.6 V.(TC55YCM316B, TC55YEM316B)

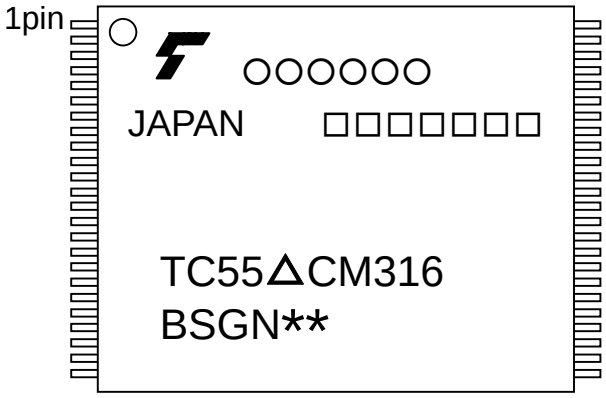
(4) In CE2 controlled data retention mode, minimum standby current mode is entered when CE2 ≤ 0.2 V.

MARKING (Example)

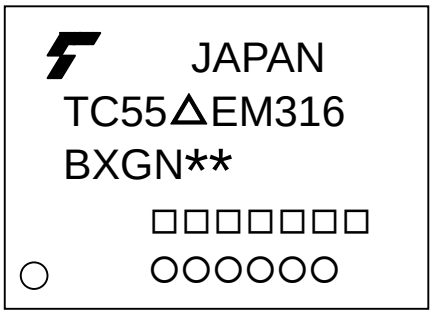
TC55VCM316BTGN/TC55YCM316BTGN Family



TC55VCM316BSGN/TC55YCM316BSGN Family



TC55VEM316BXGN/TC55YEM316BXGN Family



EXPLANATION

△ : Operating supply voltage (V:V_{DD} = 2.3 to 3.6 V, Y: V_{DD} = 1.65 to 2.2 V)

** : Speed version

○○○○○○ : Key code

□□□□□□□ : Lot code

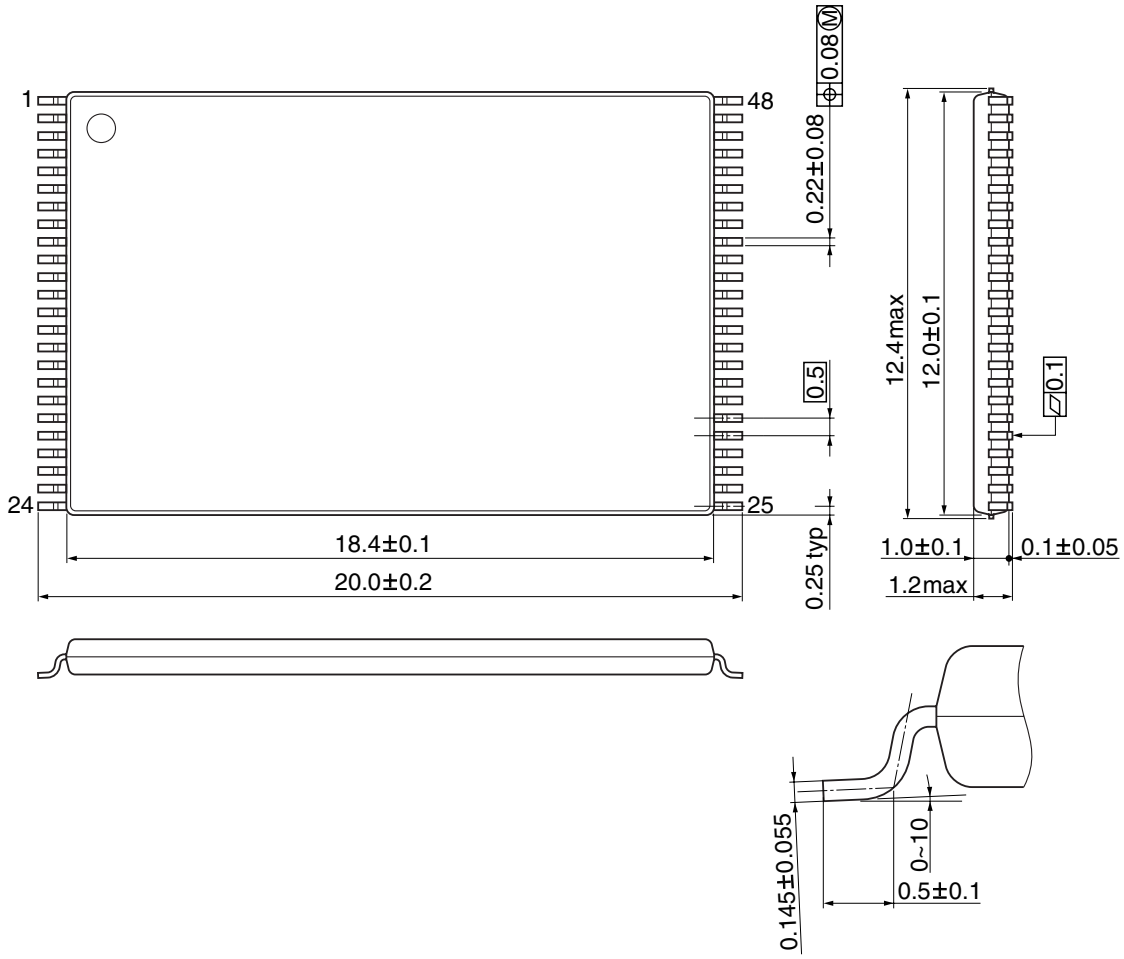
Control code

Week code

Year code

PACKAGE DIMENSIONS

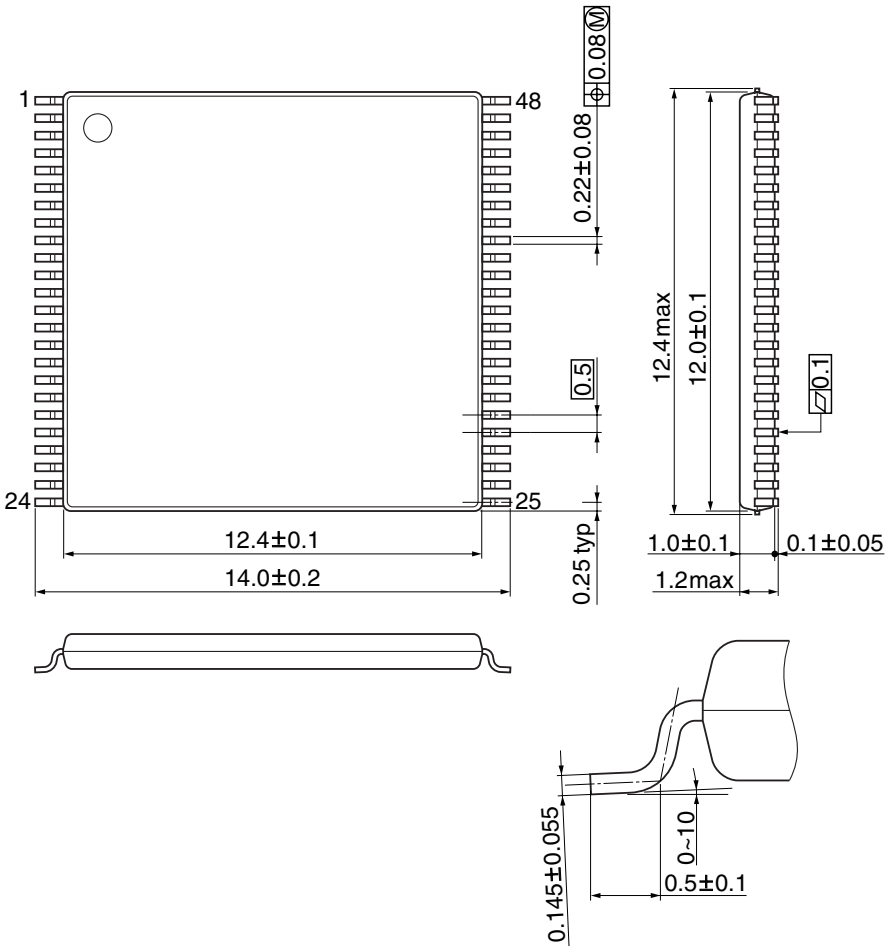
TSOP I 48-P-1220-0.50 Unit:mm



Weight:0.38 g (typ)

PACKAGE DIMENSIONS

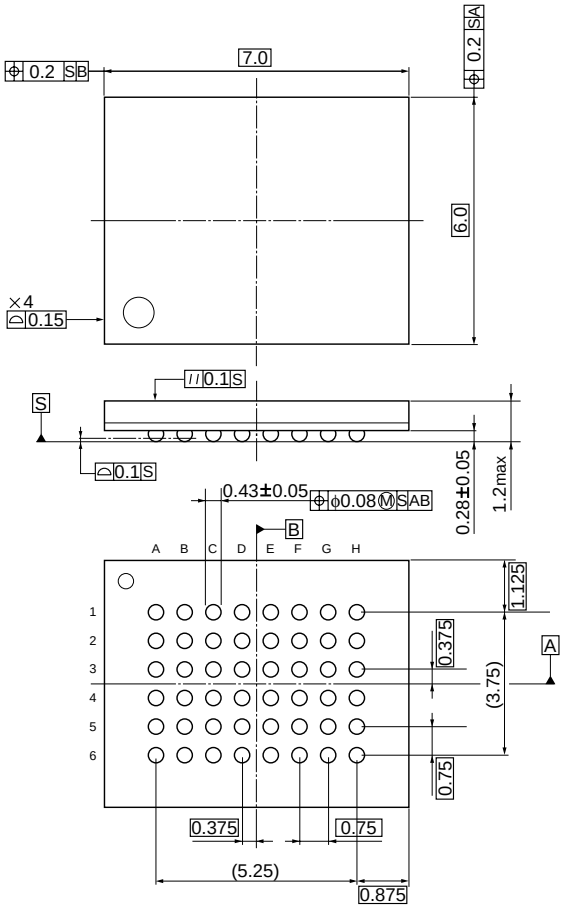
TSOP I 48-P-1214-0.50 Unit:mm



Weight:0.26 g (typ)

PACKAGE DIMENSIONS

P-TFBGA48-0607-0.75AZ Unit:mm



Weight:0.08 g (typ)

REVISION HISTORY

Draft Date	Revision Page		Type	Passage	Content
	After	Before			
V1.1a/2005-01-31	P.14,15,16	P.14,15,16		Weight	Described value of weight
V1.1b/2005-08-11	P.5,12	P.5,12		Deletion and addition of an item	Change of a I_{DDS2} temperature security definition
	P.1~18	P.1~18		Part number	Speed version change

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