CS5461

Single Phase Bi-Directional Power/Energy IC

Features

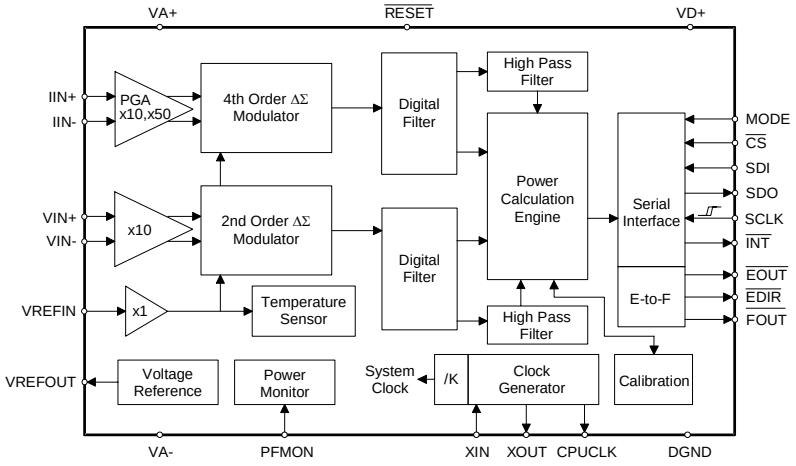
- Energy Data Linearity: ±0.1% of Reading over 1000:1 Dynamic Range
- On-Chip Functions: Energy, I ∗ V, I_{RMS} and V_{RMS}, Energy-to-Pulse Conversion
- AC/DC System Calibrations
- Meets Accuracy Spec for IEC 687/1036, JIS
- Power Consumption <12 mW
- On-Chip Temperature Sensor
- Voltage Sag Detect
- Adjustable Input Range on Current Channel
- Phase Compensation
- GND-Referenced Signals with Single Supply
- On-chip 2.5 V Reference (25 ppm/°C typ)
- Simple Three-Wire Digital Serial Interface
- Power Supply Monitor
- Interface Optimized for Shunt Sensor
- Mechanical Counter/Stepper Motor Drive
- Smart "Auto-Boot" Mode from Serial EEPROM with no microcontroller.
- Power Supply Configurations
  VA+ = +5 V; VA- = 0 V; VD+ = +3.3 V to +5 V

Description

The CS5461 is an integrated power measurement device which combines two ΔΣ ADCs, high speed power calculation functions, and a serial interface on a single chip. It is designed to accurately measure Instantaneous Current and Voltage, and calculate: Instantaneous Power, Average Power, I_{RMS}, and V_{RMS}, for single-phase 2- or 3-wire power metering applications. The CS5461 can interface to a low-cost shunt resistor or transformer for current measurement, and to a resistive divider or potential transformer for voltage measurement. The CS5461 features a bi-directional serial interface for communication with a micro-controller and a programmable energy-to-pulse output function. CS5461 has on-chip functionality to facilitate AC or DC system-level calibration. Additional features include on-chip temperature sensor, voltage sag detection, and phase compensation.

ORDERING INFORMATION:

CS5461-IS	-40°C to +85°C	24-pin SSOP



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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1. GENERAL DESCRIPTION

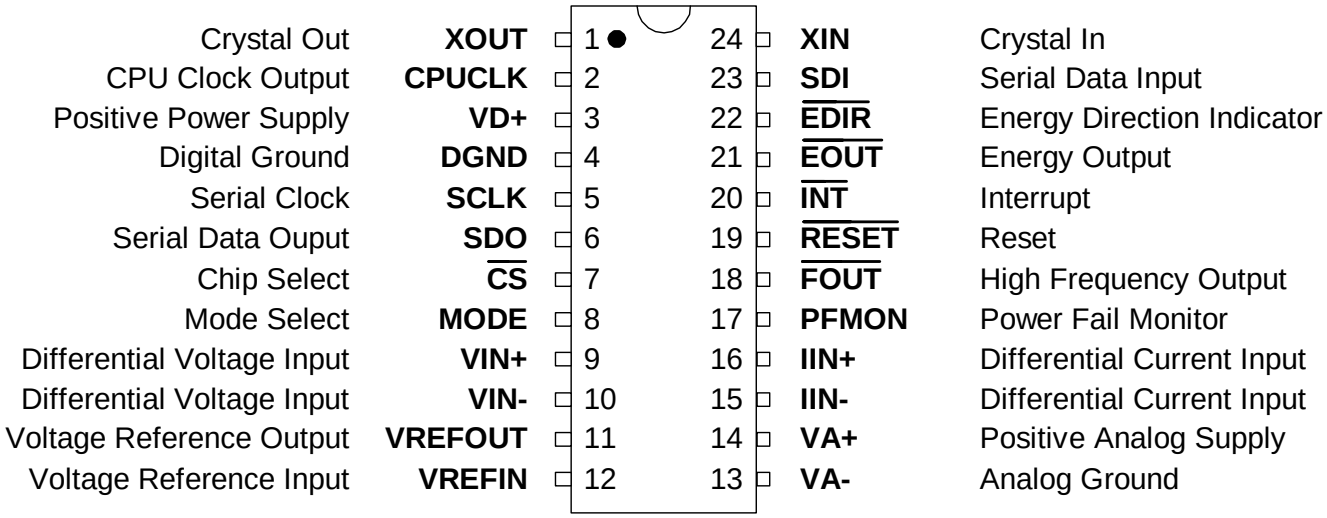
The CS5461 is a CMOS monolithic power measurement device with a real power/energy computation engine. The CS5461 combines two programmable gain amplifiers, two ΔΣ modulators, two high rate filters, system calibration, and calculation functions to provide instantaneous voltage and current data samples and to calculate average (real) power, V_{RMS}, I_{RMS}, and instantaneous power data samples.

The CS5461 functionality is optimized for power measurement applications and is optimized to interface to a shunt or current transformer for current measurement, and to a resistive divider or potential transformer for voltage measurement. To accommodate various input voltage levels from a multitude of current sensors, the CS5461's current channel has a front-end programmable gain amplifier (PGA), which allow for two available full-scale differential input signal ranges on the current channel: 100 mV_{P-P} and 500 mV_{P-P}, while the voltage channel has a set input range of 500 mV_{P-P}. With single +5 V (common-mode) supply across VA+/VA-, both of the CS5461's input channels can accommodate (common-mode + signal) levels between -0.25 V and VA+. This allows for a completely bipolar differential input configuration. The common-mode voltage level of the differential input signals can be anywhere between the supply voltage levels on the VA+/VA- pins, as long as enough voltage margin is left over so that the addition of the differential signals will not cause the total swing to go below -0.25 V or above +5 V.

The CS5461 includes two high-rate digital filters, which decimate the output from the two ΔΣ modulators. These filters integrate the output of the ΔΣ modulators for both channels to yield instantaneous voltage and current waveform output data at a (MCLK/K)/1024 output word rate (OWR).

To facilitate communication to a microcontroller, the CS5461 includes a simple three-wire serial interface which is SPI™ and Microwire™ compatible.

2. PIN DESCRIPTION



Clock Generator		
Crystal Out **Crystal In**	1,24	**XOUT, XIN** - A gate inside the chip is connected to these pins and can be used with a crystal to provide the system clock for the device. Alternatively, an external (CMOS compatible) clock can be supplied into XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** - Output of on-chip oscillator which can drive one standard CMOS load.
Control Pins and Serial Data I/O		
Serial Clock Input	5	**SCLK** - A clock signal on this pin determines the input and output rate of the data for the SDI and SDO pins respectively. This is a Schmitt Trigger input to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{CS}$ is low.
Serial Data Output	6	**SDO** -The serial data port output pin. Its output is in a high impedance state when $\overline{CS}$ is high.
Chip Select	7	**$\overline{CS}$** - When low, the port will recognize SCLK. An active high on this pin forces the SDO pin to a high impedance state.
Mode Select	8	**MODE** - When at logic high, the CS5461 will operate in auto-boot mode. For normal operation this pin must be left unconnected.
High-Frequency Energy Output	18	**$\overline{FOUT}$** - Issues active-low pulses, such that the number of pulses is proportional to the measured real energy. The energy-to-pulse ratio is programmed in the PulseRateF Register.
Reset	19	**$\overline{RESET}$** - When reset is taken low, all internal registers are set to their default states.
Interrupt	20	**$\overline{INT}$** - When $\overline{INT}$ goes low it signals that an enabled event has occurred.
Energy Output	21	**$\overline{EOUT}$** - Issues fixed-width pulses, such that the number of pulses is proportional to the real energy registration of the device. The energy-to-pulse ratio is programmed in the PulseRateE Register.
Energy Direction Indicator	22	**$\overline{EDIR}$** - Indicates if the measured energy is negative.
Serial Data Input	23	**SDI** - The serial data port input pin. Data will be input at a rate determined by SCLK.

Measurement and Reference Input		
Differential Voltage Inputs	9,10	**VIN+, VIN-** - Differential analog input pins for the voltage channel.
Differential Current Inputs	15,16	**IIN+, IIN-** - Differential analog input pins for the current channel.
Voltage Reference Output	11	**VREFOUT** - The on-chip voltage reference output. The voltage reference has a nominal magnitude of 2.5 V and is referenced to the VA- pin on the converter.
Voltage Reference Input	12	**VREFIN** - The input to this pin establishes the voltage reference for the on-chip modulator.
Power Supply Connections		
Positive Digital Supply	3	**VD+** - The positive digital supply relative to DGND.
Digital Ground	4	**DGND** - The common-mode potential of digital ground must be equal to or above the common-mode potential of VA-.
Positive Analog Supply	14	**VA+** - The positive analog supply relative to VA-.
Analog Ground	13	**VA-** - The analog ground pin must be at the lowest potential.
Power Fail Monitor	17	**PFMON** - The power fail Monitor pin monitors the analog supply. Typical threshold level (PMLO) is 2.45 V with respect to the VA- pin. If PFMON voltage threshold is tripped, the LSD (low-supply detect) bit is set in the Status Register. Once the LSD bit has been set, it cannot be reset until the PFMON voltage increases ~100 mV (typical) above the PMLO voltage.

3. CHARACTERISTICS/SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over all Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- DGND = 0 V. All voltages with respect to 0 V.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Digital Power Supply	VD	3.135	3.3	5.25	V
Positive Analog Power Supply	VA+	4.75	5	5.25	V
Negative Analog Power Supply	VA-	-0.25	0	0.25	V
Voltage Reference	VREF	-	2.5	-	V
Specified Temperature Range	T_A	-40	-	+85	°C

ANALOG CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Accuracy (Both Channels)						
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Offset Drift (Without the High Pass Filter)			-	5	-	nV/°C
Analog Inputs (Current Channel)						
Differential Input Voltage Range {(IIN+) - (IIN-)}	(Gain = 10) (Gain = 50)	IIN	0 0	- -	500 100	mV_{P-P} mV_{P-P}
Total Harmonic Distortion		THD	74	-	-	dB
Common Mode + Signal	All Gain Ranges		-0.25	-	VA+	V
Crosstalk with Voltage Channel at Full Scale	(50, 60 Hz)		-	-	-115	dB
Input Capacitance	(Gain = 10) (Gain = 50)	IC	- -	25 25	- -	pF pF
Effective Input Impedance (Note 2)	(Gain = 10) (Gain = 50)	EII	30 30	- -	- -	kΩ kΩ
Noise (Referred to Input)	(Gain = 10) (Gain = 50)	N_I	- -	- -	22.5 4.5	μV_{rms} μV_{rms}
Accuracy (Current Channel)						
Bipolar Offset Error	(Note 1)	VOS	-	-	±0.001	%F.S.
Full-Scale Error	(Note 1)	FSE	-	-	±0.001	%F.S.

Notes: 1. Applies after system calibration

2. Effective Input Impedance (EII) is determined by clock frequency (DCLK) and Input Capacitance (IC). EII = 1/(IC*DCLK/4). Note that DCLK = MCLK / K.

ANALOG CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Typ	Max	Unit
Analog Inputs (Voltage Channel)						
Differential Input Voltage Range	{(VIN+) - (VIN-)}	VIN	0	-	500	mV_{P-P}
Total Harmonic Distortion		THD	65	-	-	dB
Common Mode + Signal	All Gain Ranges		-0.25	-	VA+	V
Crosstalk with Current Channel at Full Scale	(50, 60 Hz)		-	-	-70	dB
Input Capacitance	All Gain Ranges	IC	-	0.2	-	pF
Effective Input Impedance	(Note 2)	EII	5	-	-	MΩ
Noise (Referred to Input)		N_V	-	-	250	μV_{rms}
Accuracy (Voltage Channel)						
Bipolar Offset Error	(Note 1)	VOS	-	-	±0.01	%F.S.
Full-Scale Error	(Note 1)	FSE	-	-	±0.01	%F.S.
Dynamic Characteristics						
Phase Compensation Range	(Voltage Channel, 60 Hz)		-2.8	-	+2.8	°
High Rate Filter Output Word Rate	(Both Channels)	OWR	-	DCLK/1024	-	Hz
Input Sampling Rate	DCLK = MCLK/K		-	DCLK/8	-	Hz
Full Scale DC Calibration Range	(Note 3)	FSCR	25	-	100	%F.S.
Channel-to-Channel Time-Shift Error (when PC[6:0] bits are set to “0000000”)				1.0		µs
High Pass Filter Pole Frequency	-3 dB		-	0.5	-	Hz

Notes: 3. The minimum FSCR is limited by the maximum allowed gain register value.

ANALOG CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies						
Power Supply Currents (Active State)	I_{A+}	PSCA	-	1.3	-	mA
	I_{D+} (VD+ = 5 V)	PSCD	-	2.9	-	mA
	I_{D+} (VD+ = 3.3 V)	PSCD	-	1.7	-	mA
Power Consumption (Note 5)	Active State (VD+ = 5 V)	PC	-	21	30	mW
	Active State (VD+ = 3.3 V)		-	11.6	-	mW
	Stand-By State		-	6.75	-	mW
	Sleep State		-	10	-	µW
Power Supply Rejection Ratio (Note 6) Current Channel (50, 60 Hz)	(Gain = 10)	PSRR	56	-	-	dB
	(Gain = 50)	PSRR	70	-	-	dB
Power Supply Rejection Ratio (Note 6) Voltage Channel (50, 60 Hz)	(Gain = 10)	PSRR	45	-	-	dB
PFMON Low-Voltage Trigger Threshold	(Note 7)	PMLO	2.3	2.45	-	V
PFMON High-Voltage Power-On Trip Point	(Note 8)	PMHI	-	2.55	2.7	V

Notes: 4. The minimum FSCR is limited by the maximum allowed gain register value.

5. All outputs unloaded. All inputs CMOS level.

6. Definition for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV (zero-to-peak) (60 Hz) sinewave is imposed onto the +5 V DC supply voltage at VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to VA-. Then the CS5461 is commanded to continuous conversion acquisition mode, and digital output data is collected for the channel under test. The (zero-to-peak) value of the digital sinusoidal output signal is determined, and this value is converted into the (zero-to-peak) value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as V_{eq}. PSRR is then (in dB):

$$PSRR = 20 \cdot \log\left\{\frac{150}{V_{eq}}\right\}$$

7. When voltage level on PFMON is sagging, and LSD bit is at 0, the voltage at which LSD bit is set to 1.

8. If the LSD bit has been set to 1 (because PFMON voltage fell below PMLO), this is the voltage level on PFMON at which the LSD bit can be permanently reset back to 0.

VOLTAGE REFERENCE

Parameter		Symbol	Min	Typ	Max	Unit
Reference Output						
Output Voltage		REFOUT	2.4	-	2.6	V
Temperature Coefficient	(Note 9)	TC	-	25	60	ppm/°C
Load Regulation	(Output Current 1 µA Source or Sink)	ΔV_R	-	6	10	mV
Reference Input						
Input Voltage Range		VREFIN	2.4	2.5	2.6	V
Input Capacitance			-	4	-	pF
Input CVF Current			-	25	-	nA

Notes: 9. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT Temperature Coefficient:.

$$TC_{VREF} = \left(\frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}}\right)\left(\frac{1}{T_{A}{}^{MAX} - T_{A}{}^{MIN}}\right)\left(1.0 \times 10^{6}\right)$$

5 V DIGITAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN and SCLK and $\overline{\text{RESET}}$		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and $\overline{\text{RESET}}$		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN and SCLK and $\overline{\text{RESET}}$		-	-	0.8	V
XIN		-	-	1.5	V
SCLK and $\overline{\text{RESET}}$		-	-	0.2 VD+	V
High-Level Output Voltage I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	±1	±10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

3 V DIGITAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN and SCLK and $\overline{\text{RESET}}$		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and $\overline{\text{RESET}}$		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN and SCLK and $\overline{\text{RESET}}$		-	-	0.48	V
XIN		-	-	0.3	V
SCLK and $\overline{\text{RESET}}$		-	-	0.2 VD+	V
High-Level Output Voltage I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	±1	±10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

SWITCHING CHARACTERISTICS

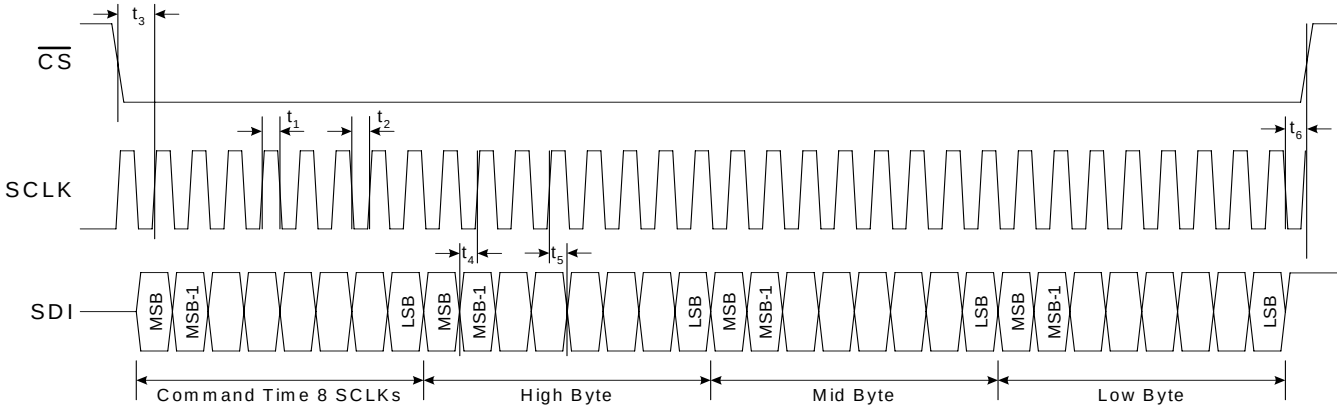
Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	Internal Gate Oscillator (Note 10)	MCLK	2.5	4.096	20	MHz
Master Clock Duty Cycle			40	-	60	%
CPUCLK Duty Cycle	(Note 11)		40		60	%
Rise Times	Any Digital Input Except SCLK	t_{rise}	-	-	1.0	µs
(Note 12)	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Fall Times	Any Digital Input Except SCLK	t_{fall}	-	-	1.0	µs
(Note 12)	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Start-up						
Oscillator Start-Up Time	XTAL = 4.096 MHz (Note 13)	t_{ost}	-	60	-	ms
Serial Port Timing						
Serial Clock Frequency		SCLK	-	-	2	MHz
Serial Clock	Pulse Width High	t_1	200	-	-	ns
	Pulse Width Low	t_2	200	-	-	ns
SDI Timing						
$\overline{CS}$ Falling to SCLK Rising		t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	100	-	-	ns
SDO Timing						
$\overline{CS}$ Falling to SDI Driving		t_7	-	20	50	ns
SCLK Falling to New Data Bit (hold time)		t_8	-	20	50	ns
$\overline{CS}$ Rising to SDO Hi-Z		t_9	-	20	50	ns
Auto-Boot Timing						
Serial Clock	Pulse Width High	t_{10}		8		MCLK
	Pulse Width Low	t_{11}		8		MCLK
MODE setup time to $\overline{RESET}$ Rising		t_{12}	50			ns
RESET rising to $\overline{CS}$ falling		t_{13}	48			MCLK
$\overline{CS}$ falling to SCLK rising		t_{14}	100	8		MCLK
SCLK falling to $\overline{CS}$ rising		t_{15}		16		MCLK
$\overline{CS}$ rising to driving MODE low (to end auto-boot sequence).		t_{16}	50			ns
SDO guaranteed setup time to SCLK rising		t_{17}	100			ns

Notes: 10. Device parameters are specified with a 4.096 MHz clock. If a crystal is used, then XIN frequency must remain between 2.5 MHz - 5.0 MHz. If an external oscillator is used, full XIN frequency range is 2.5 MHz - 20 MHz.

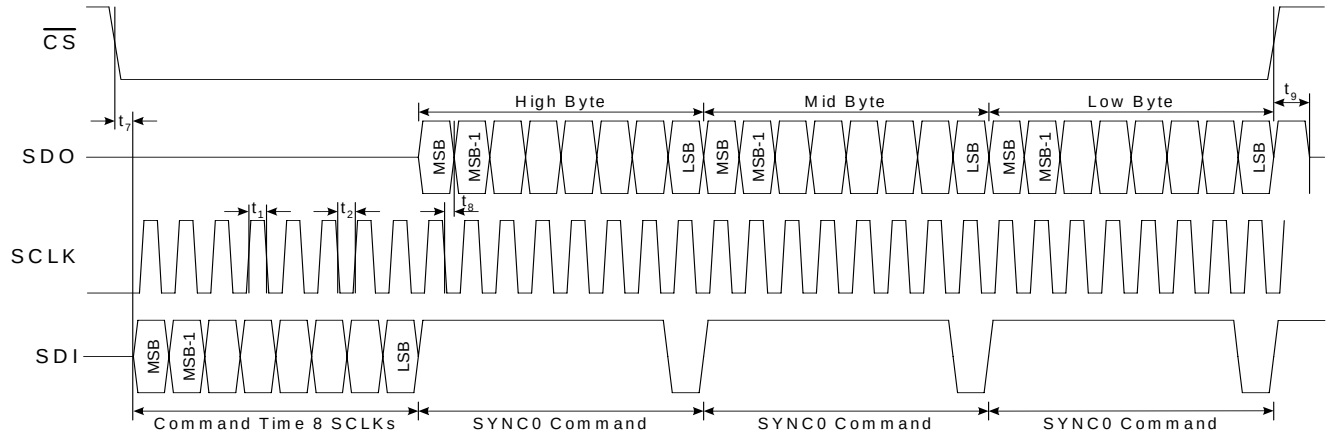
11. If external MCLK is used, then its duty cycle must be between 45% and 55% to maintain this spec.

12. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.

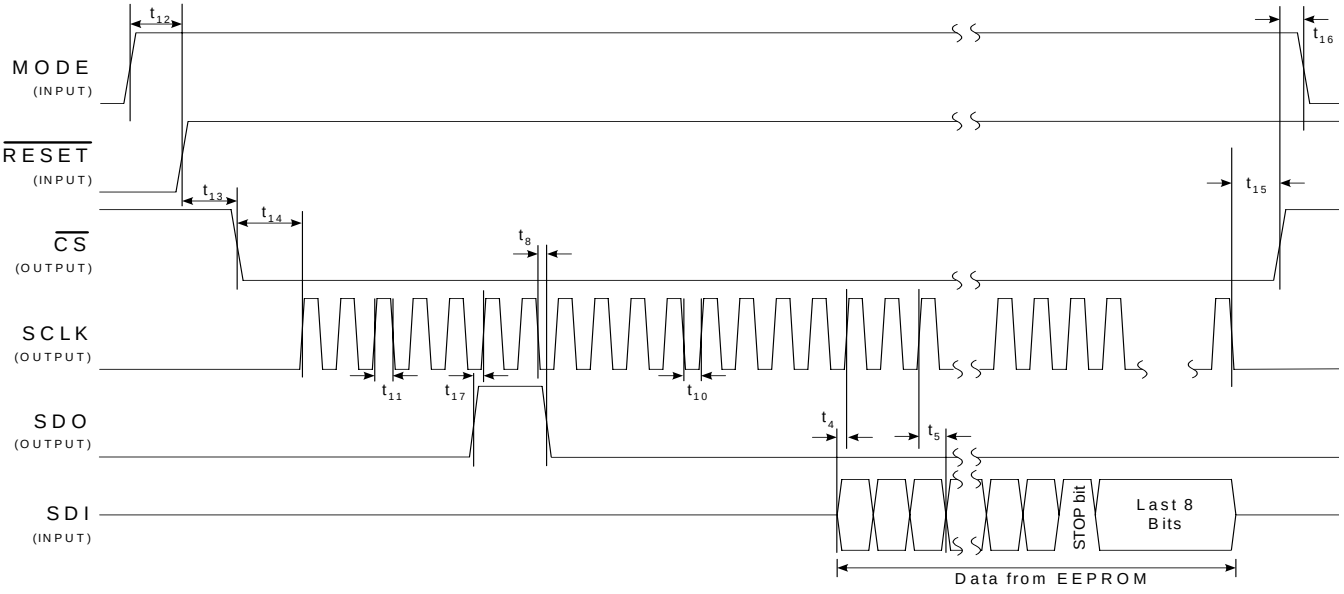
13. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.



SDI Write Timing (Not to Scale)



SDO Read Timing (Not to Scale)



Auto-Boot Sequence Timing (Not to Scale)

Figure 1. CS5461 Read and Write Timing Diagrams

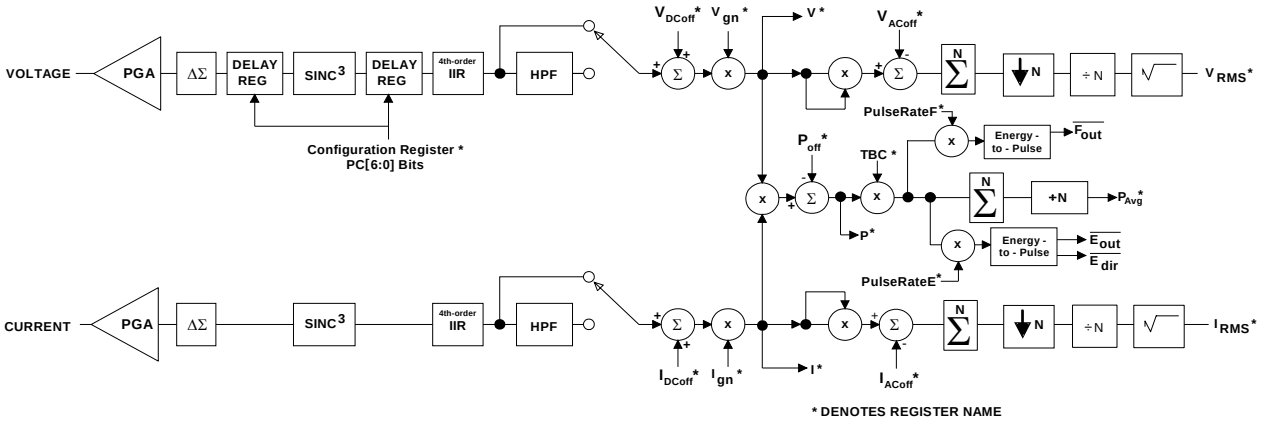


Figure 2. Data Flow.

3.1 Theory of Operation

A computational flow diagram for the two data paths is shown in Fig. 2. The analog waveforms at the voltage/current channel inputs are subject to the gains of the input PGAs. These waveforms are then sampled by the delta-sigma modulators at a rate of (MCLK/K) / 8.

3.1.1 High-Rate Digital Low-Pass Filters

The data is then low-pass filtered, to remove high-frequency noise from the modulator output. Referring to Figure 2, the high rate filters on both channels are implemented as fixed $Sinc^3$ filters.

Also note from Figure 2 that the digital data on the voltage channel is subjected to a variable time-delay filter. The delay depends on the value of the seven phase compensation bits (see *Phase Compensation*) set in the configuration register.

3.1.2 Digital Compensation Filters

The data from both channels is then passed through two 4th-order IIR "compensation" filters, whose purpose is to correct (compensate) for the magnitude roll-off of the low-pass filtering operation. These filters "re-flatten" the magnitude response of the I and V channels over the relevant frequency range, by correcting for the magnitude roll-off effects that are induced onto the I and V signal spectrums by the $Sinc^3$ low-pass filter stages.

3.1.3 Digital High-Pass Filters

Both channels provide an optional high-pass filter ("HPF" in Figure 2) which can be engaged into the signal path, in order to remove the DC content from the current/voltage signal before the RMS/energy calculations are made. These filters are activated by enabling certain bits in the Configuration Register.

3.1.4 Gain and DC Offset Adjustment

After the filtering, the instantaneous voltage and current digital codes are both subjected to value adjustments, based on the values in the DC Offset Registers (additive) and the Gain Registers (multiplicative). These registers are used for calibration of the device (see *Section 4.4, Calibration*). After offset and gain, the data is available to the user by reading the Instantaneous Voltage and Current Registers.

3.1.5 Average (Real) Power Computation

The digital instantaneous voltage and current data is then processed further. Referring to Figure 2, the instantaneous voltage/current data samples are multiplied together (one multiplication for each pair of voltage/current samples) to form instantaneous power data. The instantaneous power data is then averaged over N instantaneous conversions (N = value in Cycle Count Register) to form the result in the Average Power Register. The average power can be multiplied by the time duration of the

computation cycle, to generate a value for the accumulated real energy over the last computation cycle.

3.1.6 RMS Computations

RMS calculations are performed on the instantaneous voltage/current data and can be read from the RMS Voltage Register and the RMS Current Register. The results are computed once every computation cycle. Using N instantaneous current samples (I_n), the RMS computations for the current (and likewise for voltage, using V_n) is performed using the formula:

$$RMS = \sqrt{\frac{\sum_{n=0}^{N-1} I_n}{N}}$$

3.2 Performing Measurements

The CS5461 performs measurements of instantaneous voltage, instantaneous current, instantaneous power at an output word rate (sampling rate) of (MCLK/K) / 1024. From these instantaneous samples, average (real) power, I_{RMS}, and V_{RMS} are computed, using the most recent N instantaneous samples that were acquired. All of the measurements/results are available as a percentage of full scale. The *signed* output format is a two's complement format, and the output data words represent a normalized value between -1 and +1. The *unsigned* data in the CS5461 output registers represent normalized values between 0 and 1. A register value of 1 represents the maximum possible value. Note that a value of 1.0 is never actually obtained, the true maximum register value is [(2^23 - 1) / (2^23)] = 0.999999880791.

After each A/D conversion, the CRDY bit will be asserted in the Status Register, and the $\overline{INT}$ pin will also become active if the CRDY bit is unmasked (in the Mask Register). The assertion of the CRDY bit indicates that new instantaneous samples have been collected.

The unsigned V_{RMS}, I_{RMS}, and average power calculations are updated every N conversions (which is known as 1 "*computation cycle*") where N is the value in the Cycle Count Register. At the end of each computation cycle, the DRDY bit in the Mask Register will be set, and the $\overline{INT}$ pin will become active if the DRDY bit is unmasked.

DRDY is set only after each computation cycle has completed, whereas the CRDY bit is asserted after each individual A/D conversion. When these bits are asserted, they must be cleared by the user before they can be asserted again. If the Cycle Count Register value (N) is set to 1, all output calculations are instantaneous, and DRDY will indicate when instantaneous calculations are finished, just like the CRDY bit. For the RMS results to be valid, the Cycle-Count Register must be set to a value greater than 10.

A computation cycle is derived from the master clock and its frequency is (MCLK/K)/(1024*N). Under default conditions with a 4.096 MHz clock at XIN, instantaneous A/D conversions for voltage, current, and power are performed at a 4000 Hz rate, whereas I_{RMS}, V_{RMS}, and energy calculations are performed at a 1 Hz rate.

3.3 CS5461 Linearity Performance

	Avg Power	Vrms	Irms
Range (% of FS)	0.1% - 100%	1% - 100%	0.2% - 100%
Linearity	0.1% of reading	0.1% of reading	0.1% of reading

Table 1. Available range of ±0.1% output linearity, with default settings in the gain/offset registers.

Table 1 lists the range of input levels (as a percentage of full-scale registration in the Average Power, Irms, and Vrms Registers) over which the output linearity of the Vrms, Irms and Average Power Register measurements are guaranteed to be within ±0.1%. This linearity is guaranteed for all four of the available full-scale input voltage ranges.

Note that until the CS5461 is calibrated (see Calibration) the *accuracy* of the CS5461 (with respect to a reference line-voltage and line-current level on the power mains) is not guaranteed to within ±0.1%. But the *linearity* of any given sample of CS5461, before calibration, will be within ±0.1% of reading over the ranges specified, with respect to the input voltage levels required to cause full-scale readings in the Irms/Vrms Registers. Table 1 describes linearity + variation specs after the completion of each successive computation cycle.

The accuracy of the internal calculations can often be improved by selecting a value for the Cycle-Count Register that will cause the time duration of one computation cycle to be equal (or very close to) a whole-number of power-line cycles (and N must be greater than or equal to 4000). For example, with the cycle count set to 4200, the ±0.1% of reading linearity range for measurement of a 60 Hz sinusoidal current-sense voltage signal can be increased beyond the range of 0.2% - 70.7%. The linearity range can be increased because (4200 samples / 60 Hz) is a whole number of cycles (70).

4. FUNCTIONAL DESCRIPTION

4.1 Analog Inputs

The CS5461 has two available full-scale differential input voltage ranges on the current channel and one full-scale differential input voltage range on the voltage channel.

The input ranges are the maximum sinusoidal signals that can be applied to the current and voltage channels, yet these values will not result in full scale registration in the instantaneous current and voltage registers.

If the current and voltage channels are set to 500 mV_{P-P}, only a 250 mV_{RMS} signal will register full scale. Yet it would not be practical to inject a sinusoidal signal with a value of 250 mV_{RMS}. When such a sine wave enters the higher levels of its positive crest region (over each cycle), the voltage level of this signal exceeds the maximum differential input voltage range of the input channels. The largest sine wave voltage signal that can be placed across the inputs, with no saturation is:

$$\frac{500mV_{P-P}}{2\sqrt{2}} = \sim 176.78mV_{RMS}$$

which is ~70.7% of full-scale. So for sinusoidal inputs at the full scale peak-to-peak level the full scale registration is ~.707.

4.2 Voltage Reference

The CS5461 is specified for operation with a +2.5 V reference between the VREFIN and VA- pins. The converter includes an internal 2.5 V reference (60 ppm/°C drift) that can be used by connecting the VREFOUT pin to the VREFIN pin of the device. If higher accuracy/stability is required, an external reference can be used.

4.3 Oscillator Characteristics

XIN and XOUT are the input and output of an inverting amplifier to provide oscillation and can be configured as an on-chip oscillator, as shown in Figure 3. The oscillator circuit is designed to work with a quartz crystal or a ceramic resonator. To reduce circuit cost, two load capacitors C1 and C2 are integrated in the device. With these load capacitors, the oscillator circuit is capable of oscillation up to 20 MHz. To drive the device from an external clock source, XOUT should be left unconnected while XIN is driven by the external circuitry. There is an amplifier between XIN and the digital section which provides CMOS level signals. This amplifier works with sinusoidal inputs so there are no problems with slow edge times.

The CS5461 can be driven by an external oscillator ranging from 2.5 to 20 MHz, but the K divider value must be set such that the internal DCLK will run somewhere between 2.5 MHz and 5 MHz. The K divider value is set with the K[3:0] bits in the Configuration Register. As an example, if XIN = MCLK = 15 MHz, and K is set to 5, then DCLK is 3 MHz, which is a valid value for DCLK.

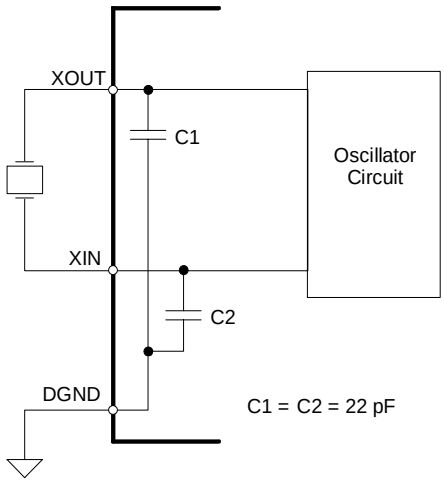


Figure 3. Oscillator Connection

4.4 Calibration

4.4.1 Overview of Calibration Process

The CS5461 offers digital calibration for both channels; AC/DC offset and AC/DC gain. For both

the voltage channel and the current channel, the AC offset calibration sequence performs an entirely different function than the DC offset calibration sequence. The AC gain and DC gain calibration sequences perform the same function, but accomplish the function using different techniques.

Since both the voltage and current channels have separate offset and gain registers associated with them, system offset or system gain can be performed on either channel without the calibration results from one channel affecting the other.

4.4.2 Calibration Sequence

1. Before Calibration the CS5461 must be operating in its *active* state, and ready to accept valid commands. The 'DRDY' bit in the Status Register should also be cleared.

2. Apply appropriate calibration signals to the inputs of the voltage/current channels (discussed next in Sections 4.4.3 and 4.4.4.)

3. Send the 8-bit calibration command to the CS5461 serial interface. Various bits within this command specify the exact type of calibration.

4. After the CS5461 finishes the desired internal calibration sequence, the DRDY bit is set in the Status Register to indicate that the calibration sequence is complete. The results of the calibration are now available in the appropriate gain/offset registers.

4.4.3 Calibration Signal Input Level

For AC/DC gain calibrations, there is an absolute limit on the RMS/DC voltage levels that are selected for the gain calibration input signals. The maximum value that the gain register can attain is 4. Therefore, for either channel, if the voltage level of a gain calibration input signal is low enough that it causes the CS5461 to attempt to set either gain register higher than 4, the gain calibration result will be invalid and all CS5461 results obtained while running A/D conversions will be invalid.

4.4.4 Calibration Signal Frequency

Optimally, the frequency of the calibration signal is the same frequency as the fundamental power line frequency of the metered power system.

4.4.5 Input Configurations for Calibrations

Figure 4 shows the basic setup for gain calibration. When performing a DC gain calibration a *positive* DC voltage level must be applied at the inputs of the voltage/current channels. This voltage should be set to the level that represents the *absolute maximum* instantaneous voltage level that needs to be measured across the inputs (including the maximum over-range level that must be accurately measured). When performing AC gain calibration, an AC reference signal should be applied that represents the desired maximum RMS level. A typical sinusoidal calibration value which allows for reasonable over-range margin would be 0.6 or 60% of the voltage/current channel's maximum input voltage level.

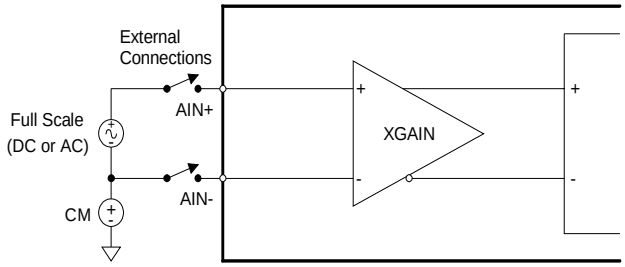


Figure 4. System Calibration of Gain.

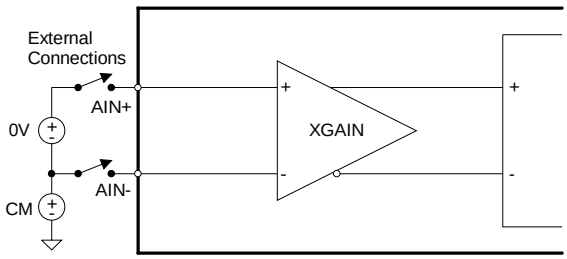


Figure 5. System Calibration of Offset.

For both AC and DC offset calibrations, the "+" and "-' pins of the voltage/current channels should

be connected to their ground reference level. (See Figure 5.)

If offset and gain calibration command bits are set, only the offset calibration will be performed.

4.4.6 Description of Calibration Algorithms

The computational flow of the CS5461's AC and DC gain/offset calibration sequences are illustrated in Figure 6. This figure applies to both the voltage channel and the current channel.

Note: For proper AC calibration, the value of the Voltage/Current Gain Registers must be set to default (1.0) before running the *gain* calibration(s), and the value in the AC Offset Registers must be set to default (0) before running calibrations. This can be accomplished by a software or hardware reset of the device. The values in the voltage/current calibration registers *do* affect the results of the calibration sequences.

4.4.6.1 AC Offset Calibration Sequence

The AC offset calibration obtains an offset value that reflects the RMS output level when the inputs are grounded. During normal operation, this AC offset register value will be subtracted from each successive voltage/current sample in order to nullify the AC offset that may be inherent in the signal path.

4.4.6.2 DC Offset Calibration Sequence

The DC Offset Registers hold the negative of the simple average of N samples taken while the DC offset calibration was executed. The inputs should be grounded during DC offset calibration. The DC offset value is added to the signal path to nullify the DC offset in the system.

4.4.6.3 AC Gain Calibration Sequence

The AC gain calibration algorithm attempts to adjust the Gain Register value such that the calibration reference signal level presented at the voltage inputs will result in a value of 0.6 in the RMS Voltage Register. The rms level of the calibration signal must be determined by the user. During AC voltage gain calibration, the value in the RMS Voltage Register is divided into 0.6 and stored in the Voltage Gain Register.

Two examples of AC calibration and the resulting shift in the digital output codes of the channel's instantaneous data registers are shown in Figures 7 and 8. Figure 8 shows that a positive (or negative) DC level signal can be used even though an AC gain calibration is being executed. However, an AC signal *cannot* be used for DC gain calibration.

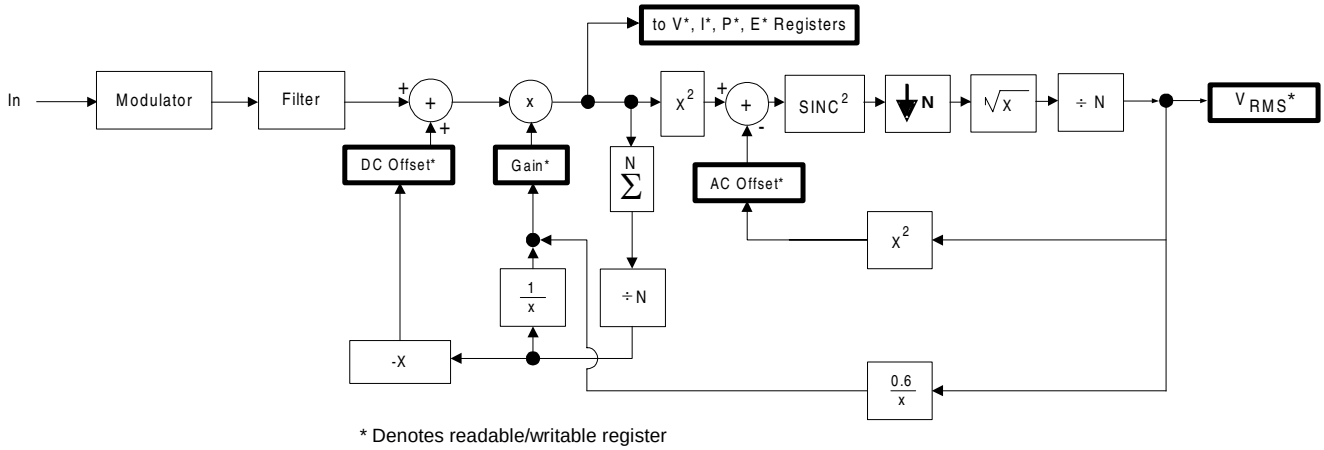


Figure 6. Calibration Data Flow

4.4.6.4 DC Gain Calibration Sequence

Based on the level of the positive DC calibration voltage applied across the "+' and "-" inputs, the CS5461 determines the DC Gain Register value by averaging the Instantaneous Register's output signal values over one computation cycle (N samples) and then dividing this average into 1. Therefore, after the DC gain calibration, the Instantaneous Register will read at full-scale whenever the DC level of the input signal is equal to the level of the DC calibration signal applied to the inputs during the DC gain calibration (see Figure 9).

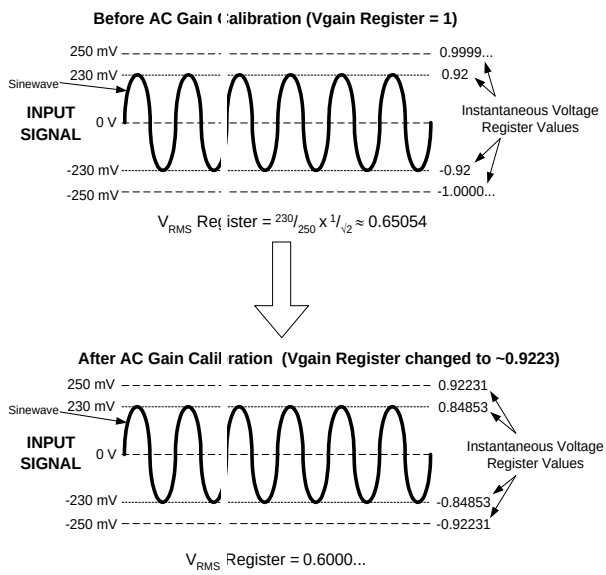


Figure 7. Example of AC Gain Calibration

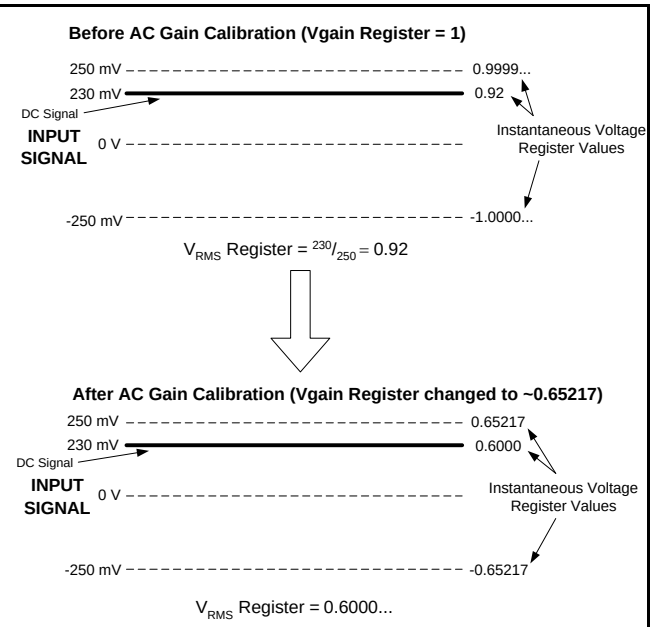


Figure 8. Another Example of AC Gain Calibration

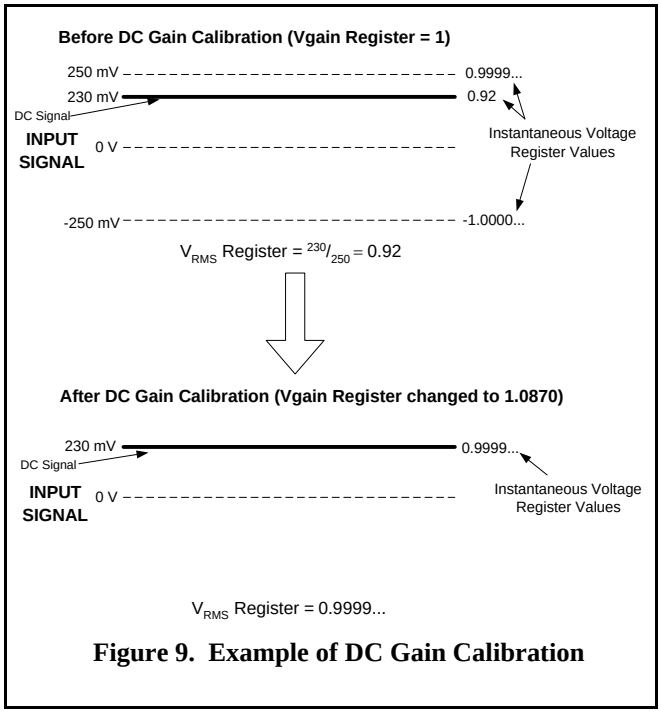


Figure 9. Example of DC Gain Calibration

4.4.7 Duration of Calibration Sequence

The value of the Cycle Count Register (N) determines the number of conversions performed by the CS5461 during a given calibration sequence. For DC offset/gain calibrations, the calibration sequence takes at least N + 30 conversion cycles to complete. For AC offset/gain calibrations, the calibration sequence takes at least 6N + 30 A/D conversion cycles to complete, (about 6 computation cycles). As N is increased, the accuracy of calibration results will increase.

4.4.8 Order of Calibration Sequences

1. If the measured signal needs to include any DC content that may be present in the voltage/current and power/energy signals, run DC offset calibration first. However, if the HPF options are turned on, then any DC component that may be present in

the power/energy signals will be removed from the CS5461's power/energy results.

2. If the energy registration accuracy needs to be within ±0.1% (with respect to reference calibration levels on the voltage/current inputs) then either the AC or the DC gain calibration is recommended for the voltage/current channels.

3. Finally, run AC offset calibration on the voltage and current channels.

4.5 Power Offset

The Power Offset Register can be used to offset system power sources that may be resident in the system, but do not originate from the power line signal. These sources of extra energy in the system contribute undesirable and false offsets to the power/energy measurement results. After determining the amount of stray power, the Power Offset Register can be set to nullify the effects of this unwanted energy.

4.6 Phase Compensation

Bits 23 to 17 of the Configuration Register are used to program the amount of phase delay added to the voltage channel signal path. This phase delay is applied to the voltage channel signal in order to compensate for phase delay that may be introduced by the voltage and current sensor circuitry external to the CS5461. Voltage and current transformers, as well as other sensor equipment applied to the front-end of the CS5461 inputs can often introduce a phase delay in the system, which distorts the phase relationship between the voltage and current signals being measured. The phase compensation bits PC[6:0] can be set to nullify this undesirable phase distortion between the two channels.

The default value of the phase compensation bits is 0000000(b). This setting represents the shortest time-delay (smallest phase delay) between the voltage and current channel signal paths. With the default setting, the phase delay on the voltage channel is 0.995 µs (~0.0215 degrees assuming a 60 Hz power signal). With MCLK = 4.096 MHz and K = 1, the range of the internal phase compensation ranges from -2.8 degrees to +2.8 degrees when the input voltage/current signals are at 60 Hz. In this condition, each step of the phase compensation register (value of one LSB) is ~0.04 degrees. For values of MCLK other than 4.096 MHz, the range (-2.8 to +2.8 degrees) and step size (0.04 degrees) should be scaled by 4.096 MHz / (MCLK / K). For power line frequencies other than 60 Hz, the values of the range and step size of the PC[6:0] bits can be determined by converting the above values to time-domain (seconds), and then computing the new range and step size (in degrees) with respect to the new line frequency.

To calibrate the phase delay, use a purely resistive load and adjust the phase compensation bits until the Average Power Register value is maximized.

4.7 Time-Base Calibration

The Time-Base Calibration Register (notated as "TBC" in Figure 2) is used to compensate for slight errors in the XIN frequency. External oscillators and crystals have certain tolerances. To improve the accuracy of the clock for energy measurements, the Time-Base Calibration Register can be manipulated to compensate for the frequency error. Note from Figure 2 that the TBC Register only affects the value in the Average Power Register.

As an example, if the desired XIN frequency is 4.096 MHz, but during production-level testing the average frequency of the crystal on a particular board is measured to be 4.091 MHz. The ratio of the desired frequency to the actual frequency is 4.096 MHz / 4.091 MHz = ~1.00122219506. The Time-Base Calibration Register can be set to 1.00122213364 = 0x80280C(h), which is close to the desired ratio.

4.8 On-Chip Temperature Sensor

After a few minutes of normal-active operation in 'continuous conversions' data acquisition mode, the CS5461 will stabilize to a constant steady-state operating temperature. However, the CS5461's operating temperature may be influenced by changes in the ambient temperature. Such ambient temperature fluctuations will cause some drift in the gain of the CS5461's two A/D converters. The on-chip temperature sensor provides the option to calibrate such drift.

The output code value in the Temperature Register is the relative temperature reading of the on-chip temperature sensor.

By recording the digitized temperature readings and comparing these readings to the fluctuations in the A/D output codes of the Vrms and Irms Register readings, the fluctuation of the A/D converter can be characterized over a wide range of ambient temperatures.

Once a temperature drift characterization of the device has been performed, a temperature compensation algorithm can be integrated into the firmware within the on-board MCU to compensate for this temperature drift.

4.9 Interrupt

The $\overline{\text{INT}}$ pin is used to indicate that an event has taken place in the converter that needs attention. These events inform the system about operation conditions and internal error conditions. The $\overline{\text{INT}}$ signal is created by combining the Status Register with the Mask Register. Whenever a bit in the Status Register becomes active, and the corresponding bit in the Mask Register is a logic 1, the $\overline{\text{INT}}$ signal becomes active. The interrupt condition is cleared when the bits of the Status Register are returned to their inactive state.

4.9.1 Typical use of the $\overline{\text{INT}}$ pin

The steps below show how interrupts can be handled.

- *Initialization*:

  Step I0 - All Status bits are cleared by writing FFFFFF (Hex) into the Status Register.

  Step I1 - The conditional bits which will be used to generate interrupts are then set to logic 1 in the Mask Register.

  Step I3 - Enable interrupts.

- *Interrupt Handler Routine*:

  Step H0 - Read the Status Register.

  Step H1 - Disable all interrupts.

  Step H2 - Branch to the proper interrupt service routine.

  Step H3 - Clear the Status Register by writing back the read value in step H0.

  Step H4 - Re-enable interrupts.

  Step H5 - Return from interrupt service routine.

  This handshaking procedure insures that any new interrupts activated between steps H0 and H3 are not lost (cleared) by step H3.

4.9.2 $\overline{\text{INT}}$ Active State

The behavior of the $\overline{\text{INT}}$ pin is controlled by the IMODE and IINV bits of the Configuration Register. The pin can be active low (default), active high, active on a return to logic 0 (pulse-low), or active on a return to logic 1 (pulse-high). If the interrupt output signal format is set for either pulse-high or pulse-low, the duration of the $\overline{\text{INT}}$ pulse will be at least one DCLK cycle (DCLK = MCLK / K).

4.10 Voltage Sag-Detect Feature

The CS5461 includes Status Register bit, VSAG; which indicates a sag in the power line voltage.

In order for sag condition to be identified, the measured V_{RMS} must remain below a set sag threshold level for a specified period of time.

To activate this feature, a voltage threshold value must be specified in the Voltage Sag Level Register ($VSAG_{Level}$); and a time-duration must be specified in the Voltage Sag Duration Register ($VSAG_{Duration}$). This Time Duration is specified in terms of A/D cycles.

If V_{RMS} is measured below the level specified in the $VSAG_{Level}$ Register for a duration of time greater than or equal to the number of A/D conversions specified in the $VSAG_{Duration}$ Register, then the VSAG bit in the Status Register will be asserted.

5. ENERGY PULSE OUTPUTS

5.1 Pulse-Rate Output ($\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$)

$\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins provide pulses which represent a predetermined magnitude of energy. With MCLK = 4.096 MHz, and default settings, the pulses will have an average frequency equal to the frequency setting in the PulseRateE Register when the input signals into the voltage and current channels cause full-scale readings in the Instantaneous Voltage and Current Registers. When MCLK/K is not equal to 4.096 MHz, the user should scale the pulse-rate by a factor of 4.096 MHz / (MCLK / K) to get the actual output pulse-rate.

5.2 Pulse Output for Normal Format, Stepper Motor Format and Mechanical Counter Format

$\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins can be set in three different output formats. The default setting is *normal* output pulse format. When the pulse is set to either of the other two formats, the time duration and/or the relative timing of the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pulses is varied such that the pulses can drive either an electro-mechanical counter or a stepper motor. The ability to set the pulse output format to one of the three available formats is controlled by setting certain bits in the Control Register.

5.2.1 Normal Format

In Normal format the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pulse output format is illustrated in Figure 10. These are *active-low* pulses of short duration. A positive energy pulse is represented by a pulse on the $\overline{\text{EOUT}}$ pin while the $\overline{\text{EDIR}}$ will remain high. A negative energy pulse is represented by synchronous pulses on both the $\overline{\text{EOUT}}$ pin and the $\overline{\text{EDIR}}$ pin.

The pulse duration is an integer multiple of MCLK cycles, approximately equal to 1/16 of the period of the contents of the Pulse-Rate Register. However for Pulse-Rate Register settings less than the sampling rate (which is [MCLK/8]/1024), the pulse duration remains constant and is equal to the duration of the pulses when the Pulse-Rate Register is set to [MCLK/K]/1024. The maximum pulse frequency from the $\overline{\text{EOUT}}$ pin is therefore [MCLK / K] / 8. When DCLK is not equal to 4.096 MHz, the pulse duration can be predicted by using the pulse duration values in Table RR and dividing them by (MCLK/K) / 4.096 MHz.

In Normal pulse output format, the number of pulses depends on the value of the PulseRateE Register and on the amount of energy registered over the most recent A/D sampling period. A running total of the energy accumulation is maintained in an internal register inside the CS5461 (not available to the user). After each A/D conversion cycle, the result in the Power Register is multiplied by the value in the PulseRateE Register, and also by the value in the TBC (Time-Base Calibration) Register, and then added to this internal energy accumulation register. Once a certain amount of positive or neg-

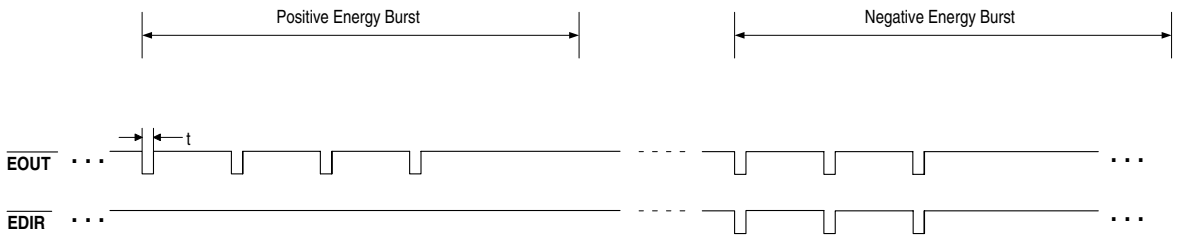


Figure 10. Time-plot representation of pulse output for a typical burst of pulses (Normal Format)

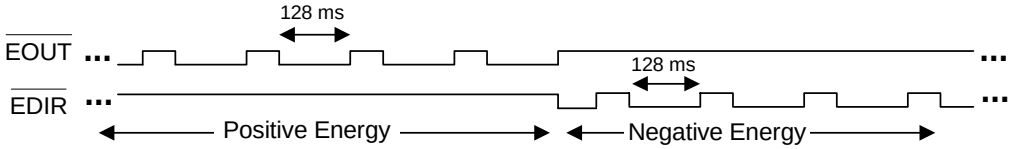


Figure 11. Mechanical Counter Format on $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$

ative energy accumulation is reached in this register, the CS5461 will issue either a positive or negative energy pulse on the $\overline{\text{EOUT}}$/$\overline{\text{EDIR}}$ pins. After the pulse or pulses are issued, a certain residual amount of energy may be left over in this internal energy accumulation register. In this situation, the residual energy is not lost or discarded, but rather it is maintained and added to the energy that is accumulated during the next update period.

5.2.2 Mechanical Counter Format

Setting the MECH bit in the Control Register to '1' and the STEP bit to '0' enables wide-stepping pulses for mechanical counters and similar discrete counter instruments. In default mechanical mode format, active-low pulses are 128 ms wide when using a 4.096 MHz crystal and K = 1. When energy is positive, the pulses appear on $\overline{\text{EOUT}}$. When energy is negative, pulses appear on $\overline{\text{EDIR}}$ (see Figure 11). The pulse width is set in the Pulsewidth register and will limit the pulse frequency available. It is up to the user to insure that pulses will not occur at a rate faster than the 128 ms pulse duration, or faster than the mechanical counter can accommodate. This is done by verifying that the PulseRateE Register is set to an appropriate value. Because in the default state the duration of each pulse is set to 128 ms, the maximum output pulse frequency is limited to ~7.8 Hz (for MCLK/K = 4.096 MHz). For values of MCLK/K different than 4.096 MHz, the duration of one pulse is (128*4.096 MHz)/(MCLK/K) milliseconds.

5.2.3 Stepper Motor Format

Setting the STEP bit in the Control Register to '1' and the MECH bit to '0' transforms the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins into two-phase stepper motor outputs. When an energy pulse occurs, one of the outputs changes state. When the next energy pulse occurs, the other output changes state. The direction the motor will rotate is determined by the order of the state changes. When energy is positive, $\overline{\text{EOUT}}$ will lead $\overline{\text{EDIR}}$. When energy is negative, $\overline{\text{EDIR}}$ will lead $\overline{\text{EOUT}}$ (see Figure 12).

5.3 $\overline{\text{FOUT}}$ Pulse Output

In many metering applications, the pulse frequency to power rate on the $\overline{\text{EOUT}}$ pin may be set to a relatively low value, such that the pulse frequency is on the order of 1-100 Hz at nominal power consumption levels. However, calibration can take a long time at such output frequencies. In order to reduce the time needed to verify the meter an extra pulse frequency-to-power output is provided on the $\overline{\text{FOUT}}$ pin. The pulse frequency-to-power rate can

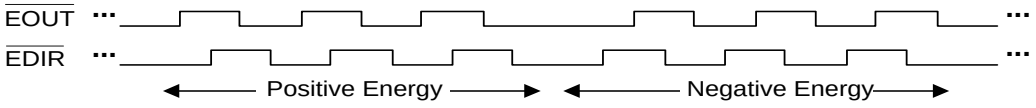


Figure 12. Stepper Motor Format on $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$

be set to a value much higher than the $\overline{EOUT}$ pulse rate.

The $\overline{FOUT}$ pin outputs negative and positive energy, but has no energy direction indicator. The maximum $\overline{FOUT}$ pulse frequency is set by the value in the PulseRateF Register.

5.4 Anti-Creep for the Pulse Outputs

Anti-Creep can be enabled/disabled for both $\overline{EOUT}$/$\overline{EDIR}$ and $\overline{FOUT}$ pulse output systems in the Control Register. Anti-creep allows the electronic meter to maintain a "buffer" energy band, defined by positive/negative energy threshold levels, such that when the magnitude of the accumulated energy is below this level, no energy pulses are issued. The anti-creep feature is especially useful when the meter demands that the energy pulse outputs are set to relatively high frequency. A higher frequency pulse rate means that less energy registration is required to generate a pulse; and so it is more likely that random noise present in the power line and/or current-sense circuit can generate a pulse that does not represent billable energy.

5.5 Design Examples

EXAMPLE #1: For a power line with maximum rated levels of 250 V (RMS) and 20 A (RMS), the pulse-frequency on the $\overline{EOUT}$ pin needs to be 'IR' = 100 pulses-per-second (100 Hz) when the RMS-voltage and RMS-current levels on the power line are 220 V and 15 A respectively. To meet this requirement, the pulse-rate frequency ('PR') in the Pulse-Rate Register must be set accordingly.

After calibration, the first step to finding the value of 'PR' is to set the voltage and current sensor gain constants, K_V and K_I, such that there will be acceptable voltage levels on the CS5461 inputs when the power line voltage and current levels are at the maximum values of 250 V and 20 A. K_V and K_I are needed to determine the appropriate ratios of the voltage/current transformers and/or shunt resistor values to use in the front-end voltage/current sensor networks.

For a sinewave, the largest RMS value that can be accurately measured (without over-driving the inputs) will register ~0.707 of the maximum DC input level. Since power signals are often not perfectly sinusoidal in real-world situations, and to provide for some over-range capability, the RMS Voltage Register and RMS Current Register is set to measure 0.6 when the RMS-values of the line-voltage and line-current levels are 250 V and 20 A. Therefore, when the RMS registers measure 0.6, the voltage level at the inputs will be 0.6 x 250 mV = 150 mV. The sensor gain constants, K_V and K_I, are determined by demanding that the voltage and current channel inputs should be 150 mV RMS when the power line voltage and current are at the maximum values of 250 V and 20 A.

K_V = 150 mV / 250 V = 0.0006

K_I = 150 mV / 20 A = 0.0075 Ω

These sensor gain constants are used to calculate what the input voltage levels will be on the CS5461 inputs when the line-voltage and line-current are 220 V and 15 A. These values are V_{Vnom} and V_{Inom}.

$V_{Vnom} = K_V * 220\ V = 132\ mV$

$V_{Inom} = K_I * 15\ A = 112.5\ mV$

The pulse rate on $\overline{EOUT}$ will be at 'PR' pulses per second (Hz) when the RMS-levels of voltage/current inputs are at 250 mV. When the voltage/current inputs are set at V_{Vnom} and V_{Inom}, the pulse rate needs to be 'IR' = 100 pulses per second. IR will be some percentage of PR. The percentage is defined by the ratios of V_{Vnom}/250 mV and V_{Inom}/250 mV with the following formula:

$$PulseRate = IR = PR \cdot \frac{V_{Vnom}}{250mV} \cdot \frac{V_{Inom}}{250mV}$$

From this equation the value of 'PR' is shown as:

$$PR = \frac{IR}{\frac{V_{Vnom}}{250mV} \times \frac{V_{Inom}}{250mV}} = \frac{100Hz}{\frac{132mV}{250mV} \times \frac{112.5mV}{250mV}}$$

Therefore the Pulse-Rate Register is set to ~420.875 Hz, or 0x00349C.

EXAMPLE #2: The required number of pulses per unit energy present at EOUT is specified to be 500 pulses/kW-hr; given that the maximum line-voltage is 250 V (RMS) and the maximum line-current is 20 A (RMS). In such a situation, the nominal line voltage and current do not determine the appropriate pulse-rate setting. Instead, the maximum line levels must be considered. As before, the given maximum line-voltage and line-current levels are used to determine K_V and K_I:

K_V = 150 mV / 250 V = 0.0006

K_I = 150 mV / 20 A = 0.0075 Ω

Again the sensor gains are calculated such that the maximum line-voltage and line-current levels will measure as 0.6 in the RMS Voltage Register and RMS Current Register.

With voltage and current channel input ranges set to 10x, the required Pulse-Rate Register setting is determined using the following equation:

$$PR = 500\frac{pulses}{kW \cdot hr} \cdot \frac{1hr}{3600s} \cdot \frac{1kW}{1000W} \cdot \frac{250mV}{K_V} \cdot \frac{250mV}{K_I}$$

Therefore PR = ~1.929 Hz.

Note that the Pulse-Rate Register cannot be set to a frequency of exactly 1.929 Hz. The closest setting that the Pulse-Rate Register can obtain is 0x00003E = 1.9375 Hz. To improve the accuracy, either gain register can be programmed to correct for the round-off error in PR. This value would be calculated as

$$Ign \text{ or } Vgn = \frac{PR}{1.929} \cong 1.00441 = 0x404830$$

When MCLK/K is not equal to 4.096 MHz, the result for 'PR' that is calculated for the Pulse-Rate Register must be scaled by a correction factor of: 4.096 MHz / (MCLK/K). For MCLK/K of 3.05856 MHz the result is scaled by 4.096/3.05856 to get a final PR result of ~2.583 Hz.

5.6 Auto-Boot Mode Using EEPROM

When the CS5461 MODE pin is left unconnected, the CS5461 is in normal operating mode, called *host mode*. When this pin is set to logic high, the CS5461 *auto-boot mode* is enabled. In auto-boot mode, the CS5461 is configured to request a memory download from an external serial EEPROM. Auto-Boot mode allows the CS5461 to operate without the need for a microcontroller.

5.6.1 Auto-Boot Configuration

Figure 13 shows the typical connections between the CS5461 and a serial EEPROM for proper auto-boot operation. In this mode, $\overline{CS}$ and SCLK are driven outputs. During the auto-boot sequence, the CS5461 drives $\overline{CS}$ low, provides a clock output on SCLK, and drives out-commands on SDO. It receives the EEPROM data on SDI. The serial EEPROM must be programmed with the user-specified commands and register data that will be used by the CS5461 to change any of the default register values and begin conversions.

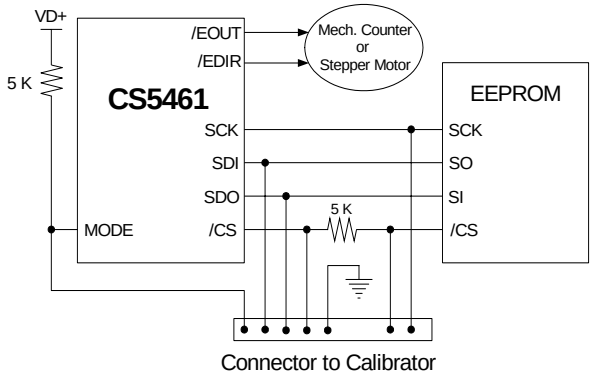


Figure 13. Typical Interface of EEPROM to CS5461

Figure 13 also shows the external connections that would be made to a calibrator device, such as a PC or custom calibration board. When the metering system is installed, the calibrator would be used to control calibration and/or to program user-specified commands and calibration values into the EEPROM. The user-specified commands/data will determine the CS5461's exact operation, when the auto-boot initialization sequence is running. Any of the valid commands can be used.

5.6.2 Auto-Boot Data for EEPROM

Below is an example code set for an auto-boot sequence. This code is written into the EEPROM by the user. The serial data for such a sequence is shown below in single-byte hexidecimal notation:

40 00 00 61	;In Configuration Register, turn high-pass filters on, set K=1.
44 7F C4 A9	;Write value of 0x7FC4A9 to Current Gain Register.
46 7F B2 53	;Write value of 0xFFB253 to DC Voltage Offset Register.
4C 00 00 14	;Set PulseRateE Register to 0.625 Hz.
74 00 00 04	;Unmask bit #2 ("LSD" bit in the Mask Register).
E8	;Start continuous conversions
78 00 01 40	;Write STOP bit to Control Register, to terminate auto-boot initialization sequence, and set the $\overline{\text{EOUT}}$ pulse output to Mechanical Counter Format.

5.6.3 Which EEPROMs Can Be Used?

Several industry-standard serial EEPROMs that will successfully run auto-boot with the CS5461 are listed below:

- Atmel — AT25010, AT25020, AT25040
- National Semiconductor — NM25C040M8, NM25020M8
- Xicor — X25040SI

These types of serial EEPROMs expect a specific 8-bit command word (00000011) in order to perform a memory download. The CS5461 has been hardware programmed to transmit this 8-bit command word to the EEPROM at the beginning of the auto-boot sequence.

6. SERIAL PORT OVERVIEW

The CS5461's serial port incorporates a state machine with transmit/receive buffers. The state machine interprets 8 bit command words on the rising edge of SCLK. Upon decoding of the command word, the state machine performs the requested command or prepares for a data transfer of the addressed register. Request for a read requires an internal register transfer to the transmit buffer, while a write waits until the completion of 24 SCLKs before performing a transfer. The internal registers are used to control the ADC's functions. All registers are 24-bits in length.

The CS5461 is initialized and fully operational in its *active* state upon power-on. After a power-on, the device will wait to receive a valid command (the first 8-bits clocked into the serial port). Upon receiving and decoding a valid command word, the state machine instructs the converter to either perform a system operation, or transfer data to or from an internal register.

6.1 Commands

All command words are 1 byte in length. Any 8-bit word that is not listed in this section is considered an invalid command word. Commands that write to a register must be followed by 3 bytes of register data. Commands that read data can be chained with other commands (e.g., while reading data, a new command can be sent to SDI which can execute before the original read is completed).

6.1.1 Start Conversions

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	C	0	0	0

This command indicates to the state machine to begin acquiring measurements and calculating results. The device has two modes of acquisition.

C = Modes of acquisition/measurement
0 = Perform a single computation cycle
1 = Perform continuous computation cycles

6.1.2 SYNC0 Command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	0

This command is the end of the serial port re-initialization sequence. The command can also be used as a NOP command. The serial port is resynchronized to byte boundaries by sending three or more consecutive SYNC1 commands followed by a SYNC0 command.

6.1.3 SYNC1 Command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	1

This command is part of the serial port re-initialization sequence. The command also serves as a NOP command.

6.1.4 Power-Up/Halt

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

If the device is powered-down, this command will initiate a power on reset. If the part is already powered-on, all computations will be halted.

6.1.5 Power-Down and Software Reset

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	S1	S0	0	0	0

The device has two power-down states to conserve power. If the chip is put in stand-by state, all circuitry except the analog/digital clock generators is turned off. In the sleep state, all circuitry except the digital clock generator and the instruction decoder is turned off. Bringing the CS5461 out of sleep state requires more time than out of stand-by state, because of the extra time needed to re-start and re-stabilize the analog clock signal.

S1,S0 Power-down state
00 = Software Reset
01 = Halt and enter stand-by power saving state. This state allows quick power-on time
10 = Halt and enter sleep power saving state. This state requires a slow power-on time
11 = Reserved

6.1.6 Calibration

B7	B6	B5	B4	B3	B2	B1	B0
1	1	0	V	I	R	G	O

The device can perform a system AC offset calibration, DC offset calibration, AC gain calibration, and DC gain calibration. Offset and gain calibrations should NOT be performed at the same time (must do one after the other). Only one gain calibration sequence should be performed for any given application. If calibration is needed, calibrate either AC gain or DC gain, but not both. The user must supply the proper inputs to the device before initiating calibration.

V,I Designates calibration channel
00 = Calibrate neither channel
01 = Calibrate the current channel
10 = Calibrate the voltage channel
11 = Calibrate voltage and current channel simultaneously

R Designates calibration
0 = DC calibration
1 = AC calibration

G Designates gain calibration
0 = No gain calibration
1 = Perform gain calibration

O* Designates offset calibration
0 = No offset calibration
1 = Perform offset calibration

*If O is set then G is ignored.

6.1.7 Register Read/Write

B7	B6	B5	B4	B3	B2	B1	B0
0	W/$\overline{R}$	RA4	RA3	RA2	RA1	RA0	0

The Read/Write informs the state machine that a register access is required. During a *read* operation, the addressed register is loaded into the device's output buffer and clocked out by SCLK. During a *write* operation, the data is clocked into the input buffer and, and all 24 bits are transferred to the addressed register on the 24th SCLK.

W/$\overline{R}$ Write/Read control
0 = Read register
1 = Write register

RA[4:0] Register address bits (bits 1 through 5) of the read/write command.

Address	RA[4-0]	Abbreviation	Name/Description
0	00000	Config	Configuration Register
1	00001	I_{DCoff}	Current Offset Register
2	00010	I_{gn}	Current Gain Register
3	00011	V_{DCoff}	Voltage Offset Register
4	00100	V_{gn}	Voltage Gain Register
5	00101	Cycle Count	Number of A/D conversions used in one computation cycle (N)).
6	00110	PulseRateE	Sets the EOUT/EDIR energy-to-frequency output pulse rate.
7	00111	I	Instantaneous Current Register (last current value)
8	01000	V	Instantaneous Voltage Register (last voltage value)
9	01001	P	Instantaneous Power Register (Last Power value)
10	01010	P_{Avg}	Average Power Register (avg. power over last computation cycle)
11	01011	I_{RMS}	RMS Current Register (RMS value over last comp. cycle)
12	01100	V_{RMS}	RMS Voltage Register (RMS value over last comp. cycle)
13	01101	TBC	Timebase Calibration Register
14	01110	P_{off}	Power Offset Calibration Register
15	01111	Status	Status Register (Write of '1' to status bit will clear the bit.)
16	10000	I_{ACoff}	AC (RMS) Current Offset Register
17	10001	V_{ACoff}	AC (RMS) Voltage Offset Register
18	10010	PulseRateF	Sets the FOUT power-to-frequency output pulse rate.
19	10011	T	Temperature Register
20	10100	Res	Reserved †
21	10101	PW	Pulse width register for mechanical counter output mode
22	10110	Res	Reserved †
23	10111	$VSAG_{Level}$	Voltage Sag Level Threshold Register.
24	11000	$VSAG_{Duration}$	Voltage Sag Duration Register.
25	11001	Res	Reserved †
26	11010	Mask	Mask Register
27	11011	Res	Reserved †
28	11100	Ctrl	Control Register
29	11101	Res	Reserved †
30	11110	Res	Reserved †
31	11111	Res	Reserved †

† These registers are for internal use only. For proper device operation, the user must *not* attempt to write to these registers.

6.2 Serial Port Interface

The CS5461's serial interface consists of four control lines, which have the following pin-names: $\overline{CS}$, SDI, SDO, and SCLK.

1) $\overline{CS}$ is the control line which enables access to the serial port. If the $\overline{CS}$ pin is tied to logic 0, the port can function as a three wire interface.
2) SDI is the data signal used to transfer data to the converter.
3) SDO is the data signal used to transfer output data from the converter. The SDO output will be held at high impedance any time $\overline{CS}$ is at logic 1.
4) SCLK is the serial bit-clock which controls the shifting of data to or from the ADC's serial port. The $\overline{CS}$ pin must be held at logic 0 before SCLK transitions can be recognized by the port logic. To accommodate opto-isolators SCLK is designed with a Schmitt-trigger input to allow an opto-isolator with slower rise and fall times to directly drive the pin.

6.3 Serial Read and Write

The state machine decodes the command word as it is received. Data is written to and read from the CS5461 by using the Register Read/Write operation. A transfer of data is always initiated by sending the appropriate 8-bit command (MSB first) to the serial port (SDI pin). Figure 1 illustrates the serial sequence necessary to write to, or read from the serial port's buffers.

During a write operation, the serial port will continue to clock in the data bits (MSB first) on the SDI pin for the 24 SCLK cycles.

When a read command is initiated, the serial port will start transferring register content bits serial (MSB first) on the SDO pin for 8, 16, or 24 SCLK cycles. Command words instructing a register read may be terminated at 8-bit boundaries. Also data register reads allow "command chaining". This means the micro-controller can send a new command while reading register data. The new command will be acted upon immediately and could possibly terminate the first register read. For example, if only the 16 most significant bits of data from the first read are required, a second read command on SDI can be initiated after the first 8 data bits are read from SDO.

During a read cycle, the SYNC0 command (NOP) should be strobed on the SDI port while clocking the data from the SDO port.

6.4 System Initialization

A software or hardware reset can be initiated at any time. The software reset is initiated by sending the command 0x80.

A hardware reset is initiated when the $\overline{RESET}$ pin is forced low with a minimum pulse width of 50 ns. The $\overline{RESET}$ signal is asynchronous, requiring no MCLKs for the part to detect and store a reset event. The $\overline{RESET}$ pin is a Schmitt Trigger input, which allows it to accept slow rise times and/or noisy control signals. Once the $\overline{RESET}$ pin is inactive, the internal reset circuitry remains active for 5 MCLK cycles to insure resetting the synchronous circuitry in the device. The modulators are held in reset for 12 MCLK cycles after $\overline{RESET}$ becomes inactive. After a hardware or software reset, the internal registers (some of which drive output pins) will be reset to their *default* values on the first MCLK received after detecting a reset event. The internal register values are also set to their default values after initial power-on of the device. The CS5461 will then assume its *active* state.

6.5 Serial Port Initialization

It is possible for the serial interface to become unsynchronized, with respect to the SCLK input. If this occurs, any attempt to clock valid CS5461 commands into the serial interface may result in unexpected operation. The CS5461's serial port must then be re-initialized. To initialize the serial port, any of the following actions can be performed:

1) Drive the $\overline{CS}$ pin low [or if $\overline{CS}$ pin is already low, drive the pin high, then back to low].
2) Hardware Reset (drive $\overline{RESET}$ pin low, for at least 10 μs).
3) Issue the *Serial Port Initialization Sequence*, which is performed by clocking 3 (or more) SYNC1 command bytes (0xFF) followed by one SYNC0 command byte (0xFE).

6.6 CS5461 Power States

Active state denotes the operation of CS5461 when the device is fully powered on (not in *sleep* state or *stand-by* state). To insure that the CS5461 is operating in the *active* state; perform one of the three actions below:

1) Power on the CS5461. (Or if the device is already powered on, recycle the power.)
2) Software Reset
3) Hardware Reset

If the device is in *sleep* state or in *stand-by* state, issuing the Power-Up/Halt command will also insure that the device is in *active* state. In order to send the Power-Up/Halt command to the device, the serial port must be initialized. Therefore, after applying power to the CS5461, a hardware reset should always be performed.

7. REGISTER DESCRIPTION

1. “Default**” => bit status after power-on or reset
2. Any bit not labeled is Reserved. A zero should always be used when writing to one of these bits.

7.1 Configuration Register

Address: 0

23	22	21	20	19	18	17	16
PC6	PC5	PC4	PC3	PC2	PC1	PC0	Igain
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EWA			IMODE	IINV	EPP	EOP	EDP
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	VHPF	IHPF	iCPU	K3	K2	K1	K0

Default** = 0x000001

PC[6:0] Phase compensation. A 2’s complement number which sets the delay in the voltage channel. When MCLK=4.096 MHz and K=1, the phase adjustment range is about -2.8 to +2.8 degrees and each step is about 0.04 degrees (assuming a power line frequency of 60 Hz). If (MCLK / K) is not 4.096 MHz, the values for the range and step size should be scaled by the factor 4.096MHz / (MCLK / K).

Default setting is 0000000 = 0.0215 degrees phase delay at 60 Hz (when MCLK = 4.096 MHz).

Igain Sets the gain of the current PGA
0 = gain is 10 (default)
1 = gain is 50

EWA Allows the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins to be configured as open-collector output pins.
0 = normal outputs (default)
1 = only the pull-down device of the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins are active

[IMODE IINV] Soft interrupt configuration bits. Select the desired pin behavior for indication of an interrupt.
00 = active low level (default)
01 = active high level
10 = falling edge (INT is normally high)
11 = rising edge (INT is normally low)

EPP Allows the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins to be controlled by the DL0 and DL1 bits. $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ can also be accessed using the Status Register.
0 = Normal operation of the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins. (default)
1 = EOP and EDP bits control the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins.

EOP When EPP = 1, $\overline{\text{EOUT}}$ becomes a user defined pin, and EOP sets the value of the $\overline{\text{EOUT}}$ pin. Default = '0'

EDP When EPP = 1, $\overline{\text{EDIR}}$ becomes a user defined pin, EDP sets the value of the $\overline{\text{EDIR}}$ pin. Default = '0'

VHPF Control the use of the High Pass Filter on the voltage Channel.
0 = High-pass filter disabled (default)
1 = High-pass filter enabled

IHPF Control the use of the High Pass Filter on the Current Channel.

0 = High-pass filter disabled (default)
1 = High-pass filter enabled

iCPU — Inverts the CPUCLK clock. In order to reduce the level of noise present when analog signals are sampled, the logic driven by CPUCLK should not be active during the sample edge.
0 = normal operation (default)
1 = minimize noise when CPUCLK is driving rising edge logic

K[3:0] — Clock divider. A 4-bit binary number used to divide the value of MCLK to generate the internal clock DCLK. The internal clock frequency is DCLK = MCLK/K. The value of K can range between 1 and 16. Note that a value of "0000" will set K to 16 (not zero).

7.2 DC Current Offset Register and DC Voltage Offset Register

Address: 1 (DC Current Offset Register); 3 (DC Voltage Offset Register)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 0.000

The DC Offset Registers are initialized to zero on reset, allowing for uncalibrated normal operation. If DC Offset Calibration is performed, this register is updated after one computation cycle with the current or voltage offset if the proper DC input signals are applied. DRDY will be asserted at the end of the calibration. This register may be read and stored for future system offset compensation. The value is in the range ± full scale. The numeric format of this register is two's complement notation.

7.3 AC/DC Current Gain Register and AC/DC Voltage Gain Register

Address: 2 (Current Gain Register); 4 (Voltage Gain Register)

MSB															LSB
2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default** = 1.000

The Gain Registers are initialized to 1.0 on reset, allowing for uncalibrated normal operation. The Gain registers hold the result of either the AC or DC gain calibrations, whichever was most recently performed. If DC calibration is performed, the register is updated after one computation cycle with the system gain when the proper DC input is applied. If AC calibration is performed, then after ~(6N + 30) A/D conversion cycles (where N is the value of the Cycle-Count Register) the register(s) is updated with the system gain when the proper AC input is applied. DRDY will be asserted at the end of the calibration. The register may be read and stored for future system gain compensation. The value is in the range $0.0 \leq \text{Gain} < 3.9999$.

7.4 Cycle Count Register

Address: 5

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default** = 4000

The Cycle Count Register value (denoted as 'N') determines the length of one energy and RMS *computation cycle*. During continuous conversions, the computation cycle frequency is (MCLK/K)/(1024∗N).

7.5 PulseRateE Register

Address: 6

MSB															LSB
2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	.....	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}

Default** = 32000.00 Hz

The PulseRateE Register determines the average frequency of the pulses issued on the $\overline{\text{EOUT}}$ output pin. The register's smallest valid value is 2^{-4} but can be in 2^{-5} increments. A pulserate higher than MCLK/K/8 will result in a pulse rate setting of MCLK/K/8.

7.6 I, V, P, & P_{Avg}: Instantaneous Current, Voltage, Power, and Average Power (Signed) Output Register

Address: 7 - 10

MSB															LSB
$-(2^{0})$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

These signed registers contain the last measured value of I, V, P, and P_{AVG}. The results will be within in the range of $-1.0 \le I,V,P,P_{Avg} < 1.0$. The value is represented in two's complement notation, with the binary point place to the right of the MSB (MSB has a negative weighting). These values are 22 bits in length. The two least significant bits have no meaning, and will always have a value of "0".

7.7 I_{RMS}, V_{RMS} Unsigned Output Register

Address: 11,12

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

These unsigned registers contain the last values of I_{RMS} and V_{RMS}. The results are in the range of $0.0 \le I_{RMS},V_{RMS} < 1.0$. The value is represented in (unsigned) binary notation, with the binary point place to the left of the MSB. These results are updated after each computation cycle.

7.8 Timebase Calibration Register

Address: 13

MSB															LSB
2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 1.000

This register can be set with a clock frequency error compensation value, to correct for a gain/timing error caused by the crystal/oscillator tolerance. The value is in the range $0.0 \le TBC < 2.0$.

7.9 Power Offset Register

Address: 14

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 0.000

This offset value is added to each power value that is computed for each voltage/current sample pair before being accumulated in the Energy Register. This register can be used to offset contributions to the energy result that are caused by undesirable sources of energy that are inherent in the system. This value is in two's complement notation.

7.10 Status Register and Mask Register

Address: *15* (*Status Register*)*; 26 (Mask Register)*

23	22	21	20	19	18	17	16
DRDY	EOUT	EDIR	CRDY			IOR	VOR
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	IROR	VROR		EOOR			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
			VOD	IOD	LSD	VSAG	$\overline{IC}$

Default** = 0x000000 (Status Register)

0x000000 (Mask Register)

The Status Register indicates the condition of the chip. In normal operation writing a '1' to a bit will cause the bit to go to the '0' state. Writing a '0' to a bit will maintain the status bit in its current state. With this feature the user can simply write to the Status Register to clear the bits that have been seen, without concern of clearing any newly set bits. Even if a status bit is masked to prevent an interrupt, the status bit will still be set in the Status Register.

The Mask Register is used to control the activation of the $\overline{INT}$ pin. Placing a logic '1' in the Mask Register will allow the corresponding bit in the Status Register to activate the $\overline{INT}$ pin when the status bit is asserted.

DRDY — Data Ready. When running in single or continuous conversion acquisition mode, this bit will indicate the end of computation cycles. When running calibrations, this bit indicates the end of a calibration sequence.

EOUT — Indicates that the energy limit has been reached for the $\overline{EOUT}$ Energy Accumulation Register, and so this register will be cleared, and one pulse will be generated on the $\overline{EOUT}$ pin (if enabled). If $\overline{EOUT}$ is asserted, this bit will be cleared automatically just after the beginning of any subsequent A/D conversion cycle in which no $\overline{EOUT}$ pulses need to be issued. The bit can also be cleared by writing to the Status Register. This status bit is set with a maximum frequency of 4 kHz (when MCLK/K is 4.096 MHz). When MCLK/K is not equal to 4.096 MHz, the user should scale the pulse-rate would be expected with MCLK/K = 4.096 MHz by a factor of 4.096 MHz / (MCLK/K), to get the actual pulse-rate.

EDIR — Set whenever the $\overline{EOUT}$ bit is asserted as long as the energy result is negative. Reset/Clear behavior of the $\overline{EDIR}$ status bit is similar to the $\overline{EOUT}$ status bit.

IOR — Current Out of Range. Set when the *magnitude* of the calibrated current value is too large or too small to fit in the Instantaneous Current Register.

CRDY — Conversion Ready. Indicates a new conversion is ready. This will occur at the output word rate.

VOR — Voltage Out of Range.

VSAG — Indicates that the voltage threshold/duration conditions, specified in the $VSAG_{level}$ and $VSAG_{duration}$ Registers, have been met.

VROR — RMS Voltage Out of Range. Set when the calibrated RMS voltage value is too large to fit in the RMS Voltage Register.

IROR — RMS Current Out of Range. Set when the calibrated RMS current value is too large to fit in the RMS Current Register.

EOOR — $\overline{EOUT}$ Energy Summation Register Out of Range. Assertion of this bit can be caused by having a pulse output frequency that is too small for the power being measured. This problem can be corrected by specifying a higher frequency in the PulseRateE register.

VOD — Modulator oscillation detect on the voltage channel. Set when the modulator oscillates due to an input above Full Scale. Note that the level at which the modulator oscillates is significantly higher than the voltage channel's Differential Input Voltage Range.

IOD — Modulator oscillation detect on the current channel. Set when the modulator oscillates due to an input above Full Scale. Note that the level at which the modulator oscillates is significantly higher than the current channel's Differential Input Voltage Range.

Note: The IOD and VOD bits may be 'falsely' triggered by very brief voltage spikes from the power line. This event should not be confused with a DC overload situation at the inputs, when the IOD and VOD bits will re-assert themselves even after being cleared, multiple times.

LSD — Low Supply Detect. Set when the voltage at the PFMON pin falls below the low-voltage threshold (PMLO), with respect to VA- pin. For a given part, PMLO can be as low as 2.3 V. LSD bit cannot be permanently reset until the voltage at PFMON pin rises back above the high-voltage threshold (PMHI), which is typically 100 mV above the device's low-voltage threshold. PMHI will never be greater than 2.7 V.

$\overline{IC}$ — Invalid Command. Normally logic 1. Set to logic 0 if the host interface is strobed with an 8-bit word that is not recognized as one of the valid commands (see Section 6.1, *Commands*).

7.11 AC Current Offset Register and AC Voltage Offset Register

Address: 16 (AC Current Offset Register); 17 (AC Voltage Offset Register)

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

Default** = 0x000000

The AC Offset Registers are initialized to zero on reset, allowing for uncalibrated normal operation. When AC Offset Calibration is performed, the offset register(s) is updated with the square of the system AC offset value. This sequence lasts ~(6N + 30) A/D conversion cycles (where N is the value of the Cycle-Count Register). DRDY will be asserted at the end of the calibration. The register value may be read and stored for future system offset compensation.

7.12 PulseRateF Register

Address: 18

MSB															LSB
2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	.....	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}

Default** = 32000.00 Hz

The PulseRateF Register sets the average pulse frequency of the $\overline{\text{FOUT}}$ output pin. The register's smallest valid value is 2^{-4} but can be in 2^{-5} increments. A pulserate higher than MCLK/K/8 will result in a pulse rate setting of MCLK/K/8.

7.13 Temperature Sensor Output Register

Address: 19

MSB															LSB
$-(2^{7})$	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	.....	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

This signed register contains the output of the On-Chip Temperature Sensor. The results are in the range of $-128.0 \leq T < 128.0$. The value is represented in unsigned binary notation, with the binary point place to the left of the MSB. This result is updated after each computation cycle.

7.14 Pulsewidth

Address: 21

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Default** = 512 sample periods

This signed register determines the pulsewidth of $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pulses in Mechanical Counter Mode. The width is set in number of sample periods. The default is 512. This corresponds to a pulsewidth of 512 samples / [(MCLK/K)/1024] = 128 msec with MCLK = 4.096 MHz and K = 1. Although this is a signed register a negative value will have no meaning; pulsewidth settings must be positive.

7.15 $VSAG_{Level}$: Voltage Sag-Detect Threshold Level

Address: 23

	MSB														LSB
$-(2^{0})$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 0x000000

This signed register sets the threshold level for the Voltage Sag Detect feature. To activate the VSAG bit the Status Register, the value of the V_{RMS} register must remain below this threshold level for a set number of samples (defined in the VSAGDuration Register). Voltage threshold levels must be positive values; a negative value can be used to disable the feature. For more information about the voltage sag detect functionality, refer to Section 4.10 of the data sheet.

7.16 $VSAG_{Duration}$: Voltage Sag-Detect Duration Level

Address: 24

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Default** = 0x000000

This Register sets the number of conversions over to accumulate RMS voltage for comparison against the $VSAG_{LEVEL}$. Setting this register to zero will disable the VSAG feature.

7.17 Control Register

Register Address: 28

23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
					FAC	EAC	STOP
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	MECH		INTOD		NOCPU	NOOSC	STEP

Default** = 0x000000

FAC 1 = enable anti-creep for $\overline{\text{FOUT}}$ pulse output function.

EAC 1 = enable anti-creep for $\overline{\text{EOUT}}$ pulse output function.

STOP 1 = used to terminate the new EEBOOT sequence.

MECH 1 = widens $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pulses for mechanical counters.

INTOD 1 = Converts $\overline{\text{INT}}$ output to open drain configuration.

NOCPU 1 = saves power by disabling the CPUCLK external drive pin.

NOOSC 1 = saves power by disabling the crystal oscillator circuit.

STEP 1 = enables stepper-motor signals on the $\overline{\text{EOUT}}$/$\overline{\text{EDIR}}$ pins.

8. BASIC APPLICATION CIRCUITS

Figure 14 shows the CS5461 connected to a service to measure power in a single-phase 2-wire system while operating in a single supply configuration. Note that in this diagram the shunt resistor used to monitor the line current is connected on the "Line" (hot) side of the power mains. In most residential power metering applications, the power meter's current-sense shunt resistor is intentionally placed on the hot side of the power mains in order to detect a subscriber's attempt to steal power. In this type of shunt-resistor configuration, the common-mode level of the CS5461 must be referenced to the hot side of the power line; which means the common-mode potential of the CS5461 will typically oscillate to very high voltage levels with respect to earth ground potential. If digital communication networks require that the CMOS-level digital interface be referenced to an earth ground, the serial interface pins on the CS5461 *must be isolated* from the external digital interface.

Figure 15 shows the same single-phase two-wire system with complete isolation from the power lines. This isolation is achieved using three transformers: a general purpose transformer to supply the on-board DC power; a high-precision, low impedance voltage transformer, with very little roll-off/phase-delay, to measure voltage; and a current transformer to sense the line current. Because the CS5461 is not directly connected to the power mains, no isolation is necessary on the CS5461's digital interface.

Figure 16 shows a single-phase 3-wire system. In many 3-wire residential power systems within the United States, only the two line terminals are available (neutral is not available). Figure 17 shows the CS5461 configured to meter a three-wire system with no neutral available.

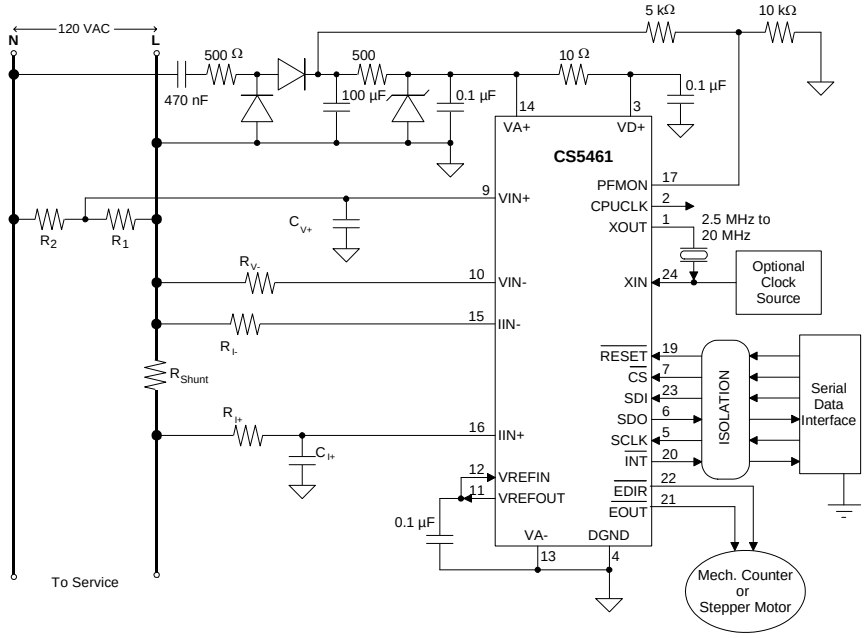


Figure 14. Typical Connection Diagram (One-Phase 2-Wire, Direct Connect to Power

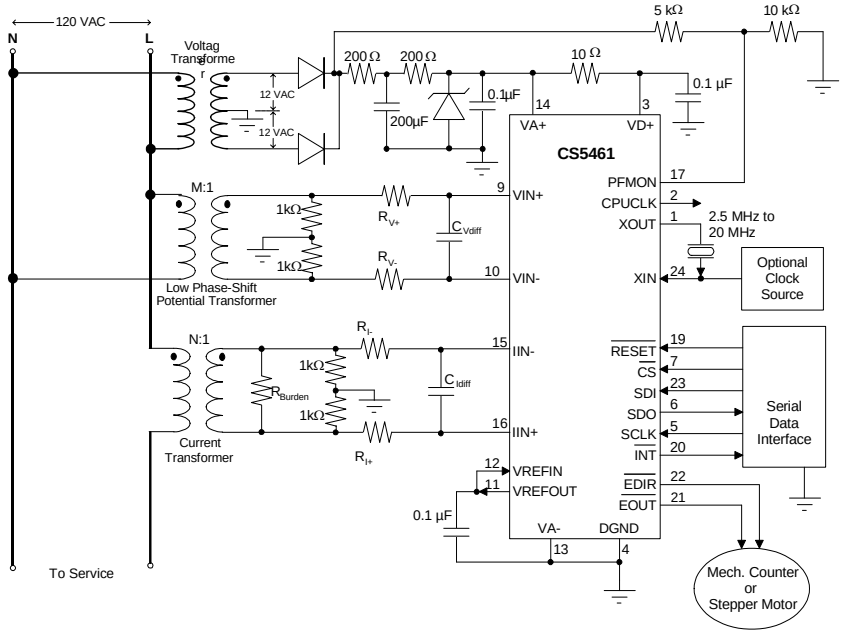


Figure 15. Typical Connection Diagram (One-Phase 2-Wire, Isolated from Power Line)

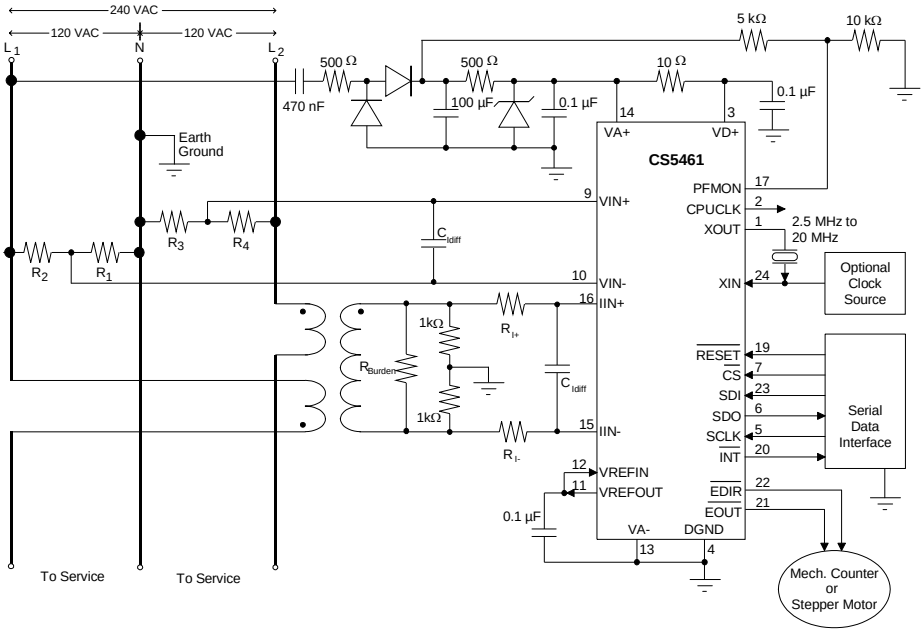


Figure 16. Typical Connection Diagram (One-Phase 3-Wire)

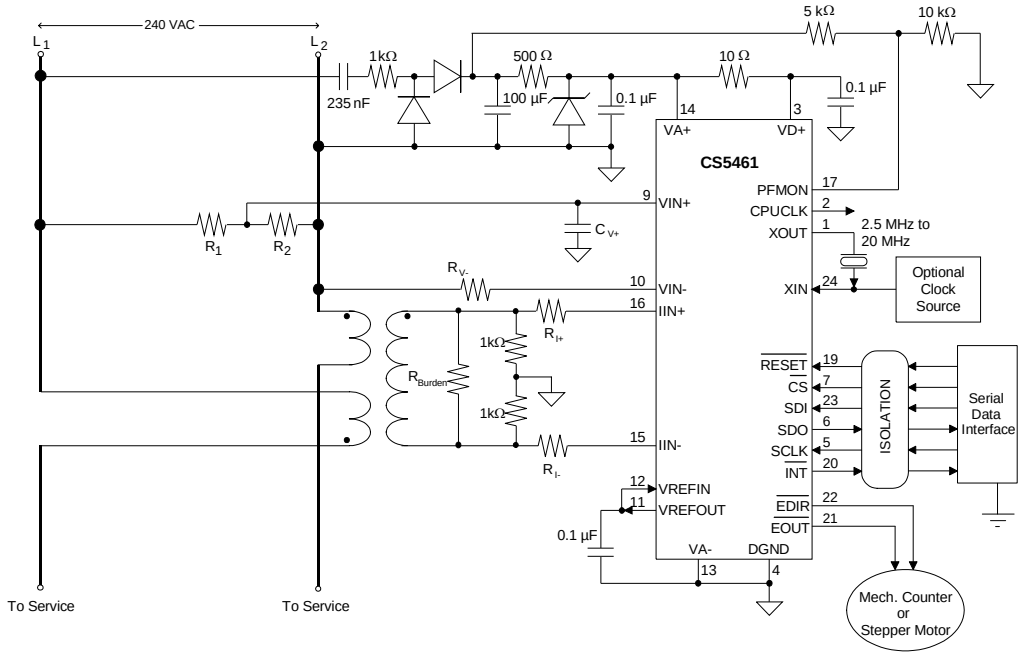
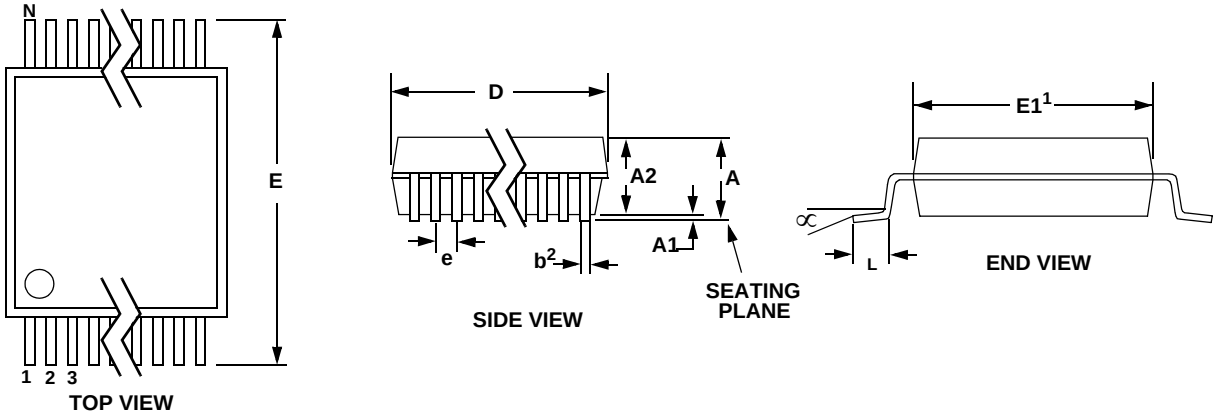


Figure 17. Typical Connection Diagram (One-Phase 3-Wire - No Neutral Available)

9. PACKAGE DIMENSIONS

24L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.068	0.074	1.62	1.73	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.311	0.323	0.335	7.90	8.20	8.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.03	0.041	0.63	0.75	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters.

Notes: 1. “D” and “E1” are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension “b” does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of “b” dimension at maximum material condition. Dambar intrusion shall not reduce dimension “b” by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

10. REVISIONS

Revision	Date	Changes
A1	March 2003	Initial Release
PP1	13 October 2003	Initial release for Preliminary Product Information
PP2	5 December 2003	1) Added Auto-boot Feature Description (Page Page 1, 6, 12, 27, 28, 37, 13) 2) Added Mode Pin Functionality (Page 6, 12, 27)

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to **www.cirrus.com**