HD66841F

LCD Video Interface Controller II (LVIC-II)

Description

The HD66841F LCD video interface controller (LVIC-II) converts standard RGB video signals for CRT display into LCD data. It enables a CRT display system to be replaced by an LCD system without any changes, and it also enables software originally intended for CRT display to control an LCD.

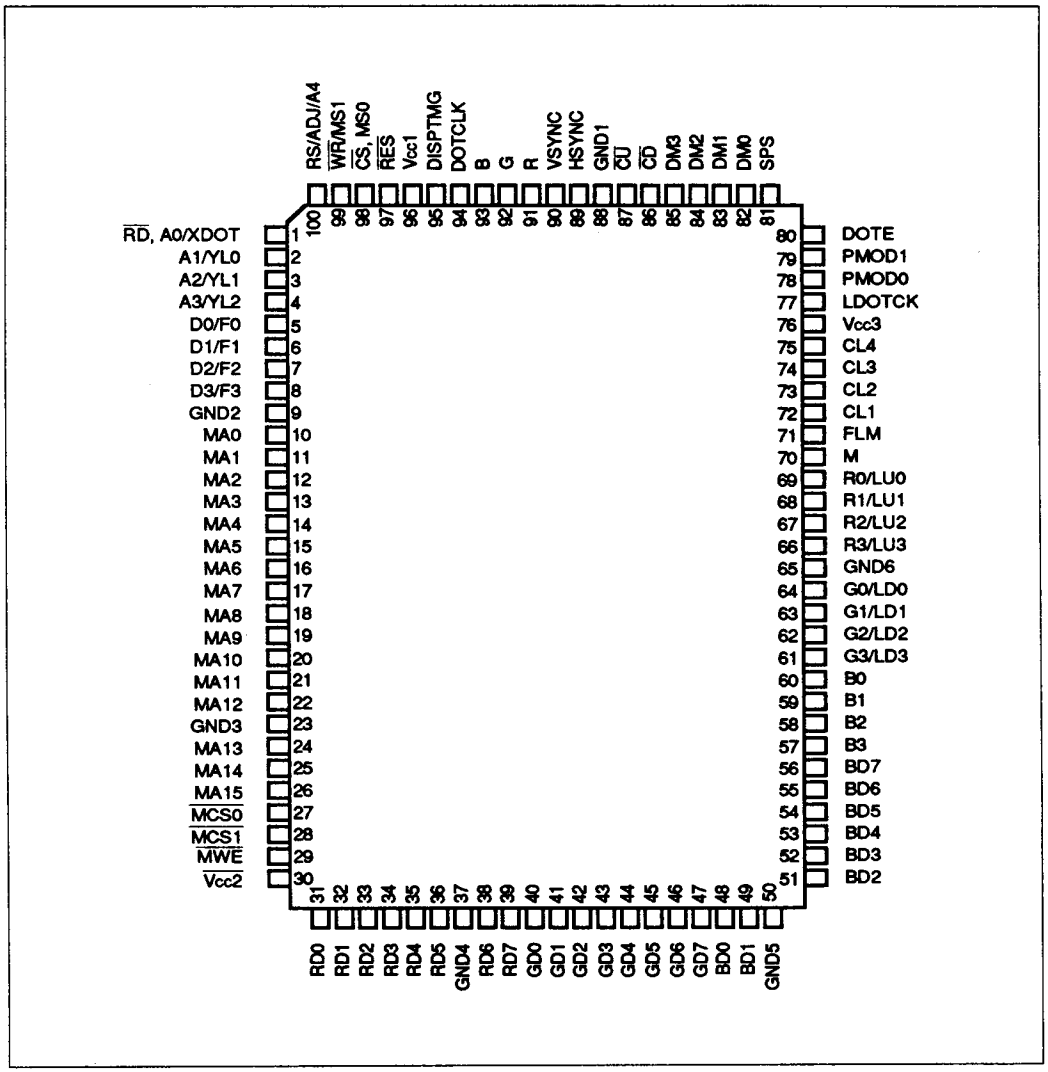
Since the LVIC-II can control TFT-type LCDs in addition to current TN-type LCDs, it can support monochrome, 8-level gray-scale, and 8-color displays. Thanks to a gray-scale palette, any 8 levels can be selected from 13 gray-scale levels, depending on the LCD panel used.

The LVIC-II also features a programmable screen size and can control a large-panel LCD of up to 720 × 512 dots.

Features

- Conversion of RGB video signals used for CRT display into LCD data:
  - Monochrome display data
  - 8-level gray-scale data
  - 8-color display data
- Selectable LVIC-II control method:
  - Pin programming method
  - Internal register programming method (either with MPU or ROM)
- Programmable screen size:
  - 640 or 720 dots (80 or 90 characters) wide by 200, 350, 400, 480, 512, or 540 dots (lines) high, using the pin programming method
  - 32 to 4048 dots (4 to 506 characters) wide by 4 to 1024 dots (lines) high, using the internal register programming method
- Double-height display capability
- Generation of display timing signal (DISPTMG) from horizontal synchronization (HSYNC) and vertical synchronization (VSYNC) signals
- Internal PLL circuit capable of generating a CRT display dot clock (DOTCLK) (external charge pump, low pass filter (LPF), and voltage-controlled oscillator (VCO) required)
- Control of both TN-type LCDs and TFT-type LCDs
- Gray-scale level selection from gray-scale palette
- Maximum operating frequency: 30MHz (DOTCLK)
- LCD driver interface: 4-, 8-, or 12-bit (4 bits each for R, G, and B) parallel data transfer
- Recommended LCD drivers: HD61104 (column), HD61105 (row), HD61106 and HD66107T (column/row)
- Direct interface with buffer memory (no external decoder required)
- 1.3-µm CMOS processing
- Single power supply: +5V ± 10%
- Package: 100-pin plastic QFP (FP-100A)

Pin Arrangement



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Pin Description

The LVIC-II's pins are listed in table 1 and their functions are described below.

Table 1 Pin Description

Classification	Symbol	Pin Number	Pin Name	I/O	Note(s)
Power supply	$V_{CC}1$–$V_{CC}3$	96, 30, 76	$V_{CC}1$ to $V_{CC}3$	—	
	GND1–GND6	88, 9, 23, 37, 50, 65	Ground 1 to Ground 6	—	
Video signal interface	R, G, B	91, 92, 93	Red, green, and blue serial data	I	1
	HSYNC	89	Horizontal synchronization	I	
	VSYNC	90	Vertical synchronization	I	
	DISPTMG	95	Display timing	I	2
	DOTCLK	94	Dot clock	I	
LCD interface	R0–R3	69–66	LCD red data 0–3	O	3
	LU0–LU3	69–66	LCD upper panel data 0–3	O	4
	G0–G3	64–61	LCD green data 0–3	O	3, 5
	LD0–LD3	64–61	LCD lower panel data 0–3	O	4, 5
	B0–B3	60–57	LCD blue data 0–3	O	3, 6
	CL1	72	LCD data line select clock	O	
	CL2	73	LCD data shift clock	O	
	CL3	74	Y-driver shift clock 1	O	7
	CL4	75	Y-driver shift clock 2	O	7
	FLM	71	First line marker	O	
	M	70	LCD driving signal alternation	O	
	LDOTCK	77	LCD dot clock	I	
Buffer memory interface	$\overline{MCS0}$, $\overline{MCS1}$	27, 28	Memory chip select 0, 1	O	8
	$\overline{MWE}$	29	Memory write enable	O	8
	MA0–MA15	10–22, 24–26	Memory address 0–15	O	8
	RD0–RD7	31–36, 38, 39	Memory red data 0–7	I/O	8
	GD0–GD7	40–47	Memory green data 0–7	I/O	8, 9
	BD0–BD7	48, 49, 51–56	Memory blue data 0–7	I/O	8, 9
Mode setting	PMOD0, PMOD1	78, 79	Program mode 0, 1	I	
	DOTE	80	Dot clock edge change	I	
	SPS	81	Synchronization polarity select	I	
	DM0–DM3	82–85	Display mode 0–3	I	
	MS0, MS1	98, 99	Memory select 0, 1	I	10, 11
	XDOT	1	X-dot	I	10
	YL0–YL2	2–4	Y-line 0–2	I	10, 12

Table 1 Pin Description(cont)

Classification	Symbol	Pin Number	Pin Name	I/O	Note(s)
Mode setting	ADJ	100	Adjust	I	10
	F0–F3	5–8	Fine adjust 0–3	I	10
MPU interface	$\overline{CS}$	98	Chip select	I	10, 11
	$\overline{WR}$	99	Write	I	10, 11, 13
	$\overline{RD}$	1	Read	I	10, 13
	RS	100	Register select	I	10
	D0–D3	5–8	Data 0–3	I/O	10
	$\overline{RES}$	97	Reset	I	14
ROM interface	A0–A4	1–4, 100	Address 0–4	O	10
	D0–D3	5–8	Data 0–3	I	10
PLL interface	$\overline{CD}$	86	Charge down	O	
	$\overline{CU}$	87	Charge up	O	

Notes:
1. Fix G and B pins low if CRT display data is monochrome.
2. Fix high or low if the display timing signal is generated internally.
3. For 8-color display modes.
4. For monochrome or 8-level gray-scale display modes.
5. Leave disconnected in 4-bit/single-screen data transfer modes.
6. Leave disconnected in monochrome or 8-level gray-scale display modes.
7. Leave disconnected in TN-type LCD modes.
8. Leave disconnected if no buffer memory is used.
9. Pull up with a resistor of about 20 kΩ in monochrome display modes. The LVIC-II writes the OR of RGB signals into R-plane RAM, so no RAM is required for the G and B planes in these modes. (If G- or B-plane RAM is connected in monochrome display modes, the LVIC-II writes G or B signals into each RAM. However, this does not affect the display or the contents of R-plane RAM.)
10. Multiplexed pins.
11. Fix high or low when using the ROM programming method.
12. Fix high or low when using the MPU programming method.
13. Do not set pins $\overline{WR}$ and $\overline{RD}$ low simultaneously.
14. A reset signal must be input after power-on.

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Power Supply

$V_{CC}1$–$V_{CC}3$: Must be connected to a +5V power supply.

GND1–GND6: Must be grounded.

CRT Display Interface

R, G, B: Input R, G, and B signals for CRT display.

HSYNC: Inputs the CRT horizontal synchronization signal.

VSYNC: Inputs the CRT vertical synchronization signal.

DISPTMG: Inputs the display timing signal which indicates the horizontal or vertical display period.

DOTCLK: Inputs dot clock pulses used for CRT display.

LCD Interface

R0–R3: Output LCD R data

LU0–LU3: Output LCD upper panel data.

G0–G3: Output LCD G data.

LD0–LD3: Output LCD lower panel data.

B0–B3: Output LCD B data.

CL1: Outputs line select clock pulses for LCD data.

CL2: Outputs shift clock pulses for LCD data.

CL3: Outputs line select and shift clock pulses for LCD data if Y-drivers are positioned on one side of the LCD screen. Refer to the LCD System Configuration section for details.

CL4: Outputs line select and shift clock pulses for LCD data if Y-drivers are positioned on both sides of the LCD screen. Refer to the LCD System Configuration section for details.

FLM: Outputs a first line marker for Y-drivers.

M: Outputs an alternation signal for converting LCD driving signals to AC.

LDOTCK: Inputs LCD dot clock pulses.

Buffer Memory Interface

$\overline{MCS0}$, $\overline{MCS1}$: Output buffer memory chip select signals.

$\overline{MWE}$: Outputs the buffer memory write enable signal.

MA0–MA15: Output buffer memory addresses.

RD0–RD7: Transfer data between R-data buffer memory and the LVIC-II.

GD0–GD7: Transfer data between G-data buffer memory and the LVIC-II.

BD0–BD7: Transfer data between B-data buffer memory and the LVIC-II.

Mode Setting

PMOD0, PMOD1: Select the programming method for the LVIC-II (table 2).

DOTE: Switches data latch timing. The LVIC-II latches RGB signals at the falling edge of DOTCLK pulses if the DOTE pin is set high, or at the rising edge if it is set low.

SPS: Selects the polarity of the VSYNC signal. (The HSYNC signal's polarity is fixed.) The VSYNC signal is active-high if SPS is set high, or active-low if it is set low.

DM0–DM3: Select the display mode (table 8).

MS0–MS1: Select the buffer memory type (table 3).

XDOT: Specifies the number of characters displayed on the LCD screen in the horizontal direction (called the horizontal displayed characters). The number is 90 (720 dots) if XDOT is set high, or 80 (640 dots) if it is set low.

YL0–YL2: Specify the number of lines displayed on the LCD screen in the vertical direction (called the vertical displayed lines) (table 4).

ADJ: Determines whether the F0–F3 pins adjust the display timing signal or the number of vertical displayed lines. They pins adjust the display timing signal if ADJ is set high, or the number of vertical displayed lines if it is set low.

F0–F3: Adjust the number of vertical displayed lines (table 5) or the display timing signal. Refer to the Display Timing Signal Fine Adjustment section for details.

MPU Interface

$\overline{CS}$: An MPU inputs the $\overline{CS}$ signal through this pin to select the LVIC. An MPU can access the LVIC-II while this signal is low.

$\overline{WR}$: An MPU inputs the $\overline{WR}$ signal through this pin to write data into the LVIC-II's internal registers. An MPU can write data while this signal is low.

$\overline{RD}$: An MPU inputs the $\overline{RD}$ signal through this pin to read data from the LVIC-II's internal registers. An MPU can read data while this signal is low.

RS: An MPU inputs the RS signal through this pin to select the LVIC's internal registers. An MPU can access data registers (R0–R15) while this signal is high and the $\overline{CS}$ signal is low, and can select the address register (AR) while both this signal and the $\overline{CS}$ signal are low.

D0–D3: Transfer LVIC-II internal register data between an MPU and the LVIC-II.

$\overline{RES}$: Externally resets the LVIC-II.

ROM Interface

A0–A4: Output external ROM addresses.

D0–D3: Input external ROM data to the LVIC-II's internal registers.

PLL Circuit Interface

$\overline{CD}$: Outputs charge-down signals to an external charge pump.

$\overline{CU}$: Outputs charge-up signals to an external charge pump.

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Table 2 Programming Method Selection

PMOD1	PMOD0	Programming Method	
0	0	Pin programming	
0	1	Internal register programming	MPU
1	0		ROM
1	1	Inhibited (Note)	

Note: This combination is for test mode: it disables display.

Table 3 Memory Type Selection

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbytes memory
1	0	32-kbytes memory
1	1	64-kbytes memory

Table 4 Number of Vertical Displayed Lines

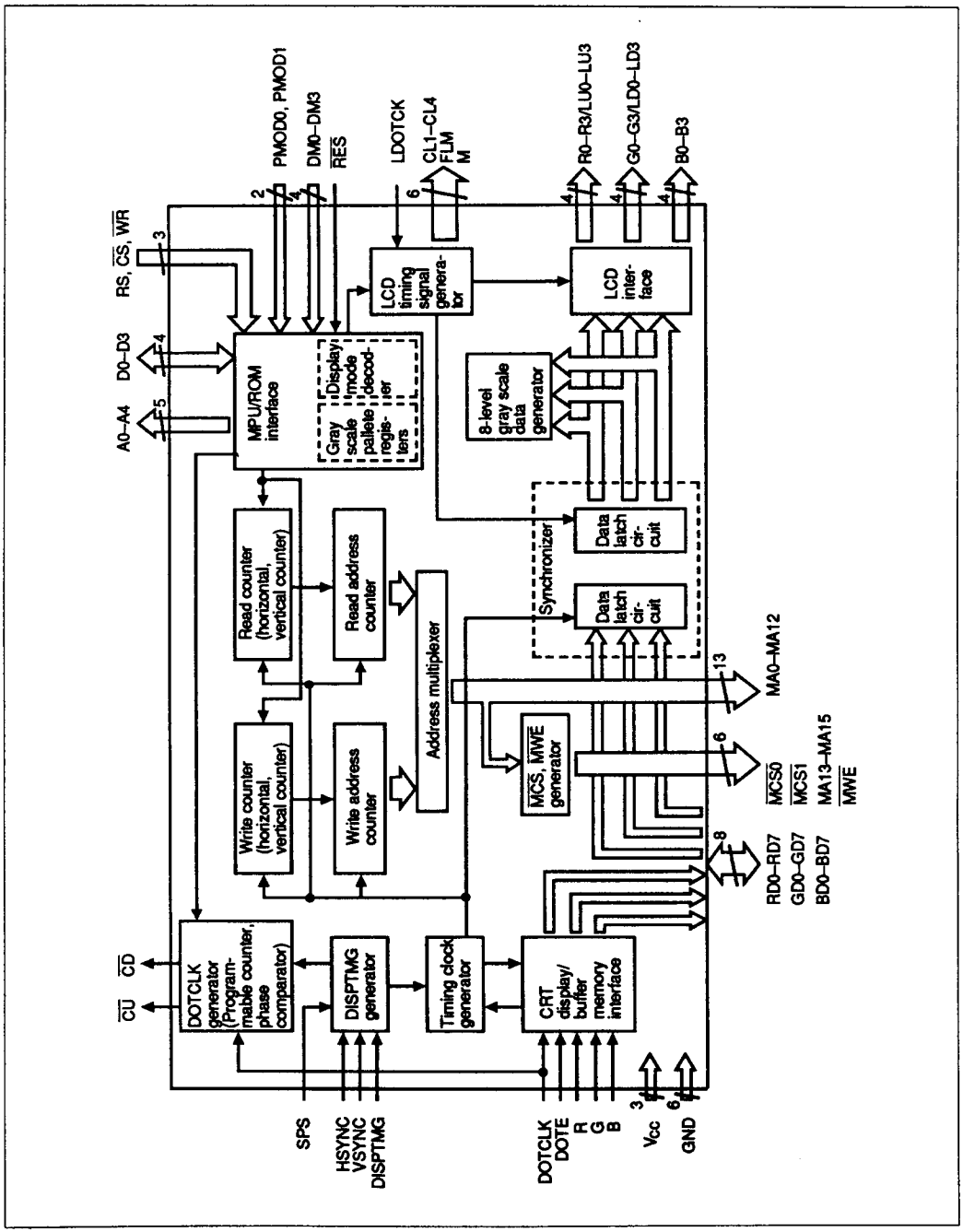
YL2	YL1	YL0	Number of Vertical Displayed Lines
0	0	0	200
0	0	1	350
0	1	0	400
0	1	1	480
1	0	0	512
1	0	1	540
1	1	0	Inhibited (Note)
1	1	1	

Note: 480 lines are displayed, but they are practically indistinguishable.

Table 5 Fine Adjustment of Vertical Displayed Lines

F3	F2	F1	F0	Number of Adjusted Lines
0	0	0	0	±0
0	0	0	1	+1
0	0	1	0	+2
⋮	⋮	⋮	⋮	⋮
1	1	1	0	+14
1	1	1	1	+15

Block Diagram



Registers

The LVIC-II's registers are listed in table 6 and the bit assignments within the registers are shown in figure 1.

Table 6 Register List

CS	RS	PS[1]	Reg. Address 3	2	1	0	Reg. No.	Register Name	Program Unit	Specified Value Symbol	Read/ Write[2]	Note(s)
1	—		—	—	—	—	—	—	—	—	—	
0	0		—	—	—	—	AR	Address register	—	—	W	3
0	1	0	0	0	0	0	R0	Control register 1	—	—	R/W	
0	1	0	0	0	0	1	R1	Control register 2	—	—	R/W	
0	1	0	0	0	1	0	R2	Vertical displayed lines register (middle-order)	Lines	Nvd	R/W	4
0	1	0	0	0	1	1	R3	Vertical displayed lines register (low-order)	Lines	Nvd	R/W	4
0	1	0	0	1	0	0	R4	Vertical displayed lines register (high-order)/ CL3 period register (high-order)	Lines/ Chars.	Nvd/ Npc	R/W	4, 5, 6
0	1	0	0	1	0	1	R5	CL3 period register (low-order)	Chars.	Npc	R/W	4, 5, 6
0	1	0	0	1	1	0	R6	Horizontal displayed characters register (high-order)	Chars.	Nhd	R/W	6
0	1	0	0	1	1	1	R7	Horizontal displayed characters register (low-order)	Chars.	Nhd	R/W	6
0	1	0	1	0	0	0	R8	CL3 pulse width register	Chars.	Npw	R/W	6
0	1	0	1	0	0	1	R9	Fine adjust register	Dots	Nda	R/W	7
0	1	0	1	0	1	0	R10	PLL frequency-division ratio register (high-order)	—	N_{PLL}	R/W	8
0	1	0	1	0	1	1	R11	PLL frequency-division ratio register (low-order)	—	N_{PLL}	R/W	8
0	1	0	1	1	0	0	R12	Vertical backporch register (high-order)	Lines	Ncvbp	R/W	4, 9
0	1	0	1	1	0	1	R13	Vertical backporch register (low-order)	Lines	Ncvbp	R/W	4, 9
0	1	0	1	1	1	0	R14	Horizontal backporch register (high-order)	Dots	Nchbp	R/W	4, 9
0	1	0	1	1	1	1	R15	Horizontal backporch register (low-order)	Dots	Nchbp	R/W	4, 9

Table 6 Register List (cont)

$\overline{CS}$	RS	PS[1]	Reg. Address 3	2	1	0	Reg. No.	Register Name	Program Unit	Specified Value Symbol	Read/ Write[2]	Note(s)
0	1	1	0	0	0	1	P1	Black palette register	—	—	R/W	
0	1	1	0	0	1	0	P2	Blue palette register	—	—	R/W	
0	1	1	0	0	1	1	P3	Red palette register	—	—	R/W	
0	1	1	0	1	0	0	P4	Magenta palette register	—	—	R/W	
0	1	1	0	1	0	1	P5	Green palette register	—	—	R/W	
0	1	1	0	1	1	0	P6	Cyan palette register	—	—	R/W	
0	1	1	0	1	1	1	P7	Yellow palette register	—	—	R/W	
0	1	1	1	0	0	0	P8	White palette register	—	—	R/W	
0	1	1	1	0	0	1		Reserved				
⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮				
0	1	1	1	1	1	1		Reserved				

Notes:
1. Corresponds to bit 2 of control register 1 (R0)
2. W indicates that the register can only be written to; R/W indicates that the register can both be read from and written to.
3. Attempting to read data from this register when RS = 0 drives the bus to high-impedance state; output data becomes undefined.
4. Write (the specified value – 1) into this register.
5. Valid only in 8-color display modes with horizontal stripes.
6. One character consists of eight horizontal dots.
7. Valid only if the display timing signal is supplied externally.
8. Valid only if the dot clock signal is generated internally.
9. Valid only if the display timing signal is generated internally.

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$\overline{CS}$	RS	PS[1]	Reg. Address 3	2	1	0	Reg. No.	Data Bits 3	2	1	0	
1	—	—	—	—	—	—	—	– [2]				
0	0	—	—	—	—	—	AR					← Address register
0	1	—	0	0	0	0	R0	DIZ	PS	DSP	DCK	← Control register 1
0	1	0	0	0	0	1	R1	MC	DON	MS1	MS0	← Control register 2
0	1	0	0	0	1	0	R2					← Vertical displayed lines register
0	1	0	0	0	1	1	R3					
0	1	0	0	1	0	0	R4					
0	1	0	0	1	0	1	R5					← CL3 period register
0	1	0	0	1	1	0	R6[3]					← Horizontal displayed characters register
0	1	0	0	1	1	1	R7					
0	1	0	1	0	0	0	R8					← CL3 pulse width register
0	1	0	1	0	0	1	R9					← Fine adjust register
0	1	0	1	0	1	0	R10					← PLL frequency-division ratio register
0	1	0	1	0	1	1	R11					
0	1	0	1	1	0	0	R12					← Vertical backporch register
0	1	0	1	1	0	1	R13					
0	1	0	1	1	1	0	R14					← Horizontal backporch register
0	1	0	1	1	1	1	R15					
0	1	1	0	0	0	1	P1[4]	0	0	0	0	← Black palette register
0	1	1	0	0	1	0	P2[4]	0	0	1	0	← Blue palette register
0	1	1	0	0	1	1	P3[4]	0	1	0	1	← Red palette register
0	1	1	0	1	0	0	P4[4]	0	1	1	0	← Magenta palette register
0	1	1	0	1	0	1	P5[4]	0	1	1	1	← Green palette register
0	1	1	0	1	1	0	P6[4]	1	0	0	0	← Cyan palette register
0	1	1	0	1	1	1	P7[4]	1	0	1	0	← Yellow palette register
0	1	1	1	0	0	0	P8[4]	1	0	0	0	← White palette register
0	1	1	1	0	0	1	—	– [5]				← Reserved registers
⋮	⋮	⋮	⋮		⋮							
0	1	1	1	1	1	1	—					

Notes:
1. Corresponds to bit 2 of control register 1 (R0).
2. Invalid bits. Attempting to read data from these bits returns undefined data.
3. The most significant bit is invalid in dual-screen configuration modes.
4. Bit values shown are default values at reset.
5. Reserved bits. Any attempt to write data into the register is invalid, although it has no affect on LSI operations. Any attempt to read data from the register returns undefined data.

Figure 1 Register Bit Assignment

System Description

Figure 2 is a block diagram of a system in which the LVIC-II is used outside a personal computer.

The LVIC-II converts the RGB serial data sent from the personal computer into parallel data and temporarily writes it to the buffer memory. It then reads out the data in order and outputs it to LCD drivers to drive the LCD. In this case, the CRT display dot clock (DOTCLK), which is a latch clock for serial data, is generated by the PLL cricuit from the horizontal synchronization signal (HSYNC). The DOTCLK signal frequency is specified by the PLL frequency-division ratio register (R10, R11).

The system can be configured without a VCO and LPF if the DOTCLK signal is supplied externally, and it can be configured without an MPU if the LVIC-II is controlled by the pin programming method.

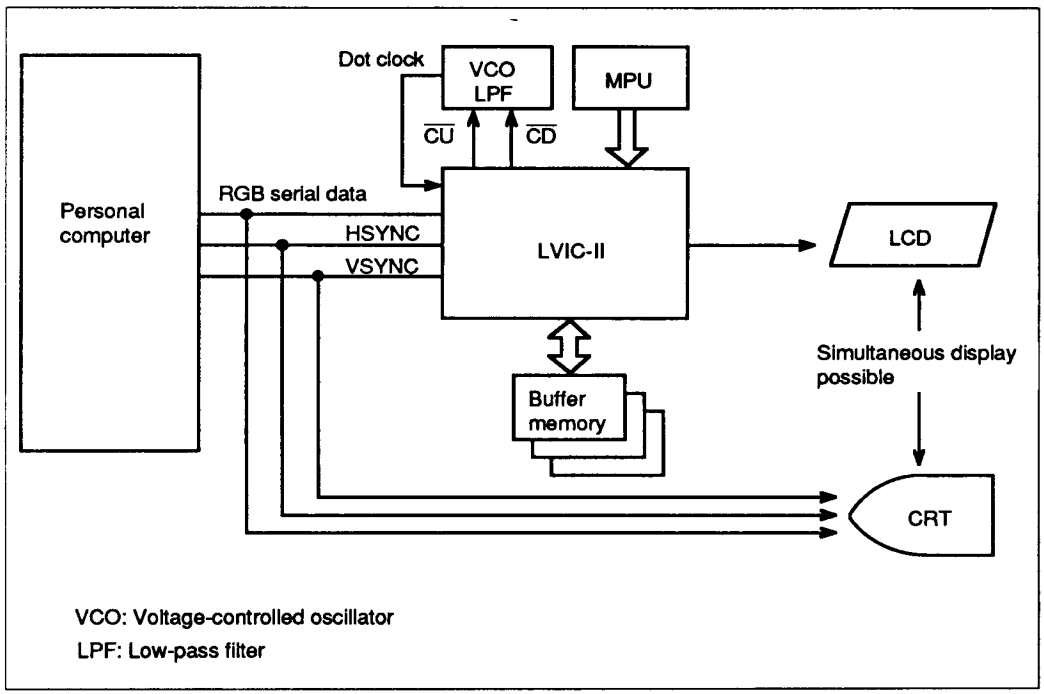

Figure 2 System Block Diagram (with MPU programming method and DOTCLK generated internally)

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Functional Description

Programming Method

One of two methods of controlling LVIC-II functions can be selected by setting pins PMOD0 and PMOD1. Control by pins is called the pin programming method and control by internal registers is called the internal register programming method. The internal register programming method can be further divided into the MPU programming method and the ROM programming method; an MPU is used to write data into internal registers in the MPU programming method and ROM is used to write data into internal registers in the ROM programming method.

Pin Programming Method: The LVIC-II's mode-setting pins control functions.

Internal Register Programming Method: An MPU or ROM is used to write data into the LVIC-II's internal registers to control functions. Figure 3 shows the connection of either an MPU or ROM to the LVIC-II. Although figure 3 (1) shows an example of the use of a 4-bit microprocessor, the LVIC-II can also be connected directly to the host MPU bus since the LVIC-II MPU bus is compatible with the 4-MHz bus of 80-series microcomputers.

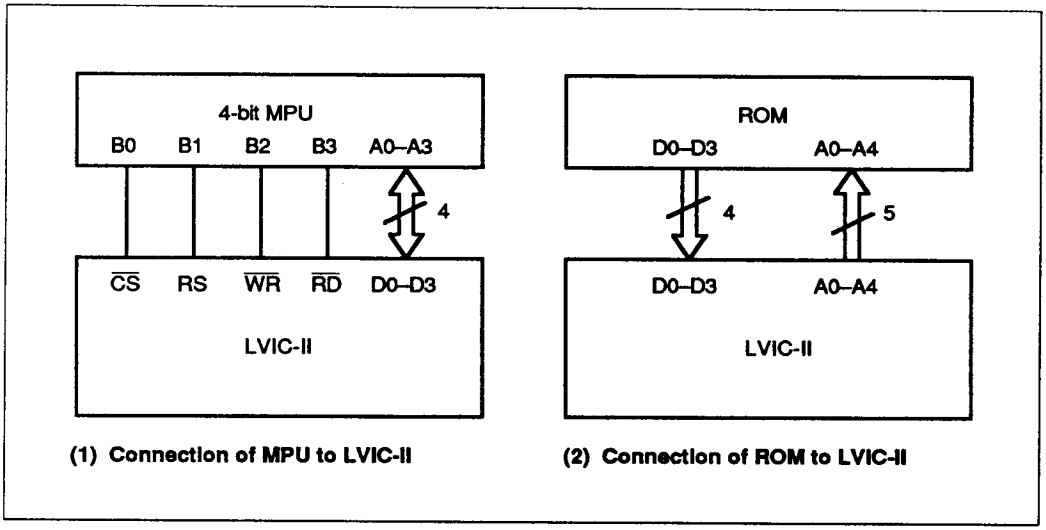

Figure 3 Connection of MPU or ROM to LVIC-II

Screen Size

Screen size can be programmed either by pins or internal registers.

In the pin programming method, either 640 dots or 720 dots (80 characters or 90 characters) can be selected with the XDOT pin as the number of horizontal displayed characters, and either 200, 350, 400, 480, 512, or 540 lines can be selected with the YL2–YL0 pins as the number of vertical displayed lines. The number of vertical displayed lines can be adjusted by from +0 to +15 lines with the ADJ and F3–F0 pins.

In the internal register programming method, any even number of characters from 4 to 506 (from 32 to 4048 dots) can be selected with the horizontal displayed characters register (R6, R7), and any even number of lines from 4 to 1028 can be selected with the vertical displayed lines register (R2, R3, and the high-order two bits of R4). However, note that an odd number of lines can also be selected if the screen configuration is single-screen and Y-drivers (scan drivers) are positioned on one side of the LCD screen.

The relationship between the LCD screen and the pins and internal registers controlling screen size is shown in figure 4.

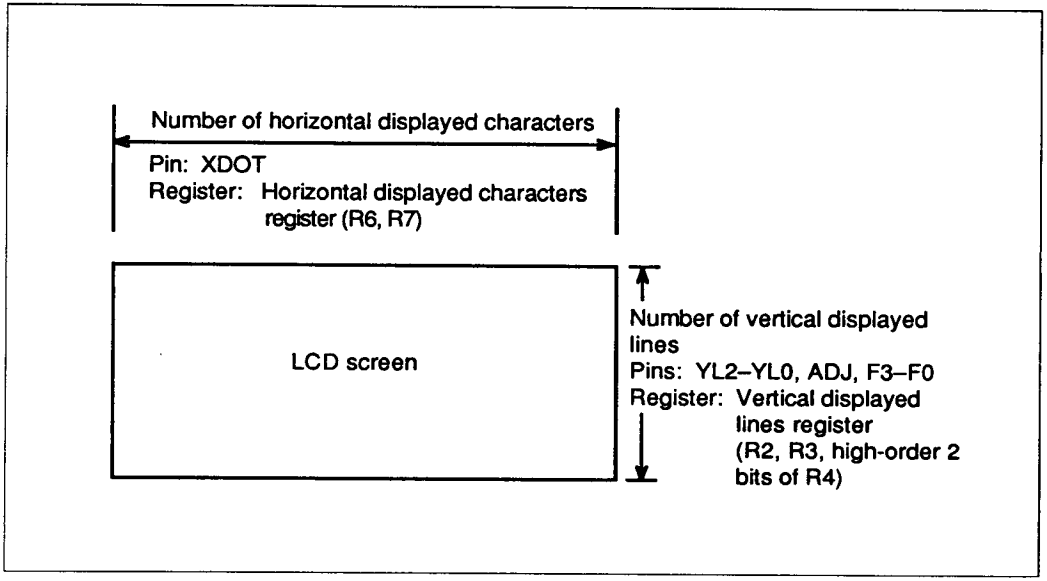

Figure 4 Relationship between LCD Screen and Pins and Internal Registers

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Memory Selection

8-, 32-, or 64-kbytes SRAMs can be selected as buffer memory for the LVIC-II. Since the LVIC-II has a chip select circuit for memory, no external decoder is required. The memory type can be selected with the MS1 and MS0 pins or the MS1 and MS0 bits of control register 2 (R1). Memory types and corresponding pin address assignments are listed in table 7.

The memory capacity required depends on screen size and can be obtained from the following equation:

Memory capacity (bytes) = Nhd × Nvd

Nhd: Number of horizontal displayed characters (where one character consists of 8 horizontal dots)

Nvd: Number of vertical displayed lines

For example, a screen of 640 × 200 dots requires a 16-kbytes memory capacity since 80 characters × 200 lines is 16 kbytes. Consequently, each plane requires two HM6264s (8-kbytes memories) in 8-level gray-scale display modes. The $\overline{MCS0}$ pin must be connected to the $\overline{CS}$ pin of one of the memory chips in each plane, and the $\overline{MCS1}$ pin must be connected to the $\overline{CS}$ pin of the remaining memory chip in each plane (figure 5 (a)).

A screen of 640 × 400 dots requires a 32-kbytes (256-kbit) memory capacity, so each plane requires an HM62256, which is a 32-kbytes memory. In this case, the $\overline{MCS0}$ pin must be connected to the $\overline{CS}$ pin of each memory chip. (figure 5 (b)).

Table 7 Memories and Pin Address Assignments

Pins or Bits					
MS1	MS0	Memory	Address Pins	Chip Select Pins	Address Assignment
0	0	No memory (Note)	—	—	—
0	1	8-kbyte	MA0–MA12	$\overline{MCS0}$	$0000–$1FFF
				$\overline{MCS1}$	$2000–$3FFF
				MA13	$4000–$5FFF
				MA14	$6000–$7FFF
				MA15	$8000–$9FFF
1	0	32-kbyte	MA0–MA14	$\overline{MCS0}$	$00000–$07FFF
				$\overline{MCS1}$	$08000–$0FFFF
				MA15	$10000–$17FFF
1	1	64-kbyte	MA0–MA15	$\overline{MCS0}$	$00000–$0FFFF
				$\overline{MCS1}$	$10000–$1FFFF

Note: There are some limitations if no memory is used. Refer to the User Notes section for details.

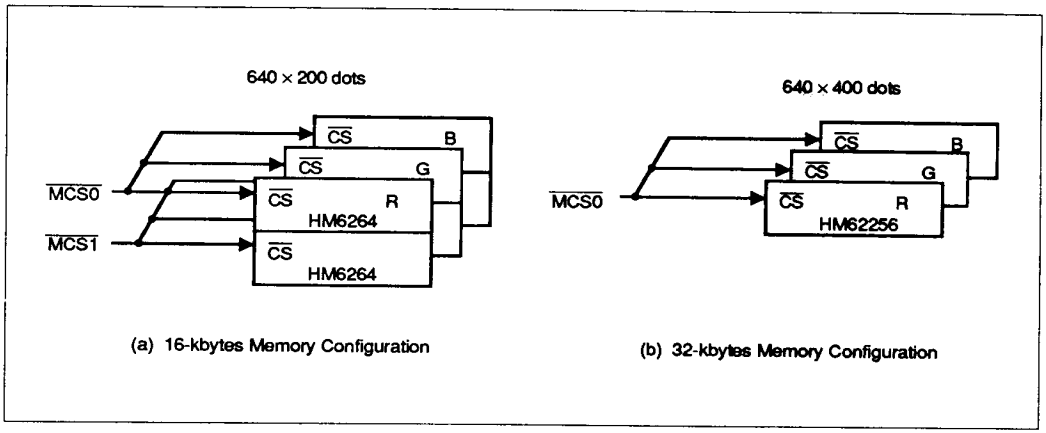

Figure 5 Screen Size and Memory Configuration

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Display Modes

The LVIC-II supports 16 display modes, depending on the states of the DM3–DM0 pins. The display mode controls display color, type of LCD data output, positions of LCD drivers for the LCD screen, arrangement of color data (type of stripes), and method of M signal output (type of alternation signal). Display modes are listed in table 8.

Table 8 Display Mode List

Mode No.	Pins DM3	DM2	DM1	DM0	Display Color	Data Transfer Type	Screen Config.	LCD Driver Positions X-driver[2]	Y-Driver[3]	Stripe[4]	Alternation
1	0	0	0	0	Mono-chrome	4-bit	Dual	One side	One side	—	Every frame
2	0	0	0	1			Single				
3[1]	0	0	1	0					Both sides		
4	0	0	1	1		8-bit			One side		
5[1]	0	1	0	0					Both sides		
6	0	1	0	1	8-level gray scale	4-bit	Dual		One side		
7	0	1	1	0			Single				
8	0	1	1	1		8-bit					
9[1]	1	0	0	0	8-color	12-bit (4 bits each for R, G, and B)	Single	One side	Onse side	Vertical	Every line
10[1]	1	0	0	1					Both sides		
11[1]	1	0	1	0				Both sides	One side		
12[1]	1	0	1	1					Both sides		
13[1]	1	1	0	0				One side	One side	Horizontal	
14[1]	1	1	0	1					Both sides		
15[1]	1	1	1	0				Both sides	One side		
16	1	1	1	1			Dual	One side		Vertical	Every frame

Notes: 1. For TFT-type LCDs.
2. Data output driver.
3. Scan driver.
4. Refer to the 8-color Display section.

Display Color

The LVIC-II converts the RGB color data normally used for CRT display into monochrome, 8-level gray-scale, or 8-color display data.

Monochrome Display (Modes 1 to 5): The LVIC-II displays two colors: black (display on) and white (display off). As shown in table 9, the CRT display RGB data is ORed to determine display on/off.

8-Level Gray Scale Display (Modes 6 to 8): The LVIC-II thins out data on certain lines or dots to provide an 8-level gray-scale display based on CRT display color (luminosity). The relationship between CRT display color (luminosity) and LCD gray scale (contrast) is shown in table 10.

This relationship corresponds to the default values in palette registers; the correspondence between color and gray scale can be changed by writing data into palette registers.

8-Color Display (Modes 9 to 16): The LVIC-II displays 8 colors through red (R), green (G), and blue (B) filters placed on liquid-crystal cells. The eight colors are the same as those provided by a CRT display. As shown in figure 6, 8-color display has two stripe modes: horizontal stripe mode in which the LVIC-II arranges RGB data horizontally for horizontal filters and vertical stripe mode in which it arranges RGB data vertically for vertical filters. Three cells express one dot in both modes.

Table 9 Monochrome Display

CRT Display Data				LCD	
R	G	B	CRT Display Color	On/Off	Color
1	1	1	White	On	Black
1	1	0	Yellow	On	Black
0	1	1	Cyan	On	Black
0	1	0	Green	On	Black
1	0	1	Magenta	On	Black
1	0	0	Red	On	Black
0	0	1	Blue	On	Black
0	0	0	Black	Off	White

Table 10 8-Level Gray-Scale Display

CRT Display Data			CRT		LCD	
R	G	B	Color	Luminosity	Gray Scale	Contrast
1	1	1	White	High	Black	Strong
1	1	0	Yellow	↑	↑	↑
0	1	1	Cyan	↑	↑	↑
0	1	0	Green	↑	↑	↑
1	0	1	Magenta	↑	↑	↑
1	0	0	Red	↑	↑	↑
0	0	1	Blue	↑	↑	↑
0	0	0	Black	Low	White	Weak

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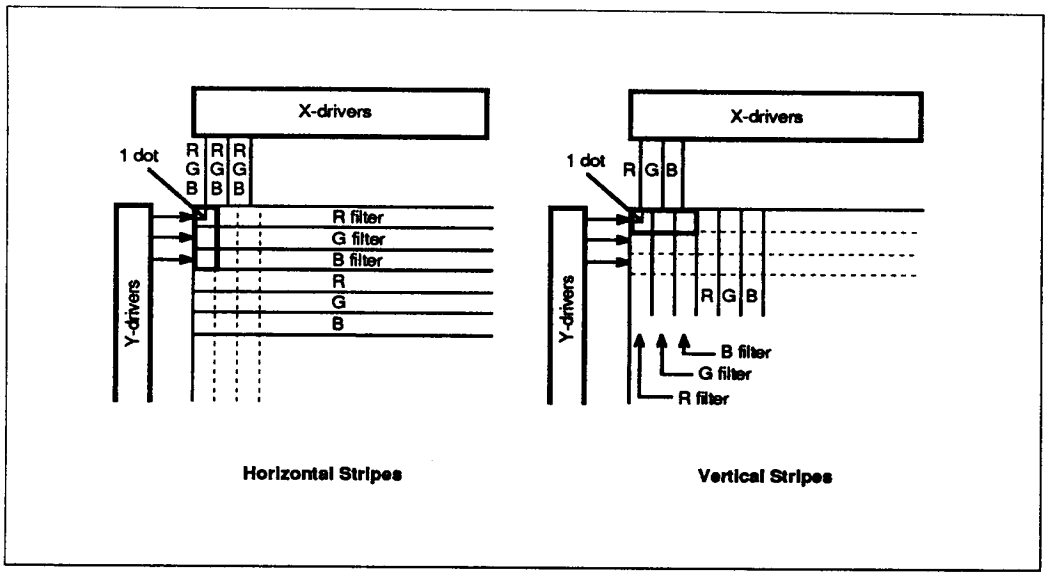


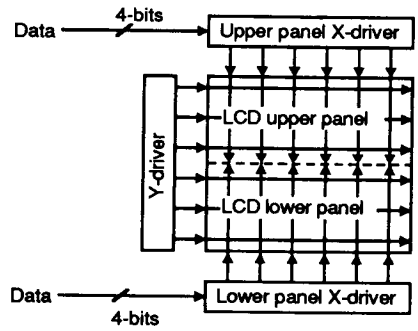
Figure 6 Stripe Modes in 8-Color Display

LCD System Configuration

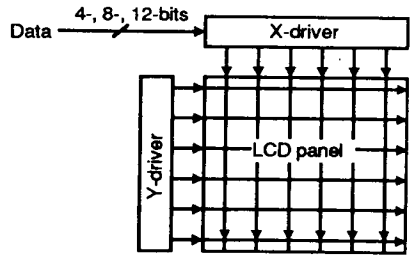
The LVIC-II supports the following LCD system configurations:

- Types of LCD data output:
  - Data transfer: 4-bit, 8-bit, or 12-bit (4 bits each for R, G, and B)
  - Screen configuration: Single or dual
- LCD driver positions around LCD screen:
  - X-drivers: On one side or on both sides
  - Y-drivers: On one side or on both sides

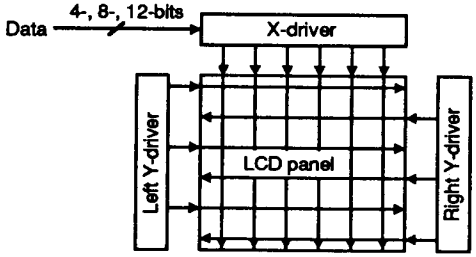
System configurations for different modes are shown in figure 7, and configurations of X- and Y-drivers positioned on both sides of an LCD screen are shown in figure 8.



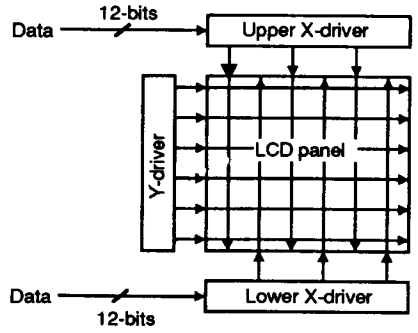
System configuretion for mode 1 and mode 6 (4-bit data transfer, dual screen, X-driver and Y-driver each on one side) Note



System configureation for modes, 2, 4, 7, 8, 9, and 13 (4-, 8-, or 12-bit data transfer, single screen, X-driver and Y-driver each on one side)



System configureaton fo rmodes 3, 5, 10, and 14 (4-, 8-, or 12-bit data transfer, single screen, X-driver on one side and Y-driver on both sides)



System configureation for mode 11 and mode 15 (12-bit data transfer, single screen, X-edriver on both sides and Y-driver on one side)

Note: Since the LCD upper panel and lower panel are each regarded as one screen, the X-drivers are considered to be positioned on one side, not on both sides.

Figure 7 System Configurations by Mode

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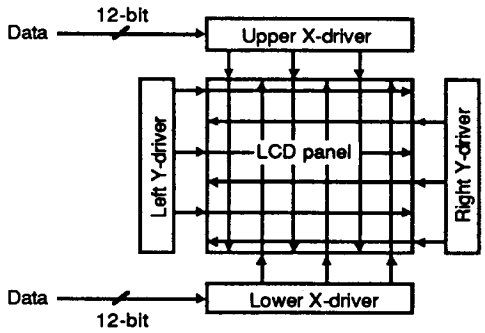
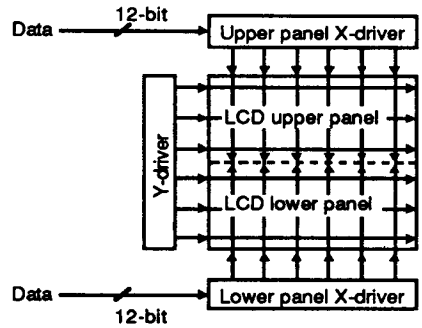


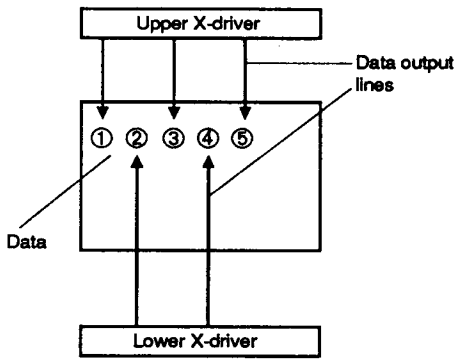
System configuration for mode 12 (12-bit data transfer, single screen, X-driver and Y-driver each on both sides)



System configuration for mode 16 (12-bit data transfer, dual screen, X-driver and Y-driver each on one side)Note

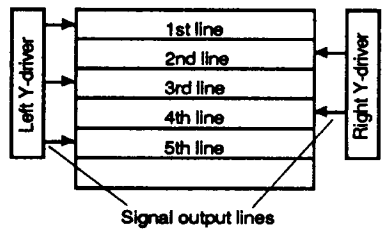
Note: Since the LCD upper panel and lower panel are each regarded as one screen, the X-drivers are considered to be positioned on one side, not on both sides.

Figure 7 System Configurations by Mode (cont)



(1) X-drivers set on both sides

Data output lines run alternately from upper and lower X-drivers, increasing the pitch of the lines to twice that for X-drivers positioned on one side.



(2) Y-drivers set on both sides

Line select signal output lines run alternately from right and left Y-drivers, increasing the pitch of the lines to twice that for Y-drivers positioned on one side.

Figure 8 X- and Y-Drivers Set on Both Sides

LDOTCK Frequency Calculation

The frequency f_L of the LCD dot clock (LDOTCK) can be obtained from the following equation:

$f_L = (Nhd + 6) \times 8 \times Nvd \times f_F$

Nhd: Number of horizontal displayed characters on LCD = (number of horizontal displayed dots on LCD) × 1/8
Nvd: Number of vertical displayed lines on LCD
f_F: Frame frequency (FLM frequency)

In this case, f_L must satisfy the following relationships, where f_D is the frequency of the dot clock for CRT display (DOTCLK):

$f_L < f_D \times 15/16$ or

$f_L = f_D$ (the phase of LDOTCK must be opposite to that of DOTCLK in this case)

Display Timing Signal Generation

CRT display data is divided into display period data and retrace period data, so the LVIC-II needs a signal indicating whether the CRT display data that has just been transferred is display period data or not. This signal is called the display timing signal.

The LVIC-II can generate the display timing signal from the HSYNC and VSYNC signals. The relationships between HSYNC, VSYNC, the display timing signal (DISPTMG), and display data are shown in figure 9. Y lines and X dots in the figure are specified by the vertical backporch register (R12, R13) and the horizontal backporch register (R14, R15), respectively.

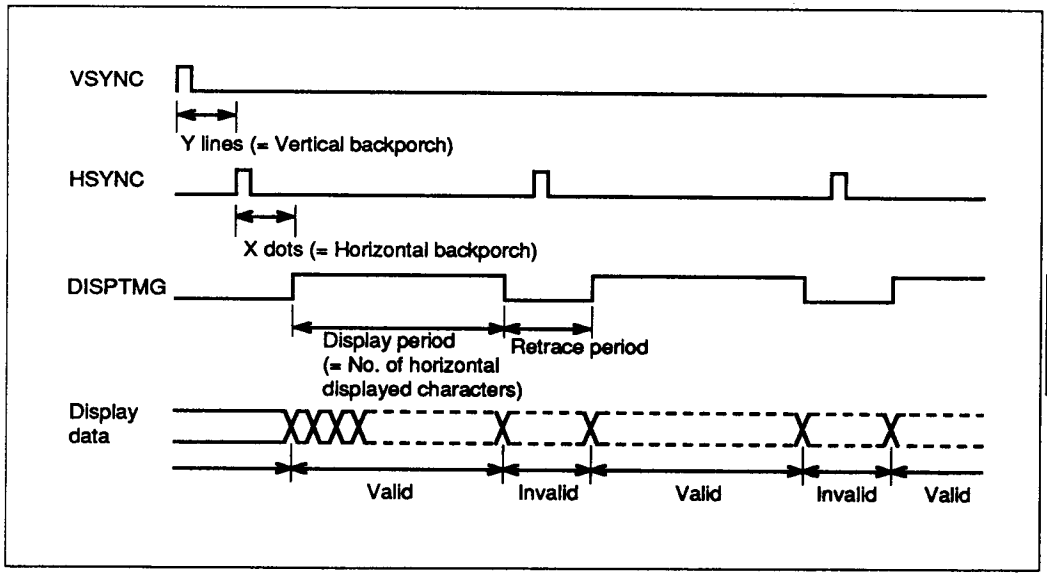


Figure 9 Relationships between HSYNC, VSYNC, DISPTMG, and Display Data

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Dot Clock Generation

The dot clock, which is a data latch clock, is not a standard video signal, so it is not usually output from the CRT display plug. Therefore, the LVIC-II must generate it. The LVIC-II has a programmable counter and a phase comparator which are parts of a phase-locked loop (PLL) circuit, and it can generate the dot clock from the HSYNC signal if a charge pump, a low-pass filter (LPF), and a voltage-controlled oscillator (VCO) are externally attached.

A block diagram of the PLL circuit is shown in figure 10. A PLL circuit is a feedback controller that generates a clock whose frequency and phase are the same as those of a basic clock. The basic clock is the HSYNC signal in this case.

At power-on, the VCO outputs to the programmable counter a signal whose frequency is determined by the voltage at that time. The counter divides the frequency of the signal according to the value in the PLL frequency-division ratio register (R10, R11), and outputs it to the phase comparator. This is the frequency-divided clock.

The comparator compares the edges of the clock pulses and the HSYNC signal pulses and outputs the $\overline{CU}$ or $\overline{CD}$ signal to the charge pump and LPF according to the result. The comparator outputs the $\overline{CU}$ signal if the frequency of the clock is lower than that of the HSYNC signal or if the phase of the clock is behind that of the HSYNC signal; otherwise it outputs the $\overline{CD}$ signal. The charge pump and LPF apply a voltage to the VCO according to the $\overline{CU}$ or $\overline{CD}$ signal.

This operation is repeated until the phase and frequency of the frequency-divided clock match those of the HSYNC signal, making it a stable dot clock.

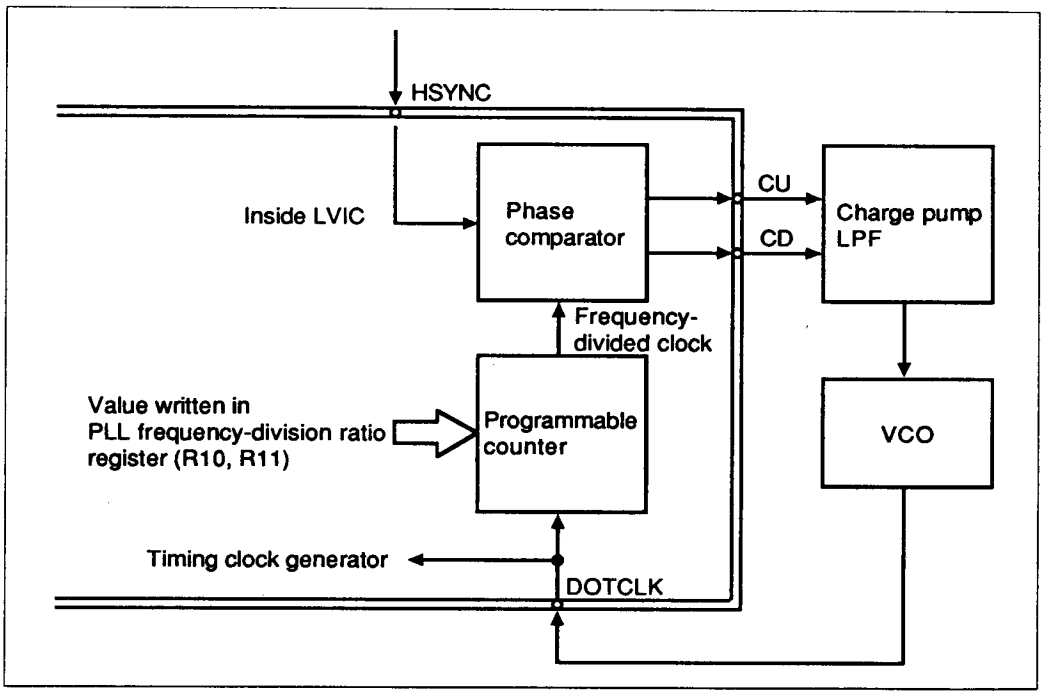

Figure 10 PLL Circuit Block Diagram

Gray-Scale Palette

The HD66841F thins out LCD data on certain dots or lines of an LCD panel every frame, changing integral voltages applied to liquid-crystal cells, to generate intermediate levels of luminosities. Consequently, the difference in depth between adjacent gray-scale shades may not be uniform in some cases since voltage-transmittance characteristics vary with different panels. To allow for this, the HD66841F is designed to generate 13 gray-scale levels and provide palette registers that assign desired levels to certain of the eight CRT display colors.

The relationships between gray scales and corresponding effective applied voltages are shown in figure 11 (a). Each gray scale is displayed according to the characteristics of its effective applied voltage and the optical transmittance of the panel (figure 11 (b)). Using the palette registers to select any 8 out of 13 levels of applied voltages enables an optimal gray-scale display conforming to the characteristics of the LCD panel. The palette registers can also be used to provide 4-level gray-scale display and reverse display.

Table 11 Default Values of Palette Registers

Register No.	CRT Display Data R	G	B	Register Name	Default Value			
P1	0	0	0	Black palette	0	0	0	0
P2	0	0	1	Blue palette	0	0	1	0
P3	1	0	0	Red palette	0	1	0	1
P4	1	0	1	Magenta palette	0	1	1	0
P5	0	1	0	Green palette	0	1	1	1
P6	0	1	1	Cyan palette	1	0	0	0
P7	1	1	0	Yellow palette	1	0	1	0
P8	1	1	1	White palette	1	1	0	0

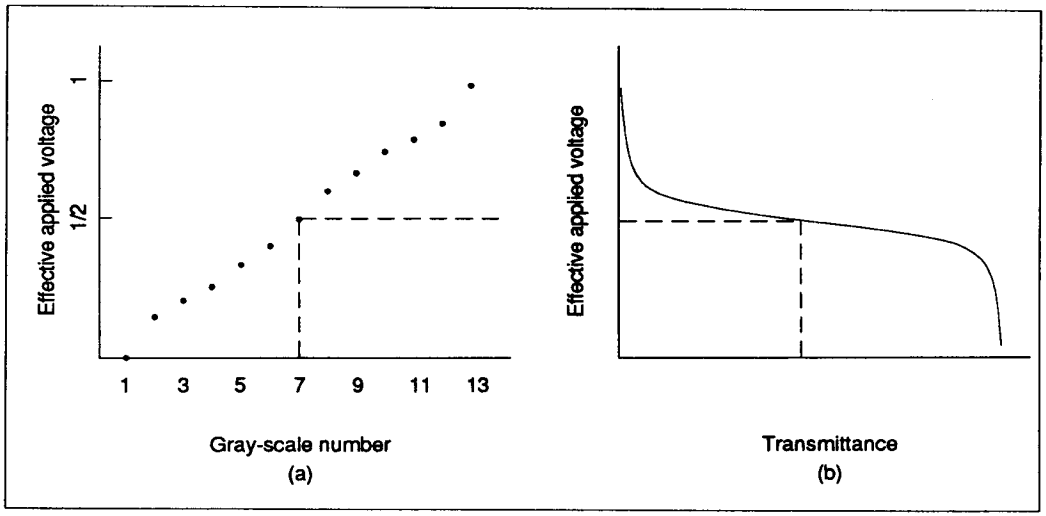

Figure 11 Relationships between Gray Scale, Transmittance, and Effective Applied Voltage

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Pin Programming Method

The palette registers cannot be used in the pin programming method.

MPU Programming Method

To change the contents of palette registers in the MPU programming method, set bit 2 (the PS bit) of control register 1 (R0), to 1. Since data registers (R1–R15) cannot be accessed while this bit is 1, set in to 0 before accessing the data registers again. However, note that control register 1 (R0) can be accessed regardless of the setting of the PS bit if $0 is set in the address register (AR).

ROM Programming Method

In the ROM programming method, the HD66841F accesses ROM sequentially from address $0000 to $001F. In this case, write 0 to bit 2 of address $0000 (PS bit) before writing data register values to addresses $0001–$000F, and write 1 to bit 2 of address $0010 (PS bit) before writing palette register values to addresses $0011–$0018.

DIZ Function

The HD66841F thins out data on certain lines or dots every frame to enable gray-scale display. If a checker-board pattern consisting of alternately arranged gray scales of different levels (figure 12) is displayed by a simple dot-basis gray-scale display control method, the display might sometimes seem to "flow" horizontally, depending on the gray-scale and LCD panel characteristics.

The HD66841F automatically checks for such a checker-board section and changes the gray-scale display control method of dot-based data thinning to that of frame-based data thinning, to reduce display flow. Setting bit 3 (DIZ) of control register 1 (R0) to 1 enables this function. In frame-based data thinning, however, flickering might appear with some LCD panels; in that case, select the control method that generates the better display.

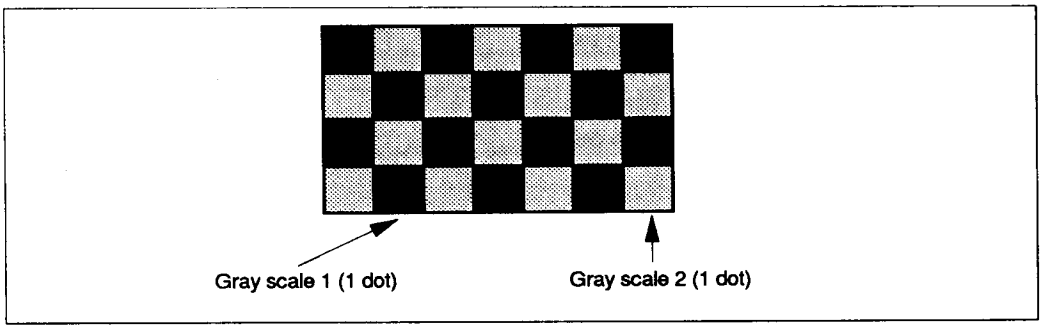

Figure 12 Checker-Board Display

Double-Height Display

The LVIC-II provides double-height display which doubles the vertical size of characters and pictures (figure 13).

In the TN-type LCD modes (display modes 1, 2, 4, and 6-8), the CL3 signal period is half as long as the CL1 signal period, as shown in figure 14. Consequently, using the CL3 signal instead of the CL1 signal (figure 15) as a line shift clock enables two lines to be selected while X-drivers (data output drivers) are outputting identical data, thus realizing double-height display. However, it should be noted that this display requires the following procedure since the LVIC-II displays twice as many lines as specified by pins or internal registers:

1. Halve the LCD dot clock (LDOTCK) frequency calculated from the number of vertical displayed lines of the LCD panel.

2. Specify half the number of vertical displayed lines of the LCD panel as the number of vertical displayed lines. (For instance, if the number of vertical displayed lines of the LCD panel is 400, specify 200 with the YL2–YL0 pins or the vertical displayed lines register.)

This function is available only in the TN-type LCD modes; it is disabled in the TFT-type LCD modes.

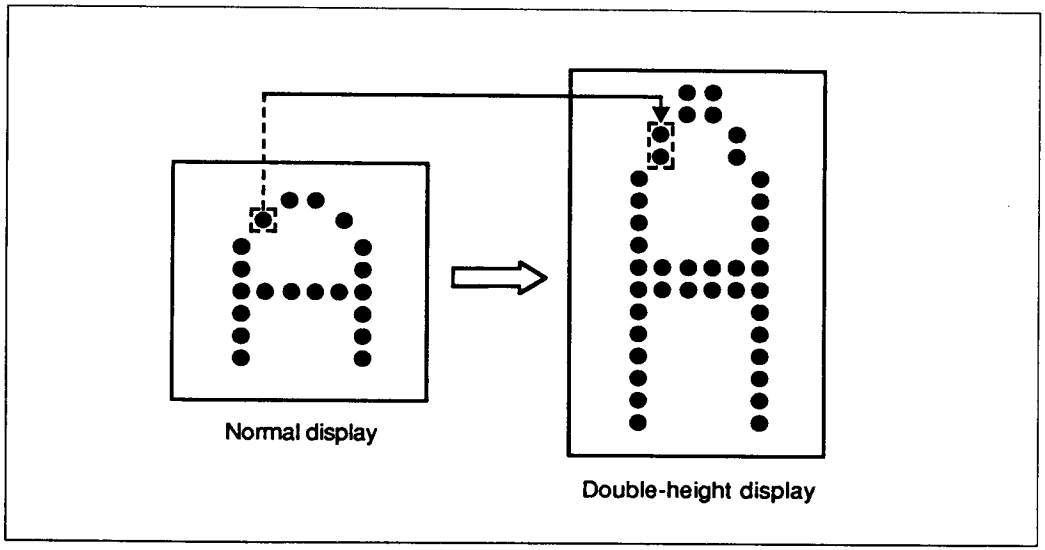

Figure 13 Double-Height Display Example

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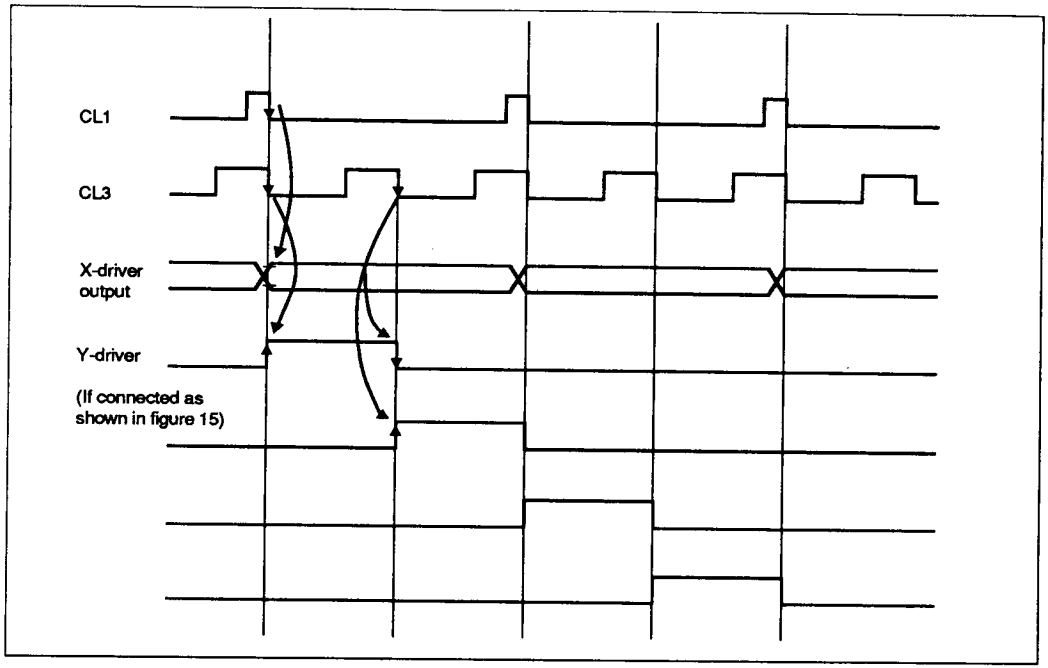

Figure 14 Relationship between CL1 and CL3 in Modes 1, 2, 4, 6, 7, and 8

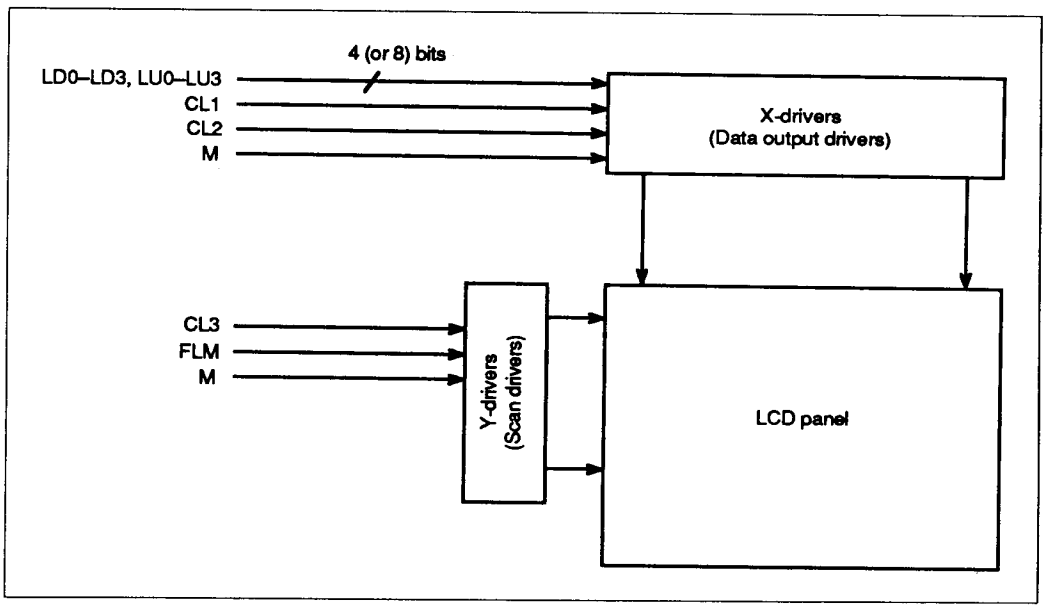

Figure 15 Connection for Double-Height Display

Display Timing Signal Fine Adjustment

If the display timing signal is supplied externally, a phase shift between CRT data and the display timing signal may appear. This is because each signal has its own specific lag. The LVIC-II can adjust the display timing signal according to pins F0–F3 or the fine adjust register (R9) to correct the phase shift.

The relationships between pins F3–F0, data bits 3 to 0 of the fine adjust register, and the resultant fine adjustments are shown in table 12. The polarity of the number of dots adjusted is given by – (minus) indicating advancing the phase of the display timing signal or + (plus) indicating delaying it. Pin F3 or data bit 3 of R9 selects the polarity. The adjustment reference point is the display start position.

Examples of adjusting the display timing signal are shown in figure 16. Since the signal is two dots ahead of the display start position in case (1), F3, F2, F1, and F0 or data bits 3, 2, 1, and 0 of R9 should be set to (1, 0, 1, 0) to delay the signal by two dots. Conversely, since the signal is two dots behind the display start position in case (2), they should be set to (0, 0, 1, 0) to advance the signal by two dots. If there is no need to adjust the signal, a setting of either (0, 0, 0, 0) or (1, 0, 0, 0) will do.

Table 12 Pins, Data Bits of R9, and Fine Adjustment

Pin	F3	F2	F1	F0	Number of Dots
R9 Bit	3	2	1	0	Adjusted
	0	0	0	0	0
		0	0	1	–1
		⋮	⋮	⋮	⋮
		1	1	0	–6
		1	1	1	–7
	1	0	0	0	0
		0	0	1	+1
		⋮	⋮	⋮	⋮
		1	1	0	+6
		1	1	1	+7

Note: To use pins to adjust the display timing signal, set the ADJ pin to 1.

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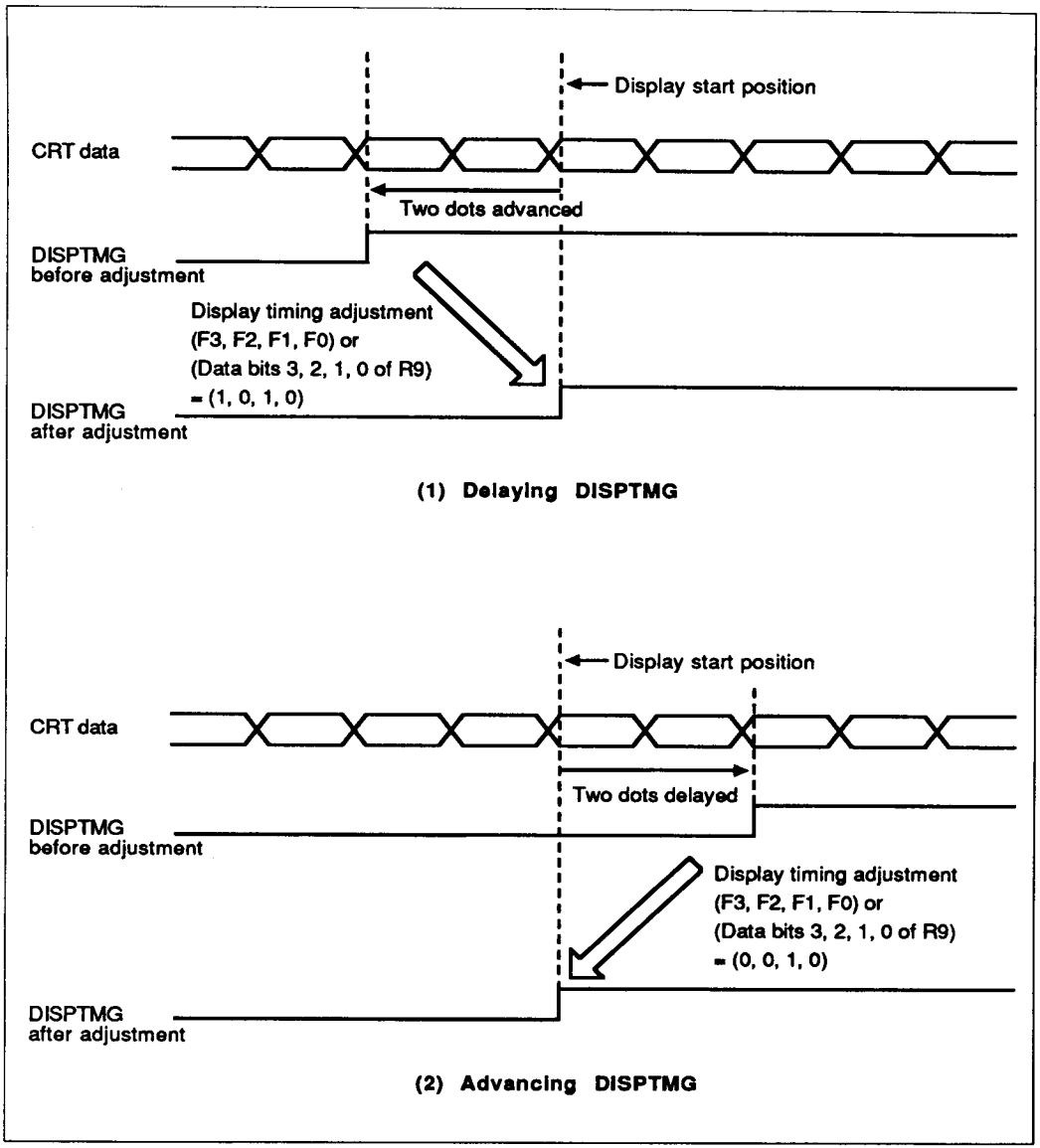

Figure 16 Adjustment of Display Timing Signal

Internal Registers

The HD66841F has an address register (AR), 16 data registers (R0–R15), and 8 palette registers (P1–P8). Write the address of a register to be used into the address register (AR), but only after setting the PS bit of control register 1 (R0) to 0 for a data register or 1 for a palette register. The MPU transfers data to the register corresponding to the written address.

Registers are valid only in the internal register programming method, they are invalid (don't care) in the pin programming method.

The 4-bit address register (figure 17) is used to select one of the 16 data registers or 8 palette registers. It can select any data register or palette register according to the register address written to it by the MPU. The addres register itself is selected if the RS signal is set low.

Control register 1 (figure 18) is composed of four bits whose functions are described below.

- DIZ bit: Changes the method used to control the gray-scale display of a checker-board pattern.
  - DIZ = 0: Data thinned out on a dot basis every frame
  - DIZ = 1: Data thinned out on a frame basis every frame
- PS bit: Specifies access to data registers (R0–R15) or palette registers (P1–P8).

  In MPU programming mode:
  - PS = 0: Specifies access to data registers (R0–R15) only.
  - PS = 1: Specifies access to palette registers (P1–P8) only.

Address Register (AR)

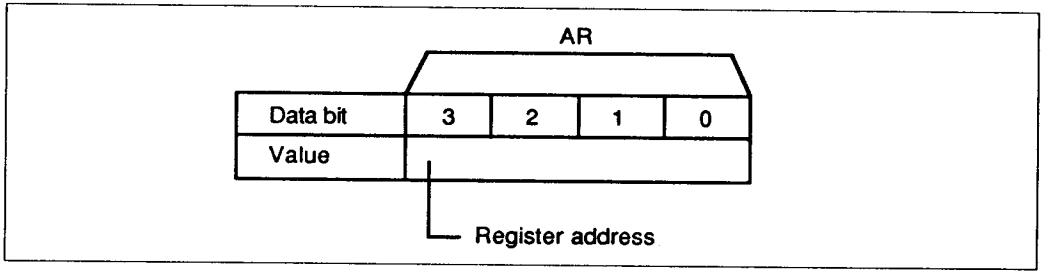

Figure 17 Address Register

Control Register 1 (R0)

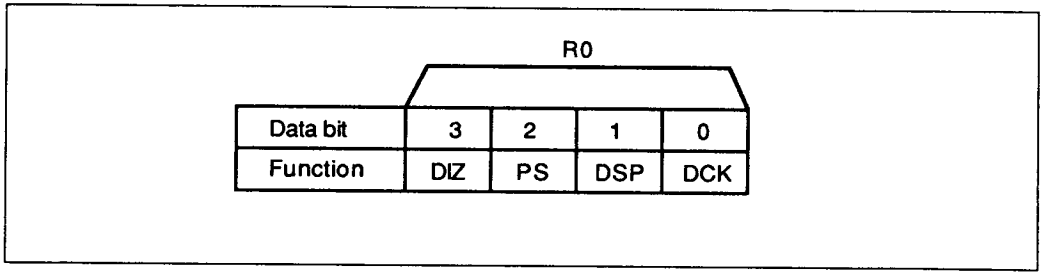

Figure 18 Control Register 1

This register can be always accessed regardless of the PS bit setting, but it cannot be read after the PS bit is set to 1. Read it when PS is 0.

In ROM programming mode: Data for LVIC-II internal data registers can be written into $0001 to $000F when bit 2 (the PS bit) of $0000 is set to 0. Data to be set into palette registers can be written into $0011 to $0018 when the PS bit of $0010 is set to 1 (figure 19 (a)).

- DSP bit
  - DSP = 1: The DISPTMG signal is generated internally.
  - DSP = 0: The DISPTMG signal is supplied externally. (However, note that if DCK is 1, the DISPTMG signal is generated internally even if DSP is 0.)
- DCK bit
  - DCK = 1: The DOTCLK signal is generated internally.
  - DCK = 0: The DOTCLK signal is supplied externally.

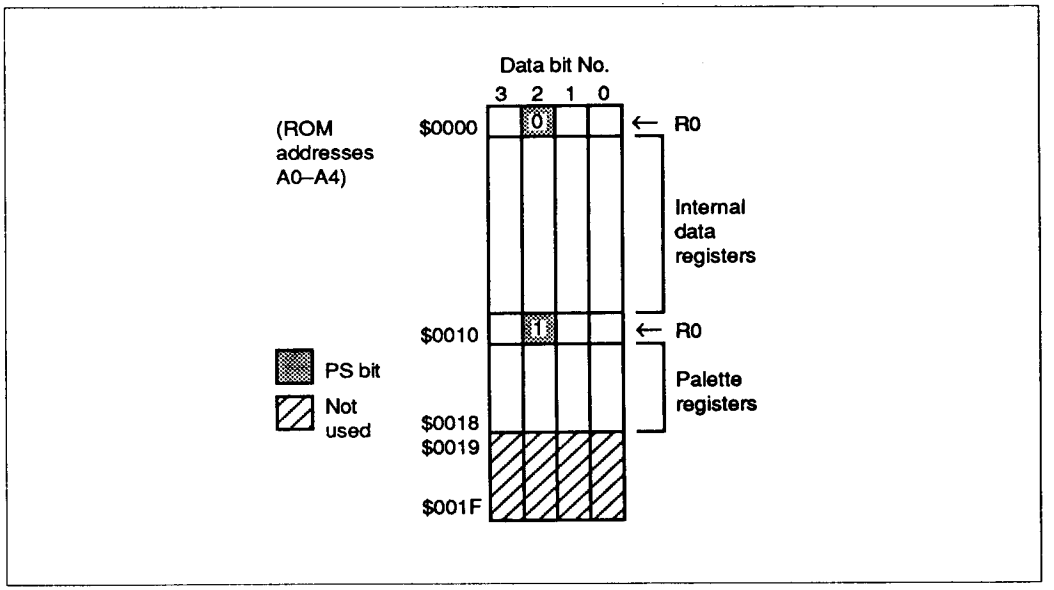

Figure 19 PS Bit Functions in ROM Programming Method

Control Register 2 (R1)

Control register 2 (figure 20) is composed of four bits whose functions are described below.

- MC bit: Specifies M signal alternation.
  - MC = 1: The M signal alternates every line.
  - MC = 0: The M signal alternates every frame.

- DON bit: Specifies whether the LCD is on or off.
  - DON = 1: LCD on
  - DON = 0: LCD off

- MS1, MS0 bits: Specify buffer memory type.
  - (MS1, MS0) = (0, 0): No memory
  - (MS1, MS0) = (0, 1): 8-kbytes memory
  - (MS1, MS0) = (1, 0): 32-kbytes memory
  - (MS1, MS0) = (1, 1): 64-kbytes memory

Vertical Displayed Lines Register (R2, R3, High-Order 2 Bits of R4)

The vertical displayed lines register (figure 21) is composed of ten bits (R2, R3, and the high-order two bits of R4). It specifies the number of lines displayed from top to bottom of the screen, called the number of vertical displayed lines. This register can specify both even and odd numbers in single screen modes with Y-drivers positioned on one side, i.e., in display modes 2, 4, and 7–9, but can specify only even numbers in other modes. The value to be written into this register is Nvd – 1, where Nvd is the number of vertical displayed lines.

CL3 Period Register (Low-Order 2 Bits of R4, R5)

The CL3 period register (figure 21), is composed of six bits (R5 and the low-order two bits of R4). It specifies the CL3 signal period in 8-color display modes with horizontal stripes (display modes 13–15), so it is invalid in other modes. CL3 is the clock signal used by the LVIC-II to output RGB data separately to LCD drivers. The value to be written into this register is Npc – 1, i.e., (Nhd + 6) × 1/3 – 1, where Nhd is the number of horizontal displayed dots × 1/8. If (Nhd + 6) is not divisible by 3, round it off.

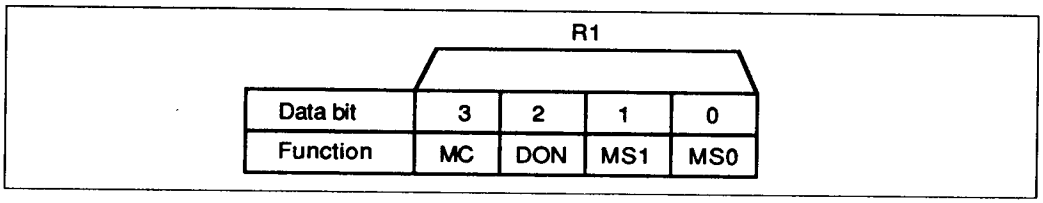

Figure 20 Control Register 2

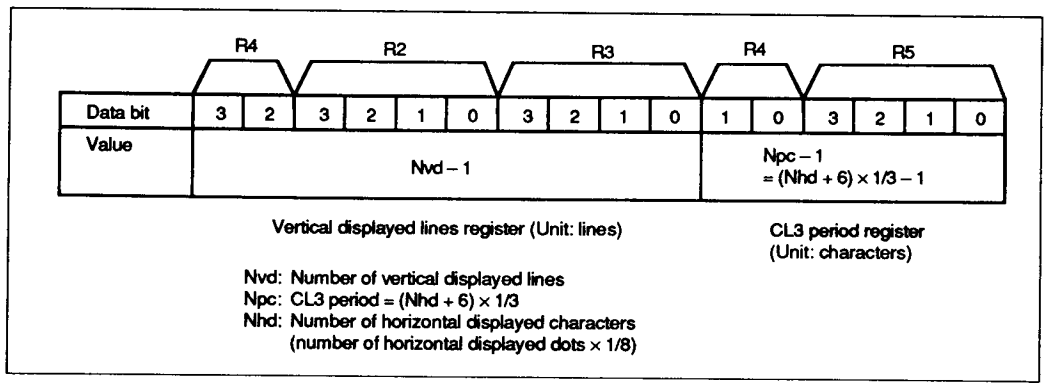

Figure 21 Vertical Displayed Lines Register and CL3 Period Register

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Horizontal Displayed Characters Register (R6, R7)

The horizontal displayed characters register (figure 22) is composed of eight bits (R6, R7). It specifies the number of characters displayed on one horizontal line, called the number of horizontal displayed characters.

This register can specify even numbers only. In dual-screen modes (display modes 1, 6, and 16), the most significant bit of this register is invalid. When writing into this register, shift (Nhd – 1) in the low-order direction for one bit to cut off the least significant bit. Figure 23 shows how to write a value into the register when Nhd = 90.

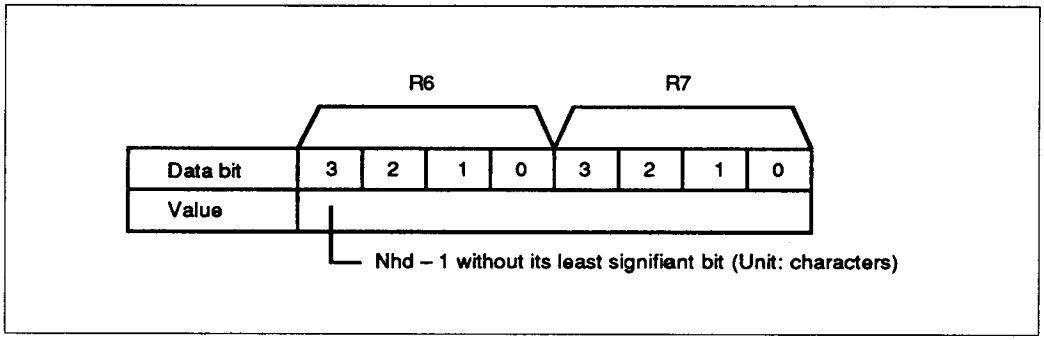

Figure 22 Horizontal Displayed Characters Register

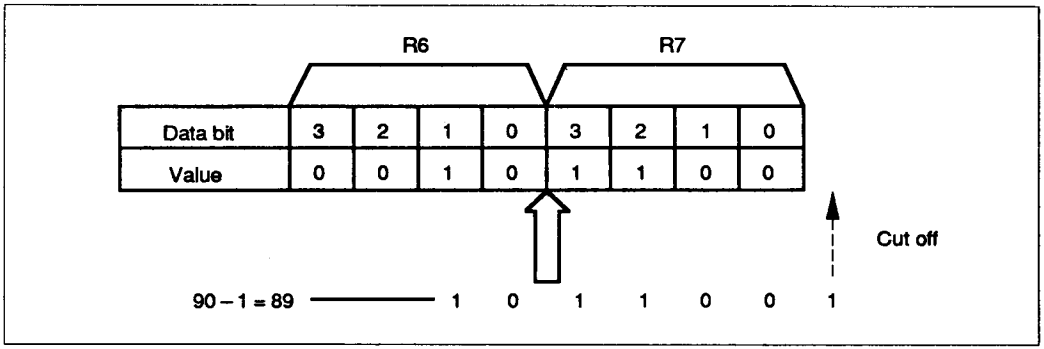

Figure 23 How to Write the Number of Horizontal Displayed Characters

CL3 Pulse Width Register (R8)

The 4-bit CL3 pulse width register (figure 24) specifies the high-level pulse width of the CL3 signal. In TFT-type LCD modes, a data hold time is necessary and it is determined by the high-level pulse width of the CL3 signal. The CL3 signal is output with the high-level pulse width specified by this register even when the LVIC-II is not in a TFT-type LCD mode.

Fine Adjust Register (R9)

The 4-bit fine adjust register (figure 25) adjusts the externally supplied display timing signal (DISPTMG) to synchronize its phase with that of LCD data. The value to be written into this register depends on the interval between the rising edge of the DISPTMG signal and the display start position. For more details, refer to the Display Timing Signal Fine Adjustment section and table 12. This register is invalid if the DISPTMG signal is generated internally, that is, if either the DCK bit or the DSP bit of control register 1 (R0) is 1.

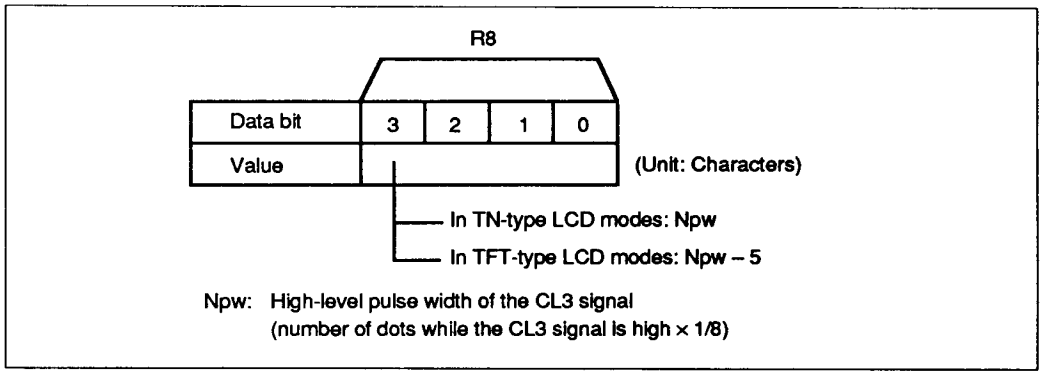

Figure 24 CL3 Pulse Width Resister

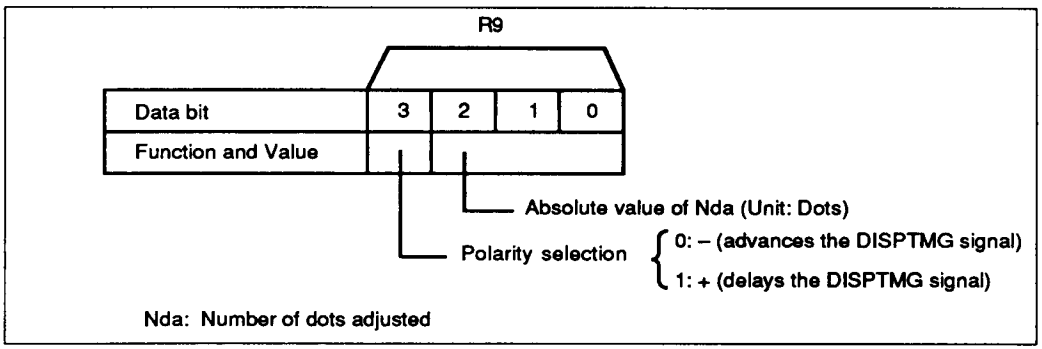

Figure 25 Fine Adjust Register

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PLL Frequency-Division Ratio Register (R10, R11)

The 8-bit PLL frequency-division ratio register (figure 26) specifies the PLL frequency-division ratio used for generating dot clock pulses by a PLL circuit. The PLL frequency-division ratio is the ratio of the DOTCLK signal's frequency to the horizontal synchronization signal's (HSYNC) frequency. The LVIC-II generates the DOTCLK signal according to this ratio. This register is invalid if the DOTCLK signal is supplied externally, i.e., it is valid only in the internal register programming method when the DCK bit of control register 1 (R0) is 0.

The value to be written into this register is $N_{PLL} - 731$, where N_{PLL} is the PLL frequency-division ratio which can be obtained from the following equation:

$N_{PLL} - 731 = Ncht \times n - 731$

Ncht: Total number of horizontal characters on CRT (Total number of horizontal dots on CRT × 1/n)

n: Horizontal character pitch (number of horizontal dots making up a character)

Ncht can be also obtained from the CRT monitor specifications as follows;

Ncht = 1/n × (DOTCLK frequency/HSYNC frequency)

Vertical Backporch Register (R12, R13)

The 8-bit vertical backporch register (figure 27) specifies the vertical backporch which is the number of lines between the active edge of the vertical synchronization signal (VSYNC) and the rising edge of the display timing signal (DISPTMG), if the DISPTMG signal is generated internally. For details on the vertical backporch, refer to the Display Timing Signal Generation section and figure 9.

This register is invalid if the DISPTMG signal is supplied externally. It is valid only in the internal register programming method when the DSP bit of control register 1 (R0) is 1. However, note that if the DCK bit of control register 1 (R0) is 1, the DISPTMG signal will always be generated internally so this register is enabled even if the DSP bit of control register 1 (R0) is 0.

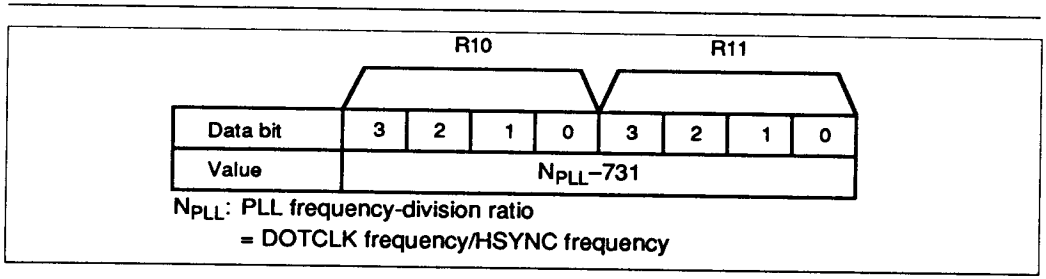

Figure 26 PLL Frequency-Division Ratio Register

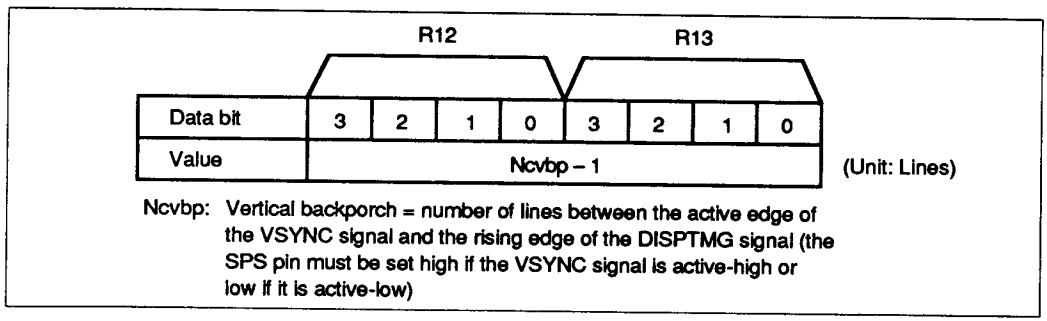

Figure 27 Vertical Backporch Register

Horizontal Backporch Register (R14, R15)

The 8-bit horizontal backporch register (figure 28) specifies the horizontal backporch which is the number of dots between the rising edge of the HSYNC signal and that of the display timing signal (DISPTMG), if the DISPTMG signal is generated internally. For details on the horizontal backporch, refer to the Display Timing Signal Generation section and figure 9.

This register is invalid if the DISPTMG signal is supplied externally. It is valid only in the internal register programming method when the DSP bit of control register 1 (R0) is 1. However, note that if the DCK bit of control register 1 (R0) is 1, the DISPTMG signal will always be generated internally so this register is enabled even if the DSP bit of control register 1 (R0) is 0.

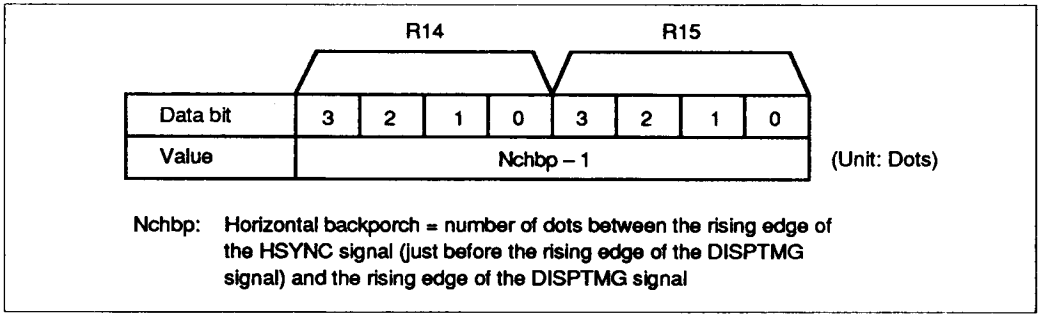

Figure 28 Horizontal Backproch Registers

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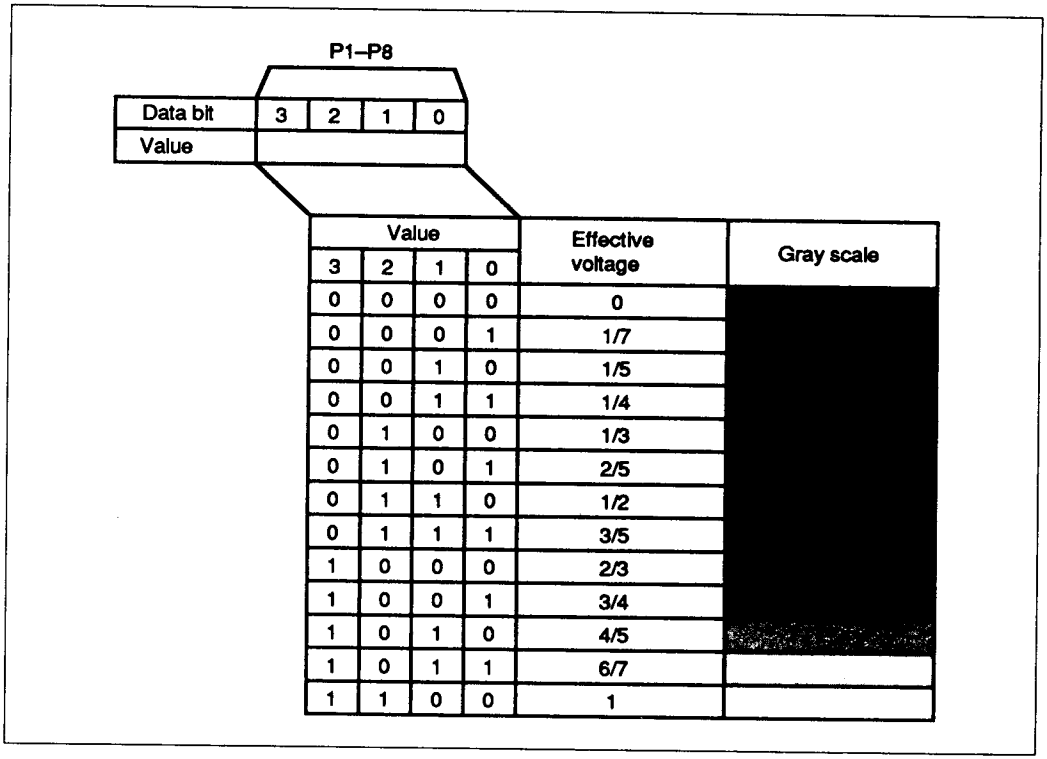
Palette Registers (P1–P8)

The eight 4-bit palette registers (figure 29) each specify one of 13 gray-scale levels for one of the eight colors provided by RGB signals. Use these registers to enable an 8-level gray-scale display appropriate to the characteristics of the LCD panel.



Value				Effective voltage	Gray scale
3	2	1	0		
0	0	0	0	0	
0	0	0	1	1/7	
0	0	1	0	1/5	
0	0	1	1	1/4	
0	1	0	0	1/3	
0	1	0	1	2/5	
0	1	1	0	1/2	
0	1	1	1	3/5	
1	0	0	0	2/3	
1	0	0	1	3/4	
1	0	1	0	4/5	
1	0	1	1	6/7	
1	1	0	0	1	

Figure 29 Palette Registers

Reset

The $\overline{RES}$ signal resets and starts the LVIC-II. The reset signal must be held low for at least 1 µs after power-on.
Reset is defined as shown in figure 30.

State of Pins after Reset

In principle, the $\overline{RES}$ signal does not control output signals and it operates regardless of other input signals. Output signals can be classified into the following five groups, depending on their reset states:

- Retains pre-reset state: CL2, A0–A4
- Driven to high-impedance state (or fixed low if no memory is used): RD0–RD7, GD0–GD7, BD0–BD7
- Fixed high: $\overline{MWE}$, CL4, M, $\overline{CU}$, $\overline{CD}$, $\overline{MCS1}$,
- Fixed low: MA0–MA12, R0–R3, G0–G3, B0–B3, CL3, FLM
- Fixed high or low, depending on memory used (table 13): MA13–MA15, $\overline{MCS0}$

State of Registers after Reset

The $\overline{RES}$ signal does not affect data register contents, so the MPU can both read from and write to data registers, even after reset. Registers will retain their pre-reset contents until they are rewritten.

The palette registers, however, are usually set to their default values by a reset. For the default values, refer to the Gray-Scale Palette section and table 11.

Memory Clear Function

After a reset, the LVIC-II writes 0s in the memory area specified by pins or register bits MS0 and MS1 (table 7).

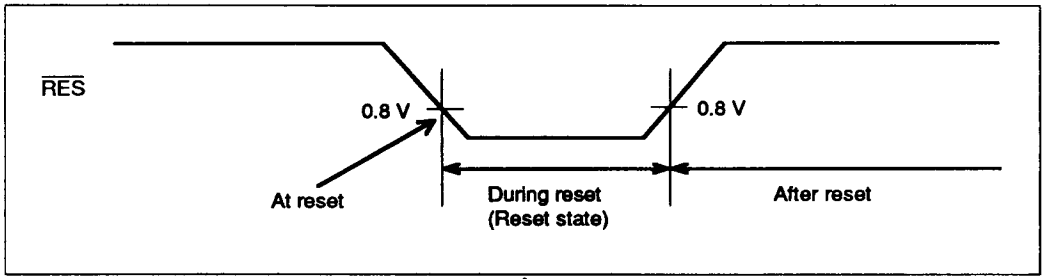


Figure 30 Reset Definition

Table 13 State of Pins after Reset and Memory Type

Memory Type	MA13	MA14	MA15	$\overline{MCS0}$
No memory	Low	Low	High	High
8-kbytes memory	High	High	High	Low
32-kbytes memory	Low	Low	High	Low
64-kbytes memory	Low	Low	Low	Low

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User Notes

1. The following limitations are imposed if no memory is used (MS0 = 0, MS1 = 0):

   - Dual-screen display modes (modes 1, 6, and 16) are disabled.

   - LCD systems with Y-drivers on both sides are disabled, even if a mode for a system with Y-drivers on both sides (mode 3, 5, 10, 12, or 14) is selected; the LVIC-II operates in exactly the same way as in the corresponding mode for a system with Y-drivers on one side (mode 2, 4, 9, 11, or 13). The CL4 pin must be left disconnected in this case.

2. With the internal register programming method, the operation of the LVIC-II after a reset cannot be guaranteed until its internal registers have been written to.

3. The memory clear function might not work normally at power-on or after a reset if the MS0 and MS1 pins or bits are not set correctly to the value corresponding to the type of memory being used.

4. Since the LVIC-II is a CMOS LSI, input pins must not be left disconnected. Refer to the Pin Description and table 1 for details on pin handling.

Programming Restrictions

The values written into the LVIC-II's internal registers have the limits listed in table 14. The symbols used in table 14 are defined in table 15 and figure 31.

Table 14 Limits on Register Values

Item	Limits	Notes	Applicable Registers
Screen configuration	$4 \leqq Nvd \leqq (Ncvbp + Ncvsp) - 1 \leqq 1024$		R2, R3, R4, R6, R7
	$4 \leqq Nhd \leqq (Nchbp \times 1/n + Nchsp) - 1 \leqq 506$	1, 2	
	$(Nhd + 6) \times n \times Nvd \times f_{FLM} \leqq f_{DOTCLK} \leqq$ 30MHz	1, 3	R2, R3, R4, R6, R7
CL3 signal control	$1 \leqq Npw \leqq (Nhd + 6)/2 - 1$	4	R4, R5, R6, R7, R8
	$1 \leqq Npw \leqq Nhd$	5	
	$1 \leqq Npw \leqq Npc - 1$	6	
DISPTMG signal generation	$1 \leqq Nchbp \leqq 256$	7	R12, R13
	$1 \leqq Ncvbp \leqq 256$	7	R14, R15
No memory	$4 \leqq Nhd \leqq Nchsp - 4$	8	R2, R3, R4,
	$4 \leqq Nvd \leqq Ncvsp - 1$	8	R6, R7

Notes:
1. Lowercase n indicates the horizontal character pitch which is the number of horizontal dots composing a character.
2. Nhd ≦ 250 in the dual screen modes (display modes 1, 6, and 16).
3. f_{FLM} is the FLM signal frequency and f_{DOTCLK} is the CRT display dot clock (DOTCLK) frequency. $f_{LDOTCK} < f_{DOTCLK} \times 15/16$ or $f_{LDOTCK} = f_{DOTCLK}$ (f_{LDOTCK} is the LCD dot clock (LDOTCK) frequency)
4. In display modes 1, 2, 4, and 6–8
5. In display modes 3, 5, and 9–12 when Npw = (value in R8) + 5
6. In display modes 13–15 when Npw = (value in R8) + 5
7. (Value in R14 and R15) ≦ (Nchsp × n + Nchbp) – Nhd × n – 2 (n = horizontal character pitch) (Value in R12 and R13) ≦ (Ncvsp + Ncvbp) – Nvd – 2
8. Nht = Nchsp + (Nchbp × 1/n), Nvd < Ncvbp + Ncvsp (Nht = (Nhd + 6) if buffer memory is used) (n = horizontal character pitch)

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Table 15 Symbol Definitions

Symbol	Definition
Nchd	Number of horizontal displayed characters on the CRT display (number of horizontal displayed dots on the CRT display × 1/8)
Nchsp	Number of characters between the rising edge of the DISPTMG signal and that of the HSYNC signal (number of dots between the rising edge of the DISPTMG signal and that of the HSYNC signal × 1/8) (= horizontal synchronization position)
Nchbp	Number of dots between the rising edge of the HSYNC signal and that of the DISPTMG signal (just after the rising edge of the HSYNC signal) (= horizontal backporch)
Ncvbp	Number of lines between the active edge of the VSYNC signal and the rising edge of the DISPTMG signal (just after the active edge of the VSYNC signal) (= vertical backporch)
Ncvsp	Number of lines between the rising edge of the DISPTMG signal and the active edge of the VSYNC signal (= vertical synch position)
Ncvd	Number of vertical displayed lines on the CRT display
Nhd	Number of horizontal displayed characters on the LCD (number of horizontal displayed dots on the LCD × 1/8)
Npc	Number of characters during one CL3 signal period (number of dots during one CL3 signal period × 1/8)
Npw	Number of characters while the CL3 signal is high (number of dots while the CL3 signal is high × 1/8)
Nht	Number of characters during a CL1 signal period (number of dots during a CL1 signal period × 1/8)
Nvd	Number of vertical displayed lines on the LCD

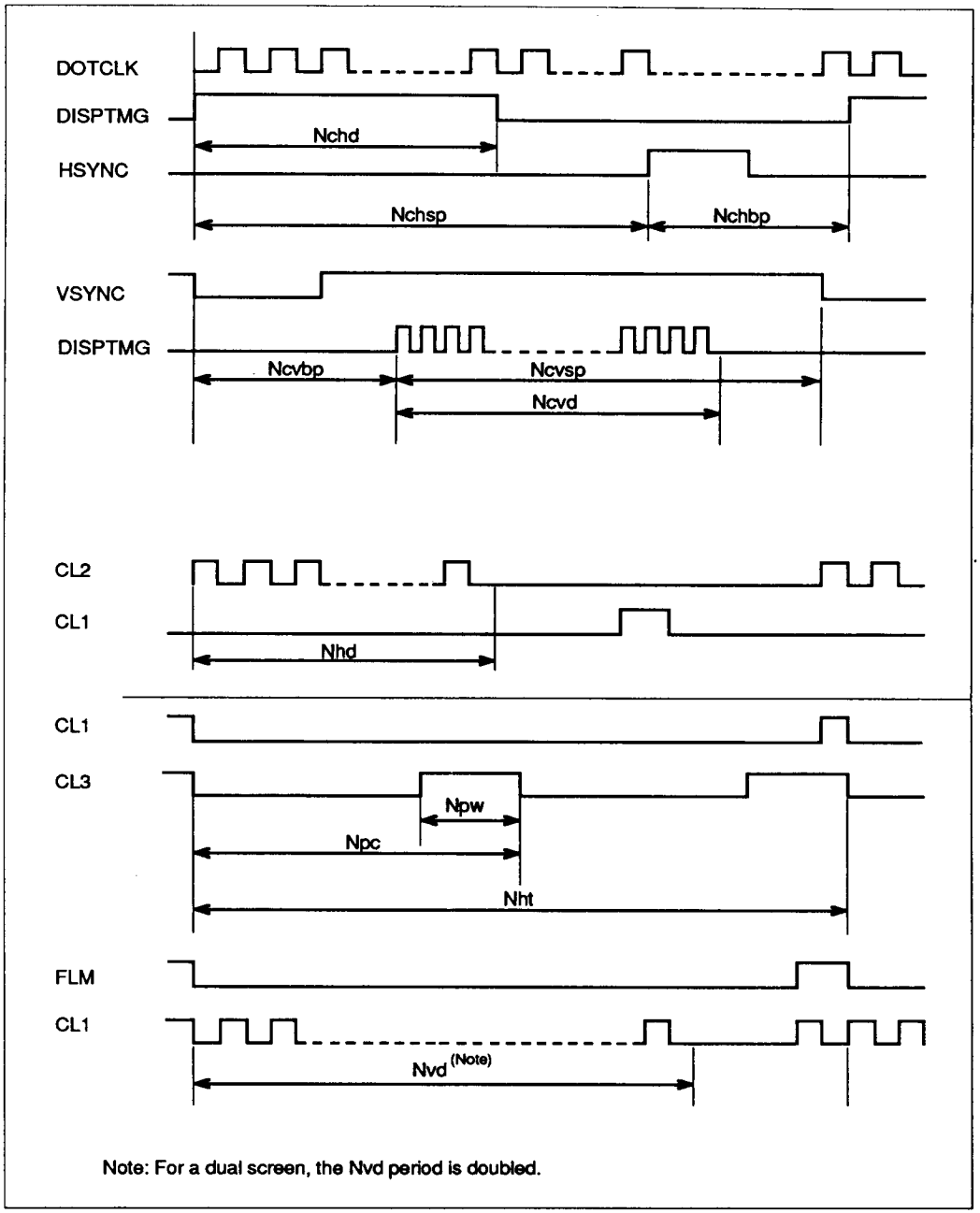

Figure 31 Symbol Definitions

Comparisons with HD66840F

Gray-Scale Generation Method

The HD66840F shifts display data so that data on different lines will be thinned out in different frames, but the HD66841F shifts display data further so that data on different dots will be thinned out in different frames. This reduces deterioration of display contrast.

Display Mode

Mode 16 of the HD66840F (for 8-color display with horizontal stripes and X- and Y-drivers positioned on both sides of the LCD) has been modified into the following new mode in the HD66841F:

Mode number:	16
Pin setting:	(DM3, DM2, DM1, DM0) = (1, 1, 1, 1)
Display colors:	8 colors
LCD data output:	– 12-bit-based data transfer – Dual screen configuration
LCD driver settings:	X-drivers and Y-drivers set on one side
Stripes:	Vertical
Alternation mode:	Every frame

In this mode, the HD66841F outputs upper screen data and lower screen data alternately, as shown in figure 32. In this case, the CL2 frequency is one quarter of the LDOTCK frequency.

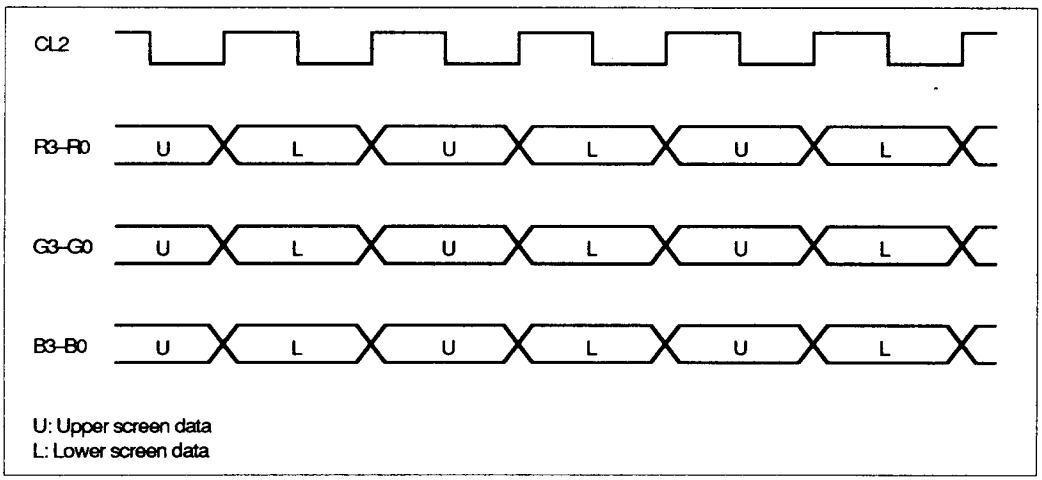

Figure 32 Operation in New HD66841F Mode 16

Table 16 Gray-Scale Palette

	HD66840F	HD66841F
Numbers of registers	16	24 (palette registers have been added to the HD66840's registers)
Selection of correspondence between CRT display colors and gray-scale levels	Impossible	Possible (any of 13 levels assignable to each of 8 colors)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	–0.3 to 7.0	V
Input voltage	V_{in}	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0V ± 10%, GND = 0 V, Ta = –20°C to +75°C). If these conditions are exceeded, LSI reliability may be affected.
2. All voltages are referenced to GND = 0 V.

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Max	Unit	Test Conditions	Note(s)
Input high voltage						
$\overline{RES}$ pin	V_{IH}	V_{CC} – 0.5	V_{CC} + 0.3	V		
TTL interface pins		2.0	V_{CC} + 0.3			1
TTL interface pins		2.2	V_{CC} + 0.3			4
CMOS interface pins		0.7 V_{CC}	V_{CC} + 0.3			1
Input low voltage						
TTL interface pins, $\overline{RES}$ pin	V_{IL}	–0.3	0.8	V		1
TTL interface pins		–0.3	0.6			5
CMOS interface pins		–0.3	0.3 V_{CC}			1
Output high voltage						
TTL interface pins	V_{OH}	2.4	—	V	I_{OH} = –200 µA	2
CMOS interface pins		V_{CC} – 0.8	—		I_{OH} = –200 µA	
Output low voltage						
TTL interface pins	V_{OL}	—	0.4	V	I_{OL} = 1.6mA	2
CMOS interface pins		—	0.8		I_{OL} = 200µA	
Input leakage current						
All inputs expect I/O common pins	I_{IL}	–2.5	2.5	µA		3
Three-state (off-state) leakage current						
I/O common pins	I_{TSL}	–10.0	10.0	µA		3
Power dissipation	I_{CC}	—	250	mW	f_{DOTCLK} = 30 MHz, output pins left disconnected	

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Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, RD0–RD7, GD0–GD7, BD0–BD7, D0–D3, A0/$\overline{RD}$/XDOT, RS/ADJ/A4, $\overline{CS}$/MS0
CMOS interface inputs: DM0–DM3, DOTE, PMOD0, PMOD1, A1/YL0–A3/YL2

2. TTL interface inputs: A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, D0–D3, RD0–RD7, GD0–GD7, BD0–BD7, MA0–MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$, RS/ADJ/A4
CMOS interface inputs: $\overline{CU}$, $\overline{CD}$, R0/LU0–R3/LU3, G0/LD0–G3/LD3, B0–B3, M, FLM, CL1, CL2, CL3, CL4

3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, D0–D3, RD0–RD7, GD0–GD7, BD0–BD7, RS/ADJ/A4
Inputs other than I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE , DM0–DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG

4. TTL interface inputs: $\overline{WR}$/MS1, LDOTCK, DOTCLK

5. TTL interface inputs: $\overline{WR}$/MS1

AC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20°C to +75°C)

Video Signal Interface

Item	Symbol	Min	Max	Unit	Reference
DOTCLK cycle time	t_{CYCD}	33	1000	ns	Figure 33
DOTCLK high-level pulse width	t_{WDH}	16.5	—	ns	
DOTCLK low-level pulse width	t_{WDL}	16.5	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
RGB setup time	t_{VDS}	10	—	ns	
RGB hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Figure 33 except for DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	

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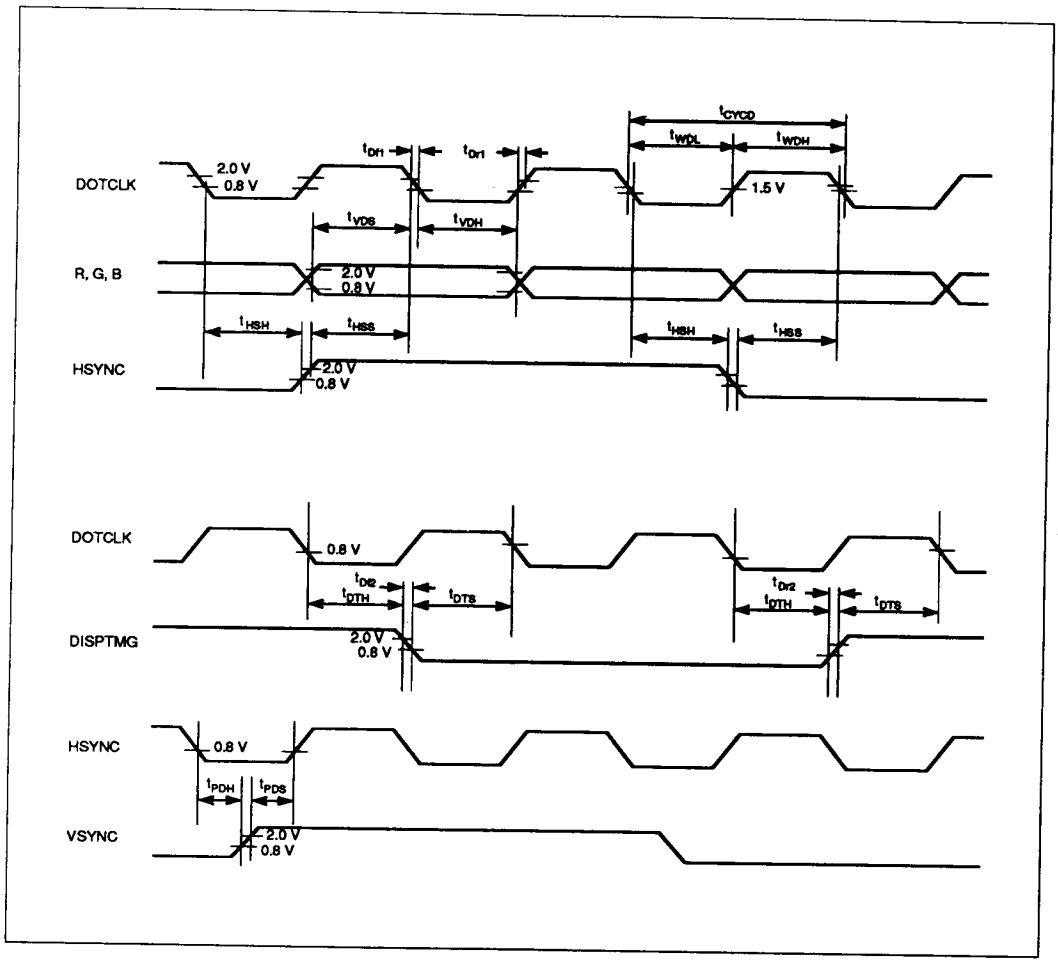

Figure 33 Video Signal Interface

Buffer Memory Interface

Item	Symbol	Min	Unit	Reference
Read cycle time	t_{RC}	5 t_{CYCD} – 50	ns	Figures 34 and 35
RD0–RD7, GD0–GD7, BD0–BD7 data setup time	t_{SMD}	25	ns	
RD0–RD7, GD0–GD7, BD0–BD7 data hold time	t_{HMD}	0	ns	
Write cycle time	t_{WC}	6 t_{CYCD} – 50	ns	
Address setup time	t_{MAS}	t_{CYCD} – 30	ns	
Address hold time	t_{WR}	t_{CYCD} – 30	ns	
Chip select time	t_{CW}	4 t_{CYCD} – 40	ns	
Write pulse width	t_{WP}	4 t_{CYCD} – 40	ns	
RD0–RD7, GD0–GD7, BD0–BD7 output setup time	t_{SMDW}	2 t_{CYCD} – 25	ns	
RD0–RD7, GD0–GD7, BD0–BD7 output hold time	t_{HMDW}	0	ns	

Note: t_{CYCD} is the DOTCLK cycle time (min 33 ns, max 1000 ns).

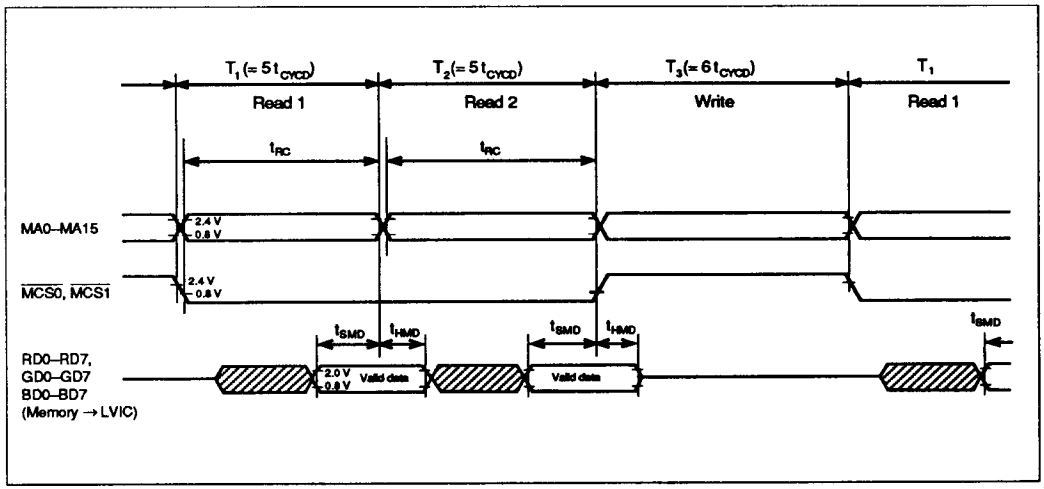

Figure 34 Buffer Memory Interface (RAM read timing)

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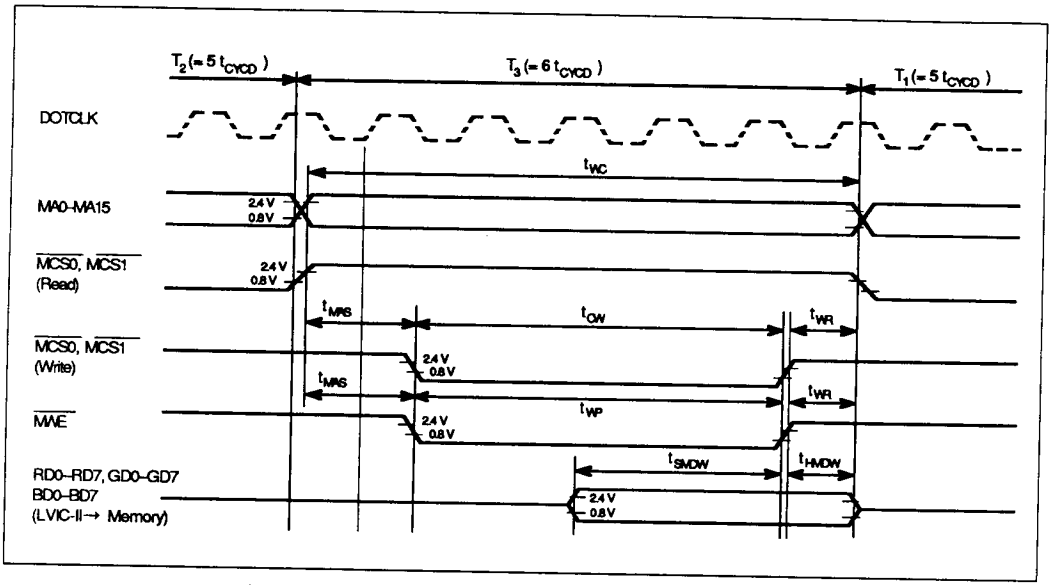

Figure 35 Buffer Memory Interface (RAM write timing)

LCD Driver Interface

TN-Type LCD Driver

Item	Symbol	Min	Max	Unit	Reference
CL2 cycle time	t_{WCL2}	166	—	ns	Figures 36 and 37
CL2 high-level pulse width	t_{WCL2H}	50	—	ns	
CL2 low-level pulse width	t_{WCL2L}	50	—	ns	
CL2 rise time	t_{CL2r}	—	30	ns	
CL2 fall time	t_{CL2f}	—	30	ns	
CL1 high-level pulse width	t_{WCL1H}	200	—	ns	
CL1 rise time	t_{CL1r}	—	30	ns	
CL1 fall time	t_{CL1f}	—	30	ns	
CL1 setup time	t_{SCL1}	500	—	ns	
CL1 hold time	t_{HCL1}	200	—	ns	
FLM hold time	t_{HF}	200	—	ns	
M output delay time	t_{DM}	—	300	ns	
Data delay time	t_{DD}	–20	20	ns	
LDOTCK cycle time	t_{WLDOT}	41	—	ns	

Note: All values are measured at f_{CL2} = 6 MHz.

TFT-Type LCD Driver

Item	Symbol	Min	Max	Unit	Reference
CL2 cycle time (X-drivers on one side)	t_{TCL2S}	133	—	ns	Figures 38 and 39
CL2 high-level pulse width (X-drivers on one side))	t_{TCL2HS}	30	—	ns	
CL2 low-level pulse width (X-drivers on one side)	t_{TCL2LS}	30	—	ns	
CL2 cycle time (X-drivers on both sides)	t_{TCL2D}	266	—	ns	
CL2 high-level pulse width (X-drivers on both sides)	t_{TCL2HD}	80	—	ns	
CL2 low-level pulse width (X-drivers on both sides)	t_{TCL2LD}	80	—	ns	
CL2 rise time	t_{CL2r}	—	30	ns	
CL2 fall time	t_{CL2f}	—	30	ns	
CL1 high-level pulse width	t_{TCL1H}	200	—	ns	
CL1 rise time	t_{CL1r}	—	30	ns	
CL1 fall time	t_{CL1f}	—	30	ns	
Data delay time	t_{DD1}	–20	20	ns	
Data setup time	t_{LDS}	15	—	ns	
Data hold time	t_{LDH}	15	—	ns	
CL1 setup time	t_{TSCL1}	500	—	ns	
CL1 hold time	t_{THCL1}	200	—	ns	
CL3 delay time	t_{DCL3}	50	—	ns	
M delay time	t_{DM}	—	300	ns	
FLM hold time	t_{TFH}	200	—	ns	
LDOTCK cycle time	t_{WLDOT}	33	—	ns	

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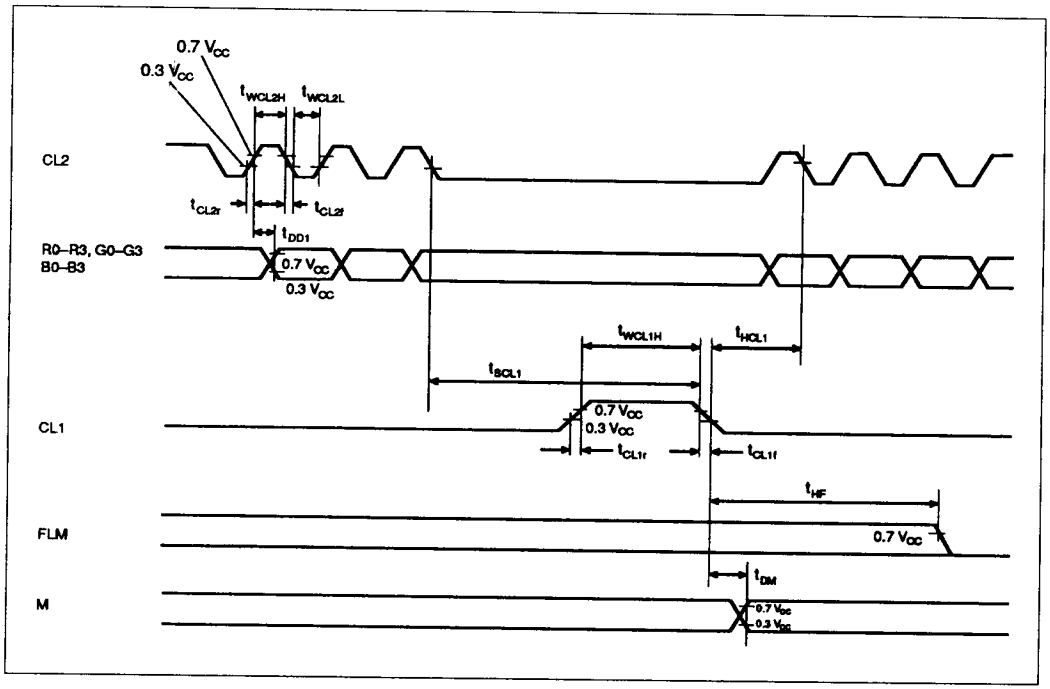

Figure 36 TN-Type LCD Driver Interface

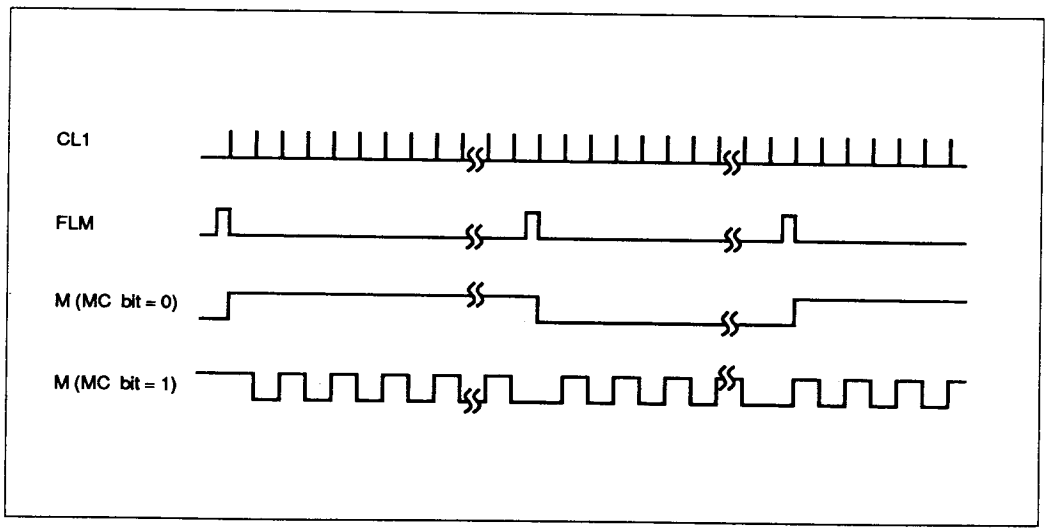

Figure 37 CL1, FLM, and M (expanded detail of figure 36)

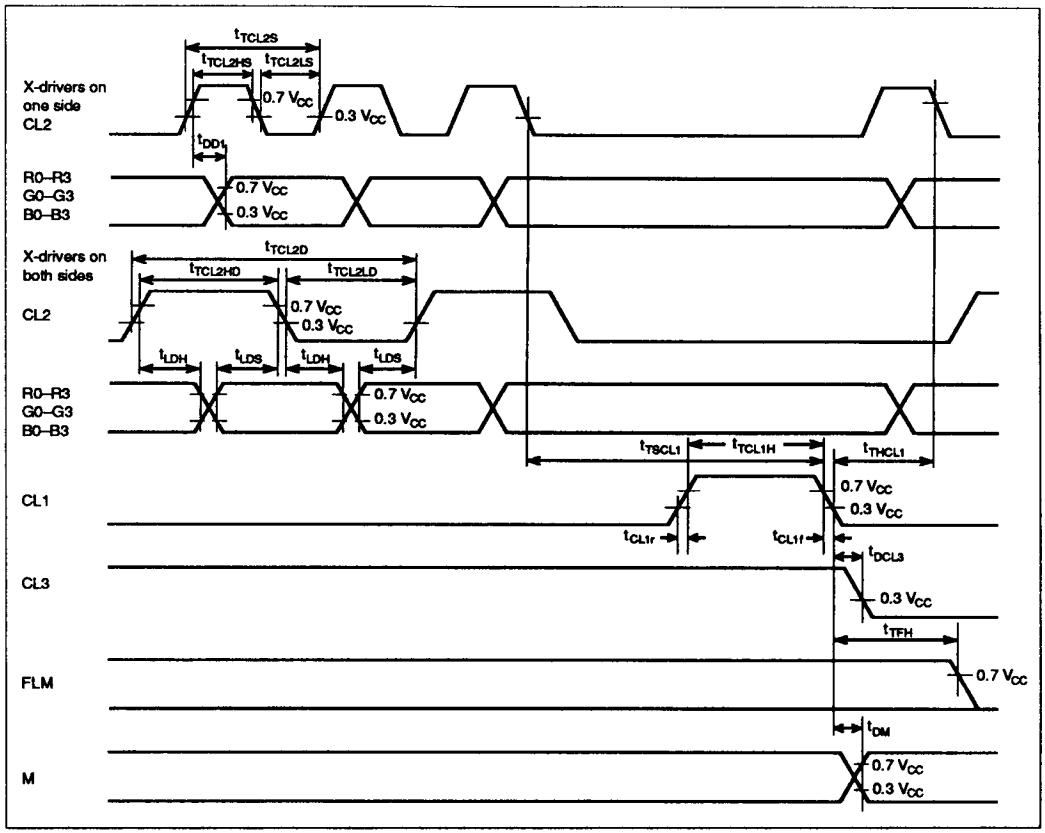

Figure 38 TFT-Type LCD Driver Interface

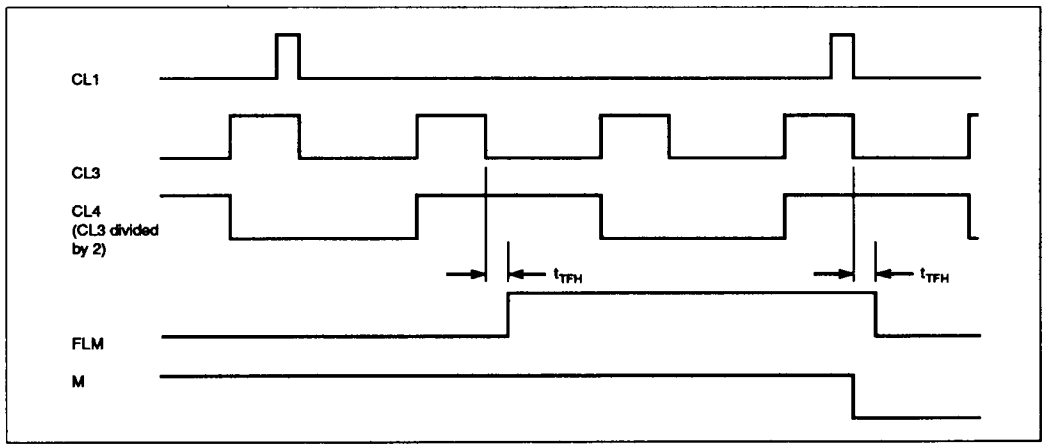

Figure 39 CL1, CL3, CL4, FLM, and M in Horizontal Stripe Modes (expanded detail of figure 38)

Register Programming

MPU Interface

Item	Symbol	Min	Max	Unit	Reference
$\overline{RD}$ high-level pulse width	t_{WRDH}	190	—	ns	Figure 40
$\overline{RD}$ low-level pulse width	t_{WRDL}	190	—	ns	
$\overline{WR}$ high-level pulse width	t_{WWRH}	190	—	ns	
$\overline{WR}$ low-level pulse width	t_{WWRL}	190	—	ns	
$\overline{CS}$, RS setup time	t_{AS}	0	—	ns	
$\overline{CS}$, RS hold time	t_{AH}	0	—	ns	
D0–D3 setup time	t_{DSW}	100	—	ns	
D0–D3 hold time	t_{DHW}	0	—	ns	
D0–D3 output delay time	t_{DDR}	—	150	ns	
D0–D3 output hold time	t_{DHR}	10	—	ns	

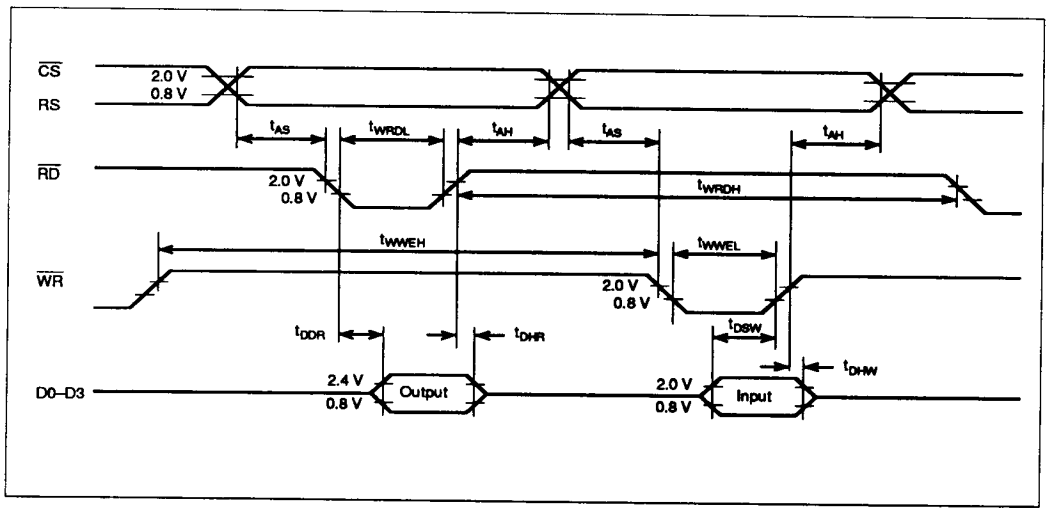

Figure 40 MPU Interface

ROM Interface

Item	Symbol	Min	Max	Unit	Reference
A signal cycle time	t_{CYCA}	528	—	ns	Figure 41
A signal rise time	t_{Ar}	—	100	ns	
A signal fall time	t_{Af}	—	100	ns	
D signal ROM data setup time	t_{DSWD}	120	—	ns	
D signal ROM data hold time	t_{DHWD}	0	—	ns	

Note: $t_{CYCA} = 16\ t_{CYCD}$ (t_{CYCD}: DOTCLK cycle time)

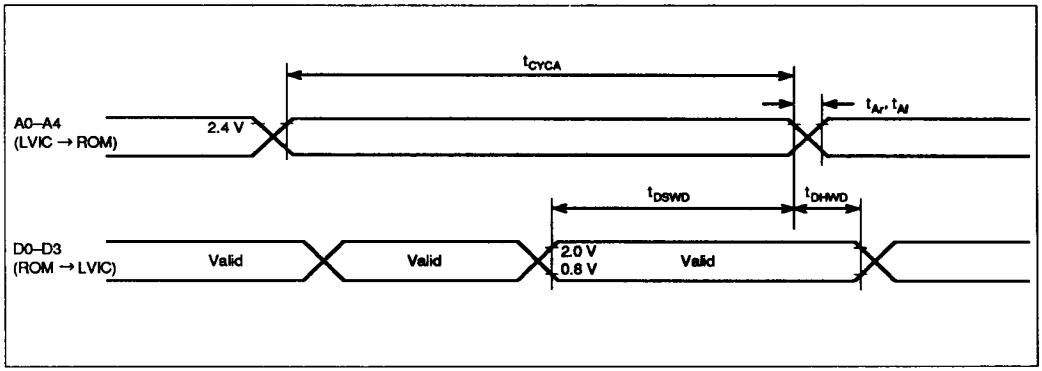

Figure 41 ROM Interface

PLL Interface

Item	Symbol	Min	Max	Unit	Referenc2
$\overline{CU}$ fall delay time	t_{Uf}	—	80	ns	Figure 42
$\overline{CU}$ rise delay time	t_{Ur}	—	80	ns	
$\overline{CD}$ fall delay time	t_{Df}	—	80	ns	
$\overline{CD}$ rise delay time	t_{Dr}	—	80	ns	

Reset Input

Item	Symbol	Min	Max	Unit	Reference
Reset input pulse width	$t_{\overline{RES}}$	1	—	µs	Figure 43

5

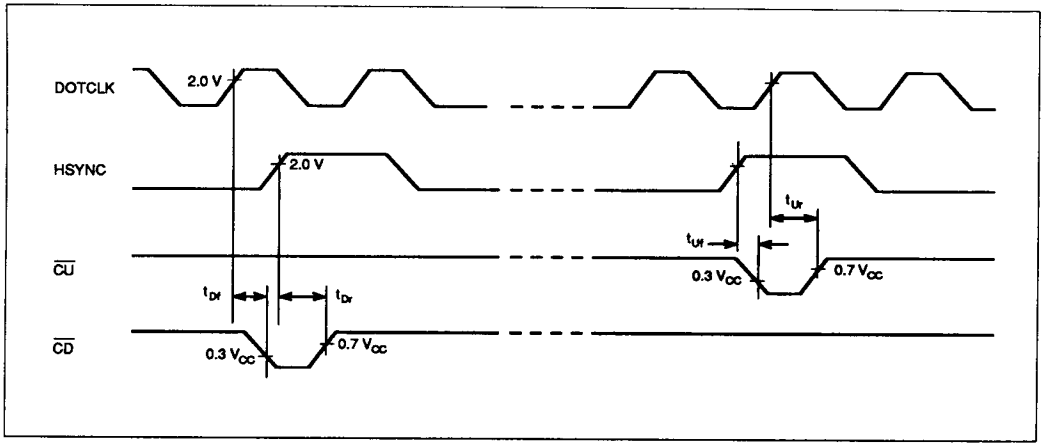

Figure 42 PLL Interface

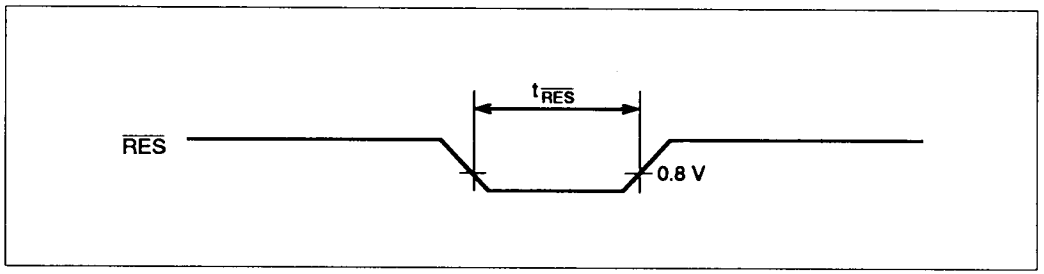

Figure 43 Reset Input

Load Circuits

TTL Load

Pins	R_L	R	C	Remarks
MA0–MA15, $\overline{MWE}$, $\overline{MCS0}$, $\overline{MCS1}$, BD0–BD7, GD0–GD7, RD0–RD7	2.4 kΩ	11 kΩ	40 pF	tr, tf: Not specified
A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, A4/RS/ADJ	2.4 kΩ	11 kΩ	40 pF	tr, tf: Specified

Capacitive Load

Pins	C	Remarks
CL1, CL2	40 pF	tr, tf: Specified
R0–R3, G0–G3, B0–B3, FLM, M, $\overline{CU}$, $\overline{CD}$, CL3, CL4	40 pF	tr, tf: Not specified

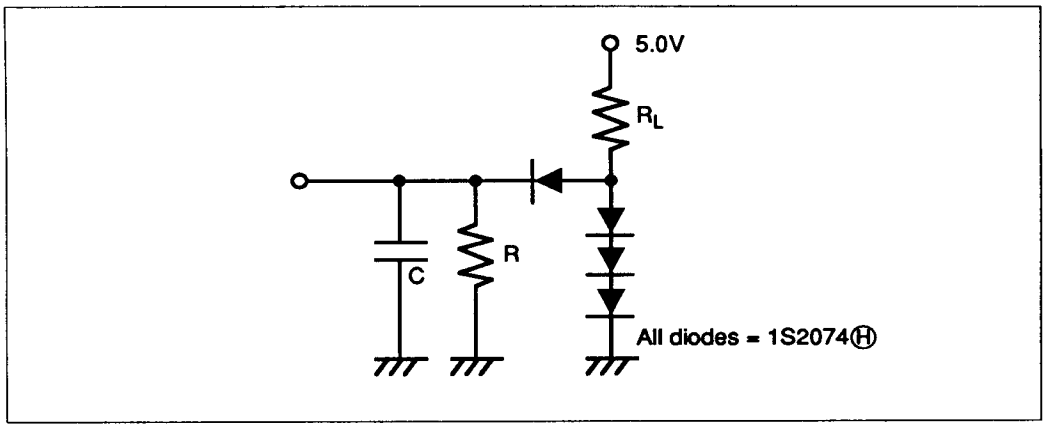

Figure 44 TTL Load Circuit

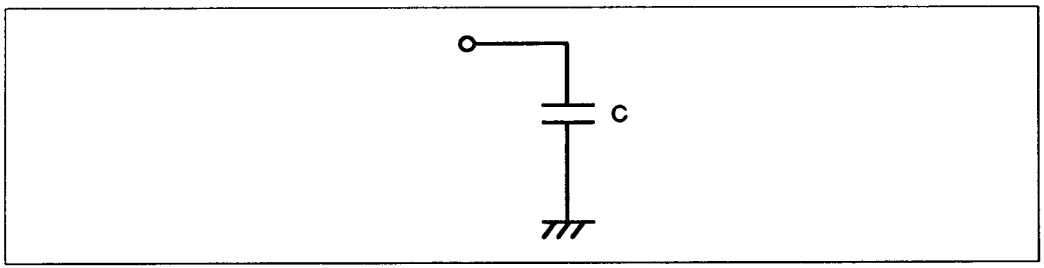

Figure 45 Capacitive Load Circuit

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