

CMOS 4-BIT MICROCONTROLLER

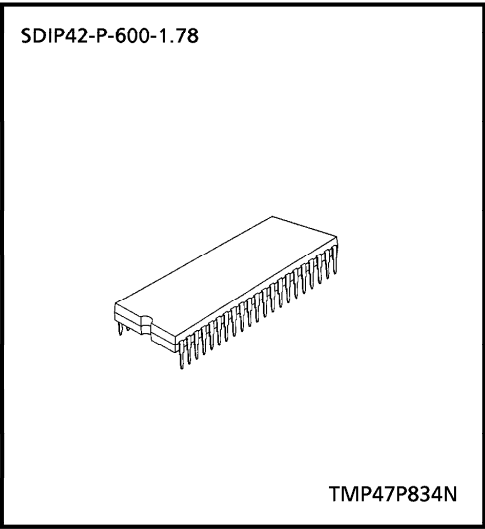
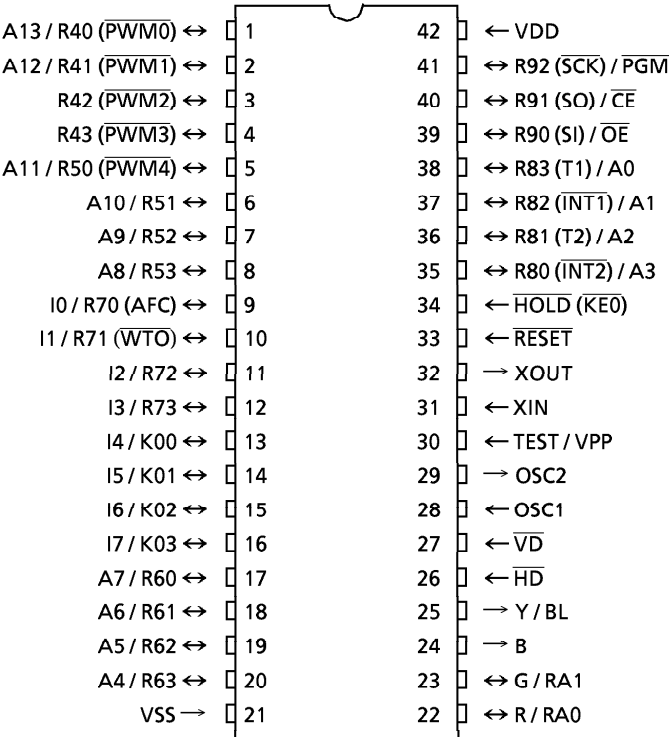
TMP47P834N  
TMP47P834F

The 47P834 is the OTP microcontroller with 64kbits PROM. For program operation, the programming is achieved by using with EPROM programmer (TMM27128A type) and adaptor socket. The function of this device is exactly same as the 47C834.

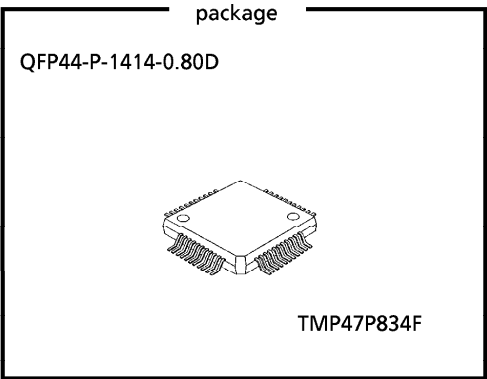
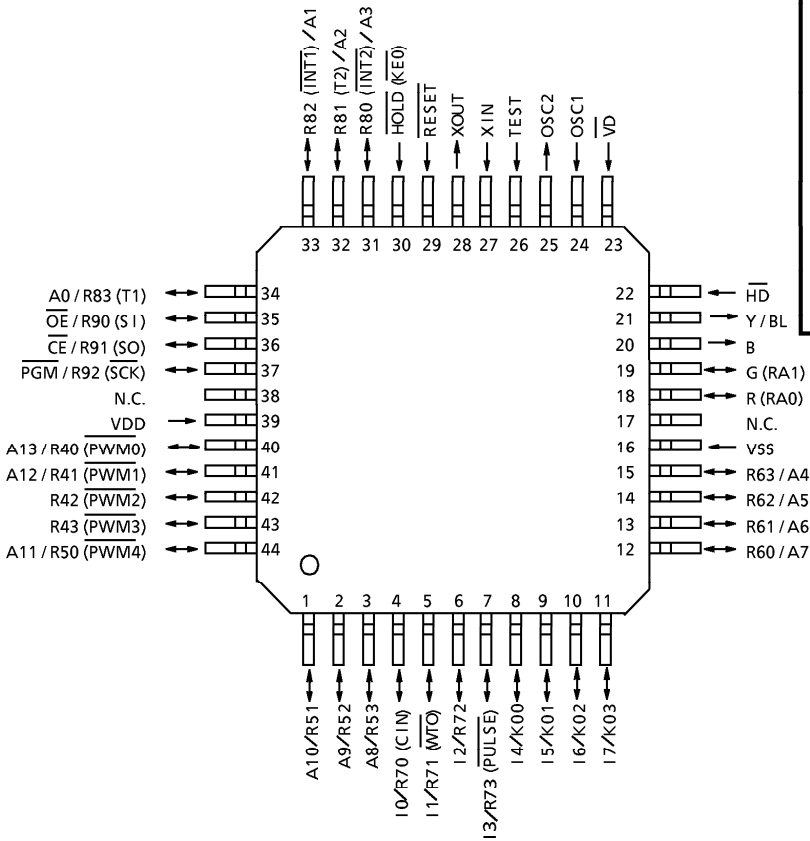
| PART No.   | ROM                 | RAM         | PACKAGE           |
|------------|---------------------|-------------|-------------------|
| TMP47P834N | OTP<br>8192 × 8-bit | 512 × 4-bit | SDIP42-P-600-1.78 |

PIN ASSIGNMENT (TOP VIEW)

SDIP42-P-600-1.78



QFP44-P-1414-0.80D



**PIN FUNCTION**

The 47P834 has MCU mode and PROM mode.

## (1) MCU mode

The 47C834 and the 47P834 are pin compatible (TEST pin for out-going test. Be fixed to low level).

## (2) PROM mode

| PIN NAME     | Input / Output | FUNCTIONS                                     | PIN NAME (MCU mode) |
|--------------|----------------|-----------------------------------------------|---------------------|
| A13 to A12   | Input          | Address inputs                                | R41 to R40          |
| A11 to A8    |                |                                               | R53 to R50          |
| A7 to A4     |                |                                               | R63 to R60          |
| A3 to A0     |                |                                               | R83 to R80          |
| I7 to I4     | I/O            | Data Inputs / outputs                         | K03 to K00          |
| I3 to I0     |                |                                               | R73 to R70          |
| PGM          | Input          | Program control input                         | R92                 |
| CE           |                | Chip Enable input                             | R91                 |
| OE           |                | Chip Enable input                             | R90                 |
| VPP          | Power supply   | + 12.5 V / 5 V (Program supply voltage)       | TEST                |
| VCC          |                | + 5 V                                         | VDD                 |
| VSS          |                | 0 V                                           | VSS                 |
| OSC1         | Output         | OSD resonator connecting pins                 |                     |
| OSC2         |                |                                               |                     |
| Y, B, HD, VD | OSD output     | Be fixed to low level                         |                     |
| G / R        |                |                                               |                     |
| RESET        | Input          | PROM mode setting pin. Be fixed to low level. |                     |
| HOLD         | Input          |                                               |                     |
| XIN          | Input          | Resonator connecting pins                     |                     |
| XOUT         | Output         |                                               |                     |

## OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P834. The 47P834 is the same as the 47C834 except that an EPROM or OTP is used instead of a built-in mask ROM.

### 1. OPERATION mode

The 47P834 has an MCU mode and a PROM mode.

#### 1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C834, except that the TEST/VPP pin does not have built in pull-down resistor and cannot be used open.

##### 1.1.1 Program Memory

The program storage area is the same as for the 47C834. Data conversion tables must be set in two locations when using the 47P834 to check 47C434/634 operation.

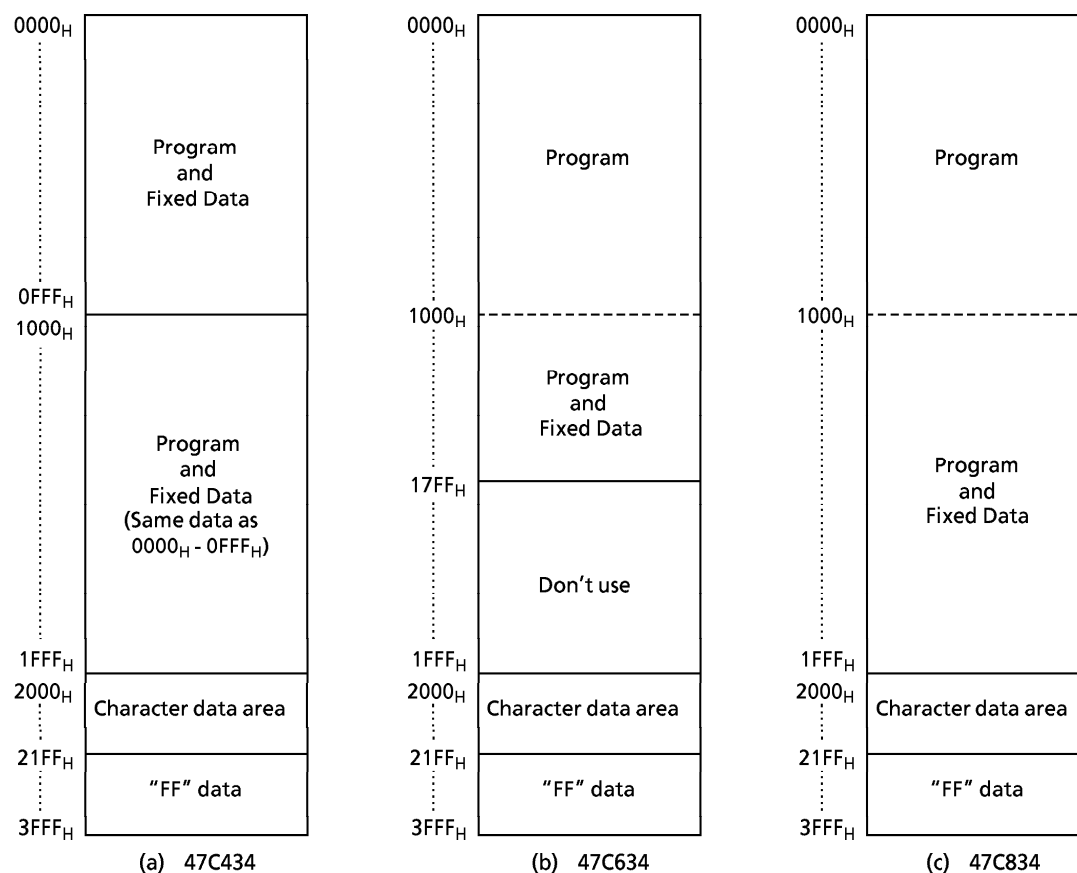


Figure 1-1. Program area

*Note. Some data have been written in address "21F0<sub>H</sub>" to "21FF<sub>H</sub>", because of the out-going test.*

#### 1.1.2 Data Memory

The 47P834 has two built-in 256 × 4-bit data memory banks (DMB0, DMB1).

When using the 47P834 as a 47C634 evaluator, do not write data to address 80<sub>H</sub> and following, even though the DMB1 addresses are 00-FF<sub>H</sub>. And when using as a 47C434 evaluator, do not write data to the whole DMB1. There is no necessary to take into consideration a special function shared area, because one is built in DMB0.

### 1.1.3 Other Peripheral Hardware Function

Using as 47C434/634 evaluator, do not write data into the command register OP0B of PULSE output control and Image Receiving Mode Control.

### 1.1.4 Input/Output Circuitry

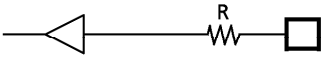
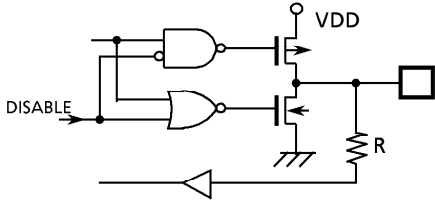
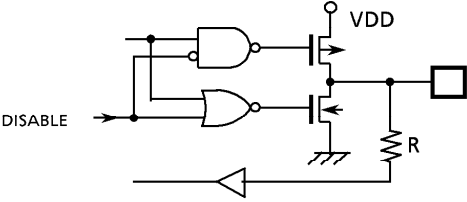
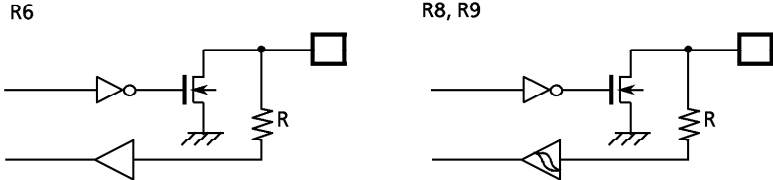
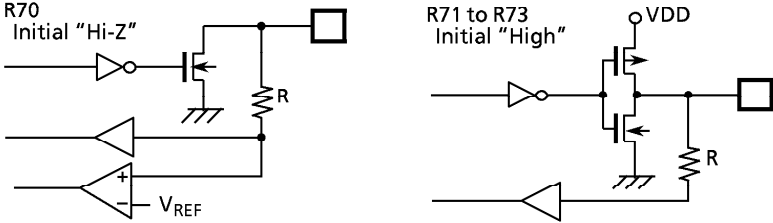
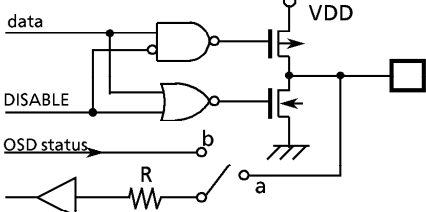
#### (1) Control pins

This is the same as for the 47C434/634/834 except that there is no built in pull-down resistor for the TEST pin. Input/output circuitry of the 47P834 control pins is shown below.

| CONTROL PIN                                      | I/O              | CIRCUITRY | REMARKS                                                                                                                                |
|--------------------------------------------------|------------------|-----------|----------------------------------------------------------------------------------------------------------------------------------------|
| XIN<br>XOUT                                      | Input<br>Output  |           | Resonator connecting pins<br>$R = 1\text{ k}\Omega$ (typ.)<br>$R_f = 1.5\text{ M}\Omega$ (typ.)<br>$R_O = 2\text{ k}\Omega$ (typ.)     |
| $\overline{\text{RESET}}$                        | Input            |           | Hysteresis input<br>Contained pull-up resistor<br>$R_{IN} = 220\text{ k}\Omega$ (typ.)<br>$R = 1\text{ k}\Omega$ (typ.)                |
| $\overline{\text{HOLD}}$ (KE0)                   | Input<br>(Input) |           | Hysteresis input<br>(Sense input)<br>$R = 1\text{ k}\Omega$ (typ.)                                                                     |
| TEST                                             | Input            |           | Not contained<br>pull-down resistor<br>$R = 1\text{ k}\Omega$ (typ.)                                                                   |
| OSC1<br>OSC2                                     | Input<br>Output  |           | Oscillation terminals for OSD<br>$R = 1\text{ k}\Omega$ (typ.)<br>$R_f = 1.5\text{ M}\Omega$ (typ.)<br>$R_O = 2\text{ k}\Omega$ (typ.) |
| $\overline{\text{HD}}$<br>$\overline{\text{VD}}$ | Input            |           | Synchronous signal input<br>Hysteresis input<br>$R = 1\text{ k}\Omega$ (typ.)                                                          |



The input/output circuitry of the 47P834 I/O port is as follows.

| PORT               | I/O    | INPUT/OUTPUT CIRCUITRY (code : PA)                                                   | REMARKS                                                                                               |
|--------------------|--------|--------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|
| K0                 | Input  |     | Not contained<br>Pull-up<br>or<br>pull-down resistor<br><br>$R = 1\text{ k}\Omega$ (typ.)             |
| R4<br>R50          | I/O    |     | Tri-state<br>Initial "Hi-Z"<br><br>$R = 1\text{ k}\Omega$ (typ.)                                      |
| R51<br>R52<br>R53  | I/O    |    | Tri-state<br>Initial "Hi-Z"<br><br>$R = 1\text{ k}\Omega$ (typ.)                                      |
| R6<br>R8<br>R9     | I/O    |  | Sink open drain<br>Initial "Hi-Z"<br>Hysteresis input (R8, R9)<br><br>$R = 1\text{ k}\Omega$ (typ.)   |
| R7                 | I/O    |  | Sink open drain<br>and<br>push-pull<br>Comparator input<br>(R70 pin)<br>$R = 1\text{ k}\Omega$ (typ.) |
| R (RA0)<br>G (RA1) | I/O    |   | Tri-state<br>Initial "Hi-Z"<br>$R = 1\text{ k}\Omega$ (typ.)                                          |
| B<br>Y (BL)        | Output |                                                                                      | R, G : Side a<br>B, Y : Side b                                                                        |

## 1.2 PROM mode

The PROM mode is set by setting the  $\overline{\text{RESET}}$ ,  $\overline{\text{HOLD}}$ , R and G pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification. (A high-speed program mode is used set the ROM type the same as for the TMM 27128A.)

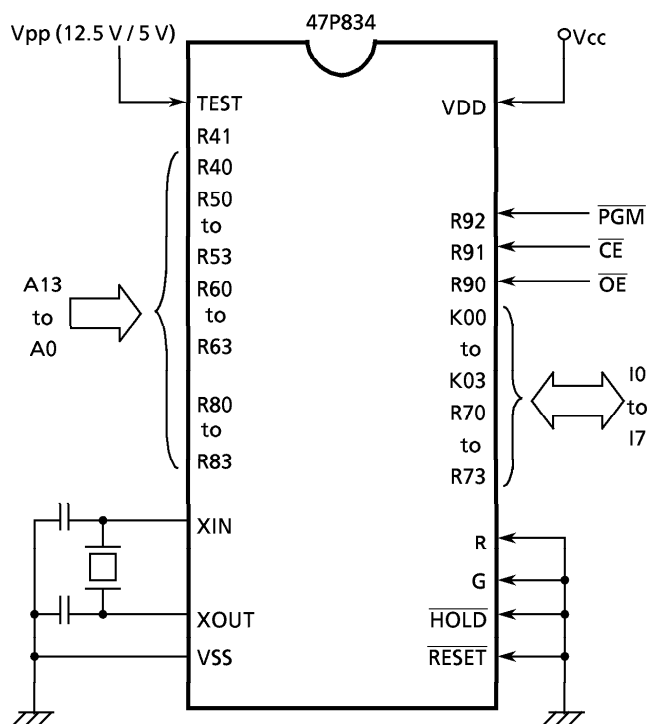


Figure 1-3. Setting for PROM mode

### 1.2.1 High speed programming mode

The device is set up in the high speed programming mode when the programming voltage (12.5 V) is applied to the Vpp pin with Vcc = 6 V and  $\overline{\text{PGM}} = V_{IH4}$ . The programming is achieved by applying a single TTL low level 1 ms, pulse the  $\overline{\text{PGM}}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify mode. If the programmed data is not correct, another program pulse of 1 ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 15 times) After correctly programming the selected address, one additional program pulse with pulse width 4 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

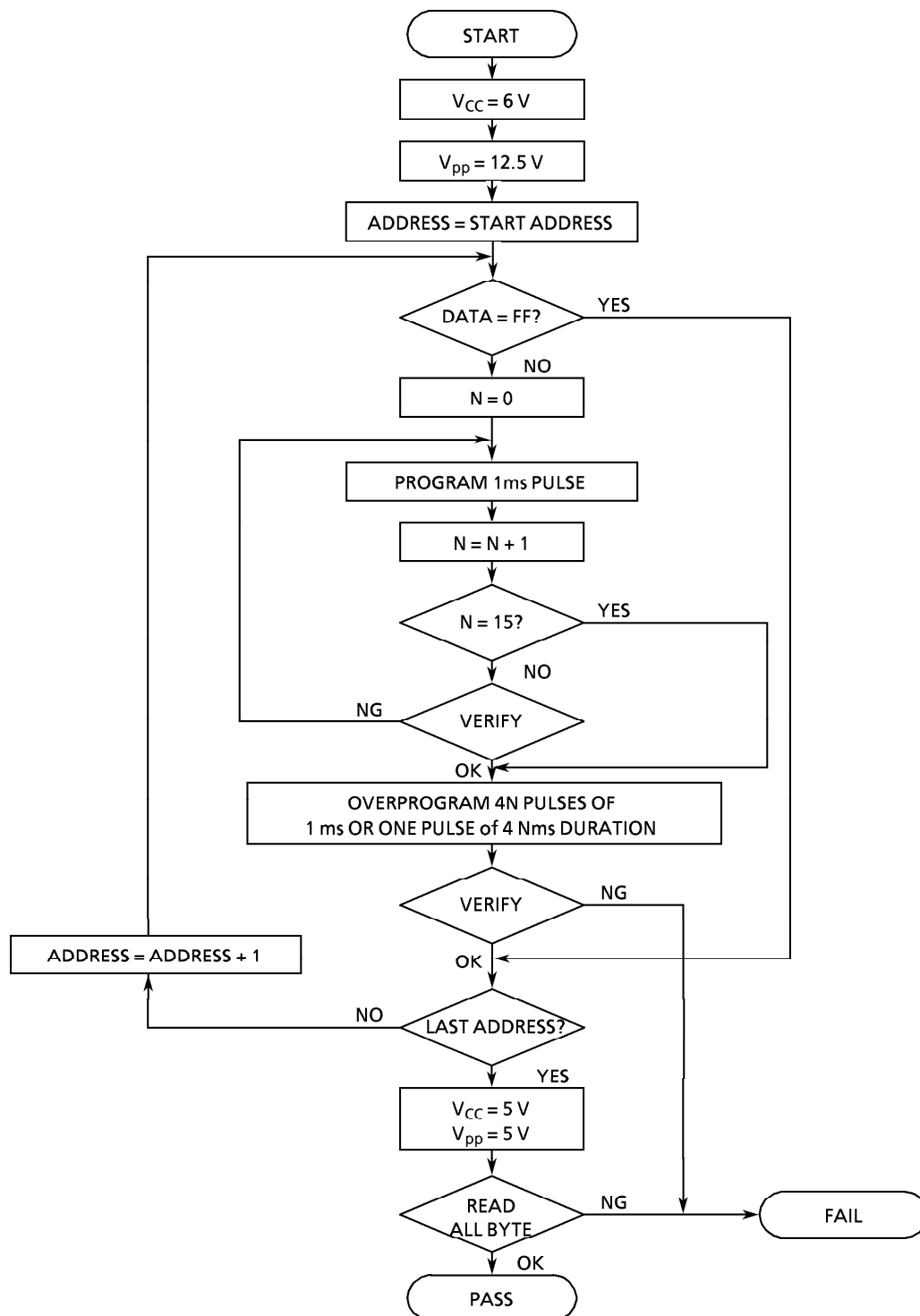


Figure1-4. FLOW CHART

## ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V<sub>SS</sub> = 0 V)

| PARAMETER                    | SYMBOL              | PINS                               | RATING                         | UNIT |
|------------------------------|---------------------|------------------------------------|--------------------------------|------|
| Supply Voltage               | V <sub>DD</sub>     |                                    | – 0.3 to 7                     | V    |
| Input Voltage                | V <sub>IN</sub>     |                                    | – 0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output Voltage               | V <sub>OUT1</sub>   | Except sink open drain pin         | – 0.3 to V <sub>DD</sub> + 0.3 | V    |
|                              | V <sub>OUT2</sub>   | Sink open drain pin except R7 port | – 0.3 to 10                    |      |
| Output Current (Per 1 pin)   | I <sub>OUT1</sub>   | R6 port                            | 30                             | mA   |
|                              | I <sub>OUT2</sub>   | R7, R8, R9 port                    | 3.2                            |      |
| Output Current (Total)       | Σ I <sub>OUT1</sub> | R6 port                            | 60                             | mA   |
| Power Dissipation            | PD                  |                                    | 600                            | mW   |
| Soldering Temperature (time) | T <sub>slid</sub>   |                                    | 260 (10 s)                     | °C   |
| Storage Temperature          | T <sub>stg</sub>    |                                    | – 55 to 125                    | °C   |
| Operating Temperature        | T <sub>opr</sub>    |                                    | – 30 to 70                     | °C   |
| Programming Voltage          | V <sub>pp</sub>     | TEST / VPP pin                     | – 0.3 to 14.0                  | V    |

RECOMMENDED OPERATING CONDITIONS (V<sub>SS</sub> = 0 V, T<sub>opr</sub> = – 30 to 70 °C)

| PARAMETER          | SYMBOL           | PINS                    | CONDITIONS              | Min.                   | Max.                   | UNIT |
|--------------------|------------------|-------------------------|-------------------------|------------------------|------------------------|------|
| Supply Voltage     | V <sub>DD</sub>  |                         | in the Normal mode      | 4.5                    | 6.0                    | V    |
|                    |                  |                         | in the HOLD mode        | 2.0                    |                        |      |
| Input High Voltage | V <sub>IH1</sub> | Except Hysteresis Input | V <sub>DD</sub> ≥ 4.5 V | V <sub>DD</sub> × 0.7  | V <sub>DD</sub>        | V    |
|                    | V <sub>IH2</sub> | Hysteresis Input        |                         | V <sub>DD</sub> × 0.75 |                        |      |
|                    | V <sub>IH3</sub> |                         | V <sub>DD</sub> < 4.5 V | V <sub>DD</sub> × 0.9  |                        |      |
| Input Low Voltage  | V <sub>IL1</sub> | Except Hysteresis Input | V <sub>DD</sub> ≥ 4.5 V | 0                      | V <sub>DD</sub> × 0.3  | V    |
|                    | V <sub>IL2</sub> | Hysteresis Input        |                         |                        | V <sub>DD</sub> × 0.25 |      |
|                    | V <sub>IL3</sub> |                         | V <sub>DD</sub> < 4.5 V |                        | V <sub>DD</sub> × 0.1  |      |
| Clock Frequency    | f <sub>c</sub>   | XIN, XOUT               |                         | 0.4                    | 4.2                    | MHz  |
|                    | f <sub>OSD</sub> | OSC1, OSC2              |                         | –                      | 6.0                    |      |

Note. Input Voltage V<sub>IH3</sub>, V<sub>IL3</sub> : in the HOLD mode.

D.C. CHARACTERISTICS (V<sub>SS</sub> = 0 V, T<sub>opr</sub> = -30 to 70 °C)

| PARAMETER                             | SYMBOL           | PINS                                   | CONDITIONS                                         | Min. | Typ. | Max. | UNIT |
|---------------------------------------|------------------|----------------------------------------|----------------------------------------------------|------|------|------|------|
| Hysteresis Voltage                    | V <sub>HS</sub>  | Hysteresis Input                       |                                                    | —    | 0.7  | —    | V    |
| Input Current                         | I <sub>IN1</sub> | K0 port, TEST, RESET, HOLD             | V <sub>DD</sub> = 5.5 V,                           | —    | —    | ± 2  | μA   |
|                                       | I <sub>IN2</sub> | R port (open drain)                    | V <sub>IN</sub> = 5.5 V / 0 V                      |      |      |      |      |
| Input Low Current                     | I <sub>IL</sub>  | R port (push-pull)                     | V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V   | —    | —    | -2   | mA   |
| Input Resistance                      | R <sub>IN1</sub> | K0 port with pull-up/pull-down         |                                                    | 30   | 70   | 150  | kΩ   |
|                                       | R <sub>IN2</sub> | RESET                                  |                                                    | 100  | 220  | 450  |      |
| Output Leakage Current                | I <sub>LO</sub>  | Tri-state R6, R8, R9 port (open drain) | V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V  | —    | —    | ± 2  | μA   |
| Output High Voltage                   | V <sub>OH1</sub> | R port (push-pull)                     | V <sub>DD</sub> = 4.5 V, I <sub>OH</sub> = -200 μA | 2.4  | —    | —    | V    |
|                                       | V <sub>OH2</sub> | R port (tri-state), OSD output         | V <sub>DD</sub> = 4.5 V, I <sub>OH</sub> = -0.7 mA | 4.1  | —    | —    |      |
| Output Low Voltage                    | V <sub>OL1</sub> | R7, R8, R9 port                        | V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 1.6 mA  | —    | —    | 0.4  | V    |
|                                       | V <sub>OL2</sub> | R port (tri-state), OSD output         | V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 0.7 mA  |      |      |      |      |
| Output Low Current                    | I <sub>OL</sub>  | R6 port                                | V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 1.0 V   | —    | 20   | —    | mA   |
| Supply Current<br>(in the Nomal mode) | I <sub>DD</sub>  |                                        | V <sub>DD</sub> = 5.5 V<br>f <sub>c</sub> = 4 MHz  | —    | 5    | 10   | mA   |
| Supply Current<br>(in the HOLD mode)  | I <sub>DDH</sub> |                                        | V <sub>DD</sub> = 5.5 V                            | —    | 0.5  | 10   | μA   |

Note 1. Typ. values show those at T<sub>opr</sub> = 25 °C, V<sub>DD</sub> = 5 V.

Note 2. Input Current I<sub>IN1</sub> : The current through resistor is not included, when the pull-up/pull-down resistor is contained.

Note 3. Supply Current : V<sub>IN</sub> = 5.3 V / 0.2 V  
 The K0 port is open when the pull-up / pull-down resistor is contained.  
 The voltage applied to the R port is within the valid range V<sub>IL</sub> or V<sub>IH</sub>.

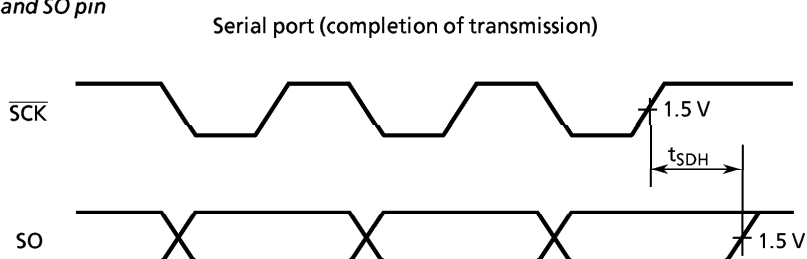
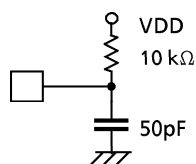
## A / D CONVERSION CHARACTERISTICS

| PARAMETER            | SYMBOL           | PINS | CONDITIONS | Min.            | Typ. | Max.            | UNIT |
|----------------------|------------------|------|------------|-----------------|------|-----------------|------|
| Analog Input Voltage | V <sub>AIN</sub> | CIN  |            | V <sub>SS</sub> | —    | V <sub>DD</sub> | V    |
| A/D Conversion Error | —                |      |            | —               | —    | ± 1/4           | LSB  |

**A.C. CHARACTERISTICS** ( $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 4.5\text{ to }6.0\text{ V}$ ,  $T_{opr} = -30\text{ to }70\text{ }^{\circ}\text{C}$ )

| PARAMETER                    | SYMBOL    | CONDITION                    | Min.              | Typ. | Max. | UNIT          |
|------------------------------|-----------|------------------------------|-------------------|------|------|---------------|
| Instruction Cycle Time       | $t_{cy}$  |                              | 1.9               | —    | 20   | $\mu\text{s}$ |
| High level Clock Pulse Width | $t_{WCH}$ | For external clock operation | 80                | —    | —    | ns            |
| Low level Clock Pulse Width  | $t_{WCL}$ |                              |                   |      |      |               |
| Shift Data Hold Time         | $t_{SDH}$ |                              | $0.5t_{cy} - 300$ | —    | —    | ns            |

*Note. Shift data Hold Time*  
*External circuit for  $\overline{\text{SCK}}$  pin and SO pin*

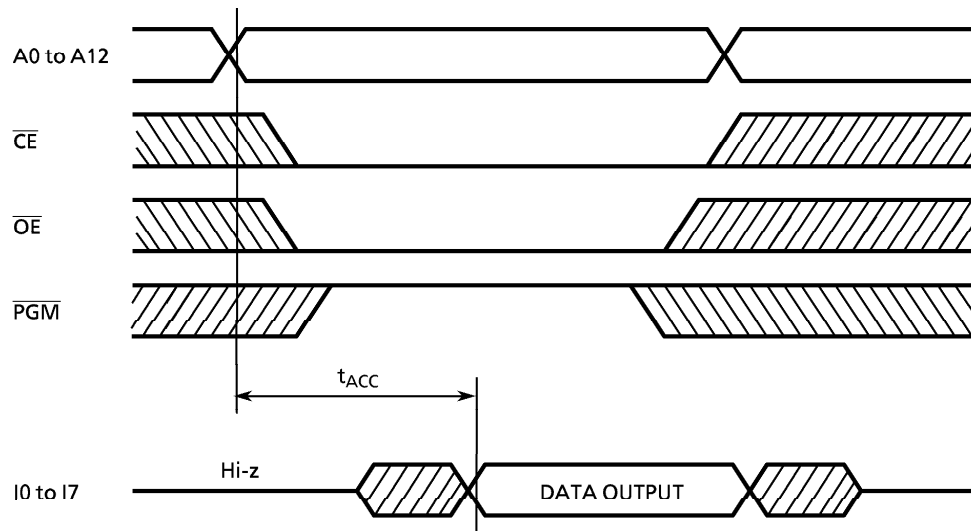

**RECOMMENDED OSCILLATING CONDITIONS** ( $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 4.5\text{ to }6.0\text{ V}$ ,  $T_{opr} = -30\text{ to }70\text{ }^{\circ}\text{C}$ )

Recommended oscillating conditions of the 47P834 are equal to the 47C834's.

**DC/AC CHARACTERISTICS** ( $V_{SS} = 0\text{ V}$ )

**(1) Read Operation**

| PARAMETER                 | SYMBOL    | CONDITION                        | Min.                | Typ. | Max.                | UNIT |
|---------------------------|-----------|----------------------------------|---------------------|------|---------------------|------|
| Output Level High Voltage | $V_{IH4}$ |                                  | $V_{CC} \times 0.7$ | —    | $V_{CC}$            | V    |
| Output Level Low Voltage  | $V_{IL4}$ |                                  | 0                   | —    | $V_{CC} \times 0.3$ | V    |
| Supply Voltage            | $V_{CC}$  |                                  | 4.75                | —    | 6.0                 | V    |
| Programming Voltage       | $V_{PP}$  |                                  |                     |      |                     |      |
| Address Access Time       | $t_{ACC}$ | $V_{CC} = 5.0 \pm 0.25\text{ V}$ | 0                   | —    | 350                 | ns   |



## (2) High Speed Programming Operation

| PARAMETER                     | SYMBOL    | CONDITION                 | Min.                | Typ. | Max.                | UNIT |
|-------------------------------|-----------|---------------------------|---------------------|------|---------------------|------|
| Input High Voltage            | $V_{IH4}$ |                           | $V_{CC} \times 0.7$ | —    | $V_{CC}$            | V    |
| Input Low Voltage             | $V_{IL4}$ |                           | 0                   | —    | $V_{CC} \times 0.3$ | V    |
| Supply Voltage                | $V_{CC}$  |                           | 4.75                | —    | 6.0                 | V    |
| $V_{PP}$ Power Supply Voltage | $V_{PP}$  |                           | 12.25               | 12.5 | 12.75               | V    |
| Programming Pulse Width       | $t_{PW}$  | $V_{CC} = 6.0 \pm 0.25$ V | 0.95                | 1.0  | 1.05                | ms   |

