

Single 16/Differential 8 Channel CMOS Analog Multiplexers With Active Overvoltage Protection

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- No Channel Interaction During Overvoltage
- Guaranteed R_{ON} Matching
- 44V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range..... $\pm 15V$
- Access Time (Max.) $1.0\mu s$
- Power Dissipation (Max.) $45mW$

Applications

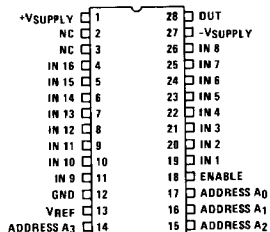
- Data Acquisition Systems
- Control Systems
- Telemetry

Description

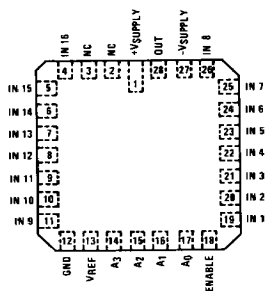
The HI-546/883 and HI-547/883 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels with $\pm 15V$ supplies and digital inputs will sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents $1k\Omega$ of resistance under this condition. These features make the HI-546/883 and HI-547/883 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-546/883 is a 16 channel device and the HI-547/883 is an 8 channel differential version. If input overvoltage protection is not needed, the HI-506/883 and HI-507/883 multiplexers are recommended. For further information see Application Notes 520 and 521.

Pinouts

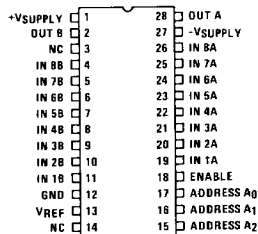
HI1-546/883 (CERAMIC DIP)
TOP VIEW



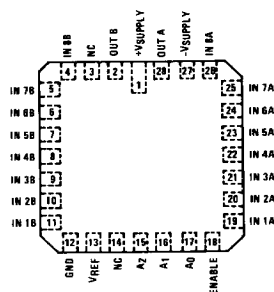
HI4-546/883 (CERAMIC LCC)
TOP VIEW



HI1-547/883 (CERAMIC DIP)
TOP VIEW

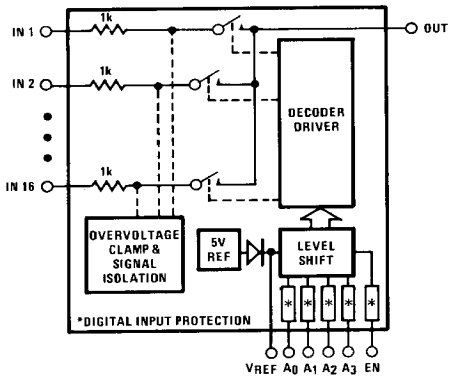


HI4-547/883 (CERAMIC LCC)
TOP VIEW



Functional Diagrams

HI-546/883

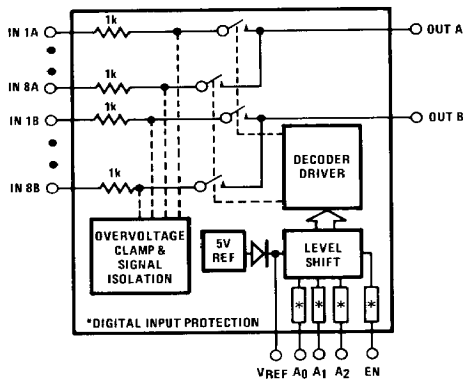


TRUTH TABLES

HI-546/883

A ₃	A ₂	A ₁	A ₀	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-547/883



HI-547/883

A ₂	A ₁	A ₀	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Specifications HI-546/883 HI-547/883

Absolute Maximum Ratings

Voltage Between Supply Pins	44V
+VSUPPLY to Ground	22V
-VSUPPLY to Ground	25V
Analog Input Voltage	+VSUPPLY +20V -VSUPPLY -20V
Digital Input Voltage	+VSUPPLY +4V -VSUPPLY -4V or 20mA, whichever occurs first
Continuous Current, S or D	20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max.)	40mA
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 Seconds)	275°C

Junction Temperature	+175°C
Thermal Resistance, Junction-to-Case (θ_{JC})	180°C/W Ceramic DIP Package 40°C/W Ceramic LCC Package
Thermal Resistance, Junction-to-Ambient (θ_{JA})	500°C/W Ceramic DIP Package 81°C/W Ceramic LCC Package
Power Dissipation	2.0W Ceramic DIP Package 1.23W Ceramic LCC Package
Power Dissipation Derating Factor (Above +75°C)	20.0mW/°C Ceramic DIP Package 12.3mW/°C Ceramic LCC Package
ESD Classification	≤2000V

Recommended Operating Conditions

Operating Temperature Range	-55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$)	±15V
Analog Input Voltage (V_S)	±VSUPPLY

Logic Low Level (V_{AL})	0V to 0.8V
Logic High Level (V_{AH})	+4V to +VSUPPLY
Max RMS Current, S or D	8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at +VSUPPLY = +15V, -VSUPPLY = -15V, VEN = 4.0V, VREF (Pin 13) = OPEN, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH} I_{IL}	Measure Inputs Sequentially, Connect All Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	μA
Leakage Current Into the Source Terminal of an "OFF" Switch	+IS(OFF) -IS(OFF)	$V_S = +10V$, $V_D = -10V$, $V_{EN} = 0.8V$ All Unused Inputs = -10V $V_S = -10V$, $V_D = +10V$, $V_{EN} = 0.8V$ All Unused Inputs = +10V	1 2, 3	+25°C +125°C, -55°C	-10 -50	+10 +50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	+ID(OFF) -ID(OFF)	$V_D = +10V$, $V_{EN} = 0.8V$ All Unused Inputs = -10V HI-546/883 HI-547/883 $V_D = -10V$, $V_{EN} = 0.8V$ All Unused Inputs = +10V HI-546/883 HI-547/883	1 2, 3 2, 3 1 2, 3 2, 3	+25°C +125°C, -55°C +25°C, -55°C +25°C +125°C, -55°C +125°C, -55°C	-10 -300 -200 -10 -300 -200	+10 +300 +200 +10 +300 +200	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	+ID(ON) -ID(ON)	V_{IN} (Selected Chan.) = $V_D = +10V$ V_S = Unused Inputs = -10V HI-546/883 HI-547/883 V_{IN} (Selected Chan.) = $V_D = -10V$ V_S = Unused Inputs = +10V HI-546/883 HI-547/883	1 2, 3 2, 3 1 2, 3 2, 3	+25°C +125°C, -55°C +125°C, -55°C +25°C +125°C, -55°C +125°C, -55°C	-10 -300 -200 -10 -300 -200	+10 +300 +200 +10 +300 +200	nA
Overvoltage Protected, Leakage Current Into the Drain Terminal of an "OFF" Switch	ID(OFF) Overvoltage	$V_S = 33V$, $V_D = 0V$, $V_{EN} = 0.8V$ V_S applied at ≤ 25% duty cycle $V_S = -33V$, $V_D = 0V$, $V_{EN} = 0.8V$ V_S applied at ≤ 25% duty cycle	1, 2, 3	+25°C, +125°C, -55°C	-2.0	+2.0	μA
Positive Supply Current	I(+)	$V_A = 0V$, $V_{EN} = 4.0V$	1, 2, 3	+25°C, +125°C, -55°C		2.0	mA
Negative Supply Current	I(-)	$V_A = 0V$, $V_{EN} = 4.0V$	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Standby Positive Supply Current	+ISBY	$V_A = 0V$, $V_{EN} = 0V$	1, 2, 3	+25°C, +125°C, -55°C		2.0	mA
Standby Negative Supply Current	-ISBY	$V_A = 0V$, $V_{EN} = 0V$	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Switch "ON" Resistance	+RDS1 -RDS1	$V_S = 10V$ $I_D = 100\mu A$ $V_S = -10V$ $I_D = -100\mu A$	1 2, 3 1 2, 3	+25°C +125°C, -55°C +25°C +125°C, -55°C		1500 1800 1500 1800	Ω
Logic Level Voltage	V _{AL1} V _{AH1} V _{AL2} V _{AH2}	Notes 1, 2 Notes 1, 2 Note 3 Note 3	1, 2, 3 1, 2, 3 1, 2, 3 1, 2, 3	+25°C, +125°C, -55°C +25°C, +125°C, -55°C +25°C, +125°C, -55°C +25°C, +125°C, -55°C		4.0 0.8 6.0	V
Difference in switch "ON" Resistance Between Channels	+ΔRDS1 -ΔRDS1	$\frac{(+R_{DS1MAX}) - (+R_{DS1MIN}) \times 100}{+R_{DS1AVE}}$ $\frac{(-R_{DS1MAX}) - (-R_{DS1MIN}) \times 100}{-R_{DS1AVE}}$	1 1	+25°C +25°C		7 7	%

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at +V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V, V_{EN} = 4.0V, V_{REF} (Pin 13) = OPEN, Unless Otherwise Specified.

A.C. PARAMETER	SYMBOL	CONDITIONS	SUBGROUP	TEMP	LIMITS		UNITS
					MIN	MAX	
Break-Before-Make Time Delay	t _D	R _L = 1k Ω , C _L = 12.5pF	9	+25°C	25		ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t _A	R _L = 10M Ω , C _L = 14pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
Enable to I/O	t _{ON(EN)}	R _L = 1k Ω , C _L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
	t _{OFF(EN)}	R _L = 1k Ω , C _L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at +V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V, V_{EN} = 4.0V, V_{REF} (Pin 13) = OPEN, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS		UNITS
					MIN	MAX	
Capacitance: Address Input	C _A	V ₊ = V ₋ = 0V f = 1MHz	4	+25°C		12	pF
Capacitance: Output Switch	C _{OS}	V ₊ = V ₋ = 0V HI-546/883	4	+25°C		85	pF
		f = 1MHz HI-547/883	4	+25°C		50	pF
Capacitance Input Switch	C _{IS}	V ₊ = V ₋ = 0V f = 1MHz	4	+25°C		15	pF
Charge Transfer Error	V _{CTE}	V _S = GND V _{GEN} = 0V to 5V	4	+25°C		10	mV
Off Isolation	V _{ISO}	V _{EN} = 0.8V, R _L = 1k Ω C _L = 15pF, V _S = 7VRMS f = 100kHz	4, 5	+25°C	-50		dB

NOTES: 1. Used for forcing conditions for all DC Tests, unless otherwise specified.

2. To drive from DTL/TTL circuits, 1k Ω pull-up resistors to +5.0V supply are recommended.

3. V_{REF} = +10V.

4. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

5. Worst case isolation occurs on channel 8B due to proximity of the output pins.

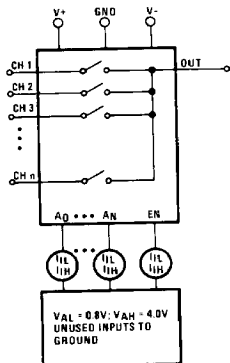
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

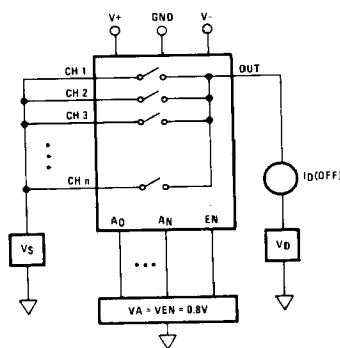
*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Test Circuits

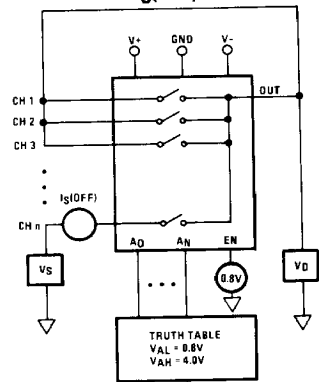
INPUT LEAKAGE CURRENT



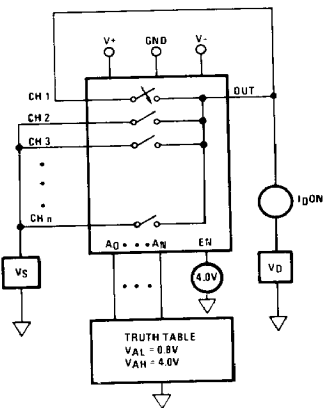
ID(OFF)



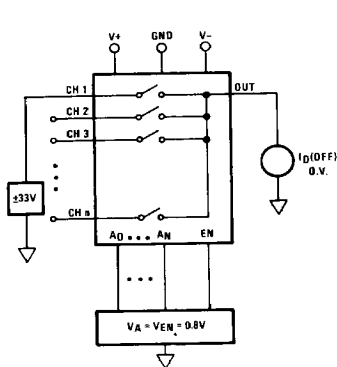
IS(OFF)



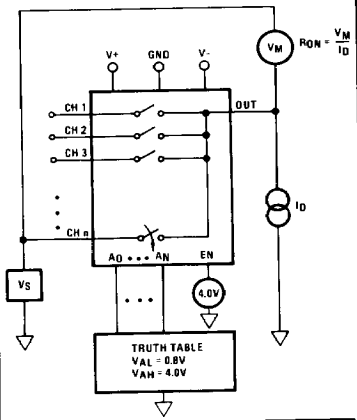
ID(ON)



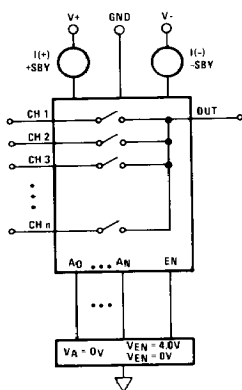
ID(OFF) OVERVOLTAGE



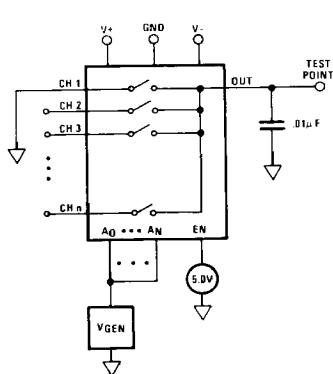
Rps



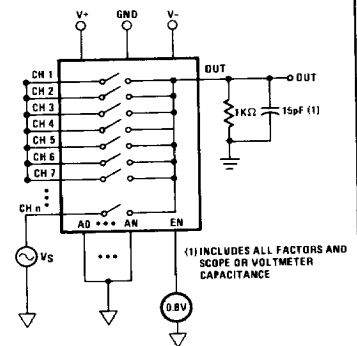
SUPPLY CURRENTS



CHARGE TRANSFER ERROR



OFF CHANNEL ISOLATION

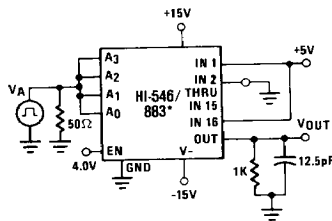
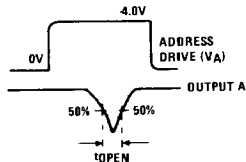


5

CMOS ANALOG
MULTIPLEXERS

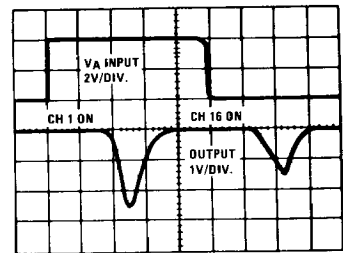
Switching Waveforms

BREAK-BEFORE-MAKE DELAY (t_{OPEN})



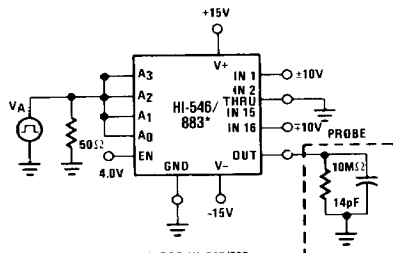
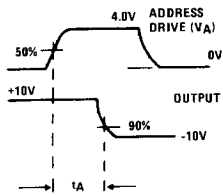
*SIMILAR CONNECTION FOR HI-547/883

BREAK-BEFORE-MAKE DELAY (t_{OPEN})



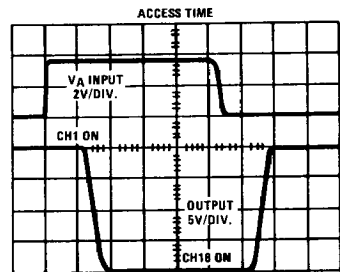
100ns/DIV.

ACCESS TIME vs. LOGIC LEVEL (HIGH)



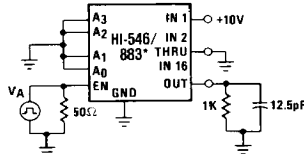
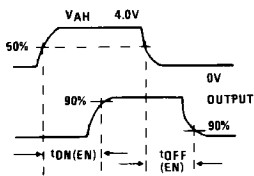
*SIMILAR CONNECTION FOR HI-547/883

ACCESS TIME



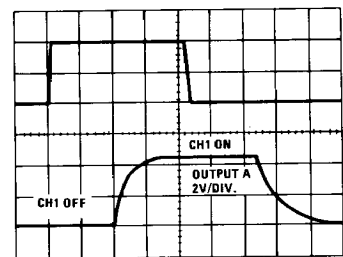
200ns/DIV.

ENABLE DELAY $t_{ON}(EN)$, $t_{OFF}(EN)$



*SIMILAR CONNECTION FOR HI-547/883

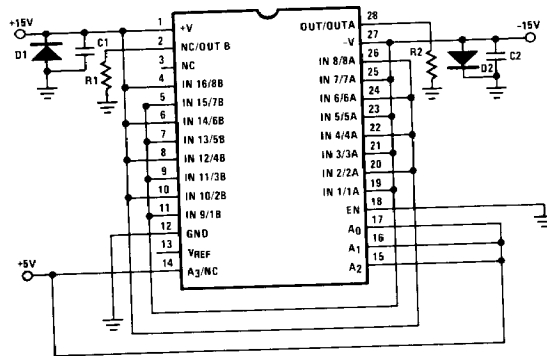
ENABLE DELAY $t_{ON}(EN)$, $t_{OFF}(EN)$



100ns/DIV.

Burn-In Circuits

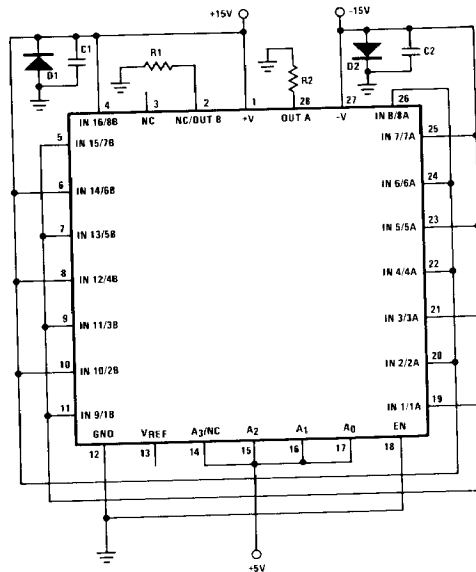
HI-546/883 HI-547/883 CERAMIC DIP



NOTES:

R1, R2 = $10k\Omega \pm 5\%$ 1/2 or 1/4W (per socket)
 C1, C2 = $0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
 D1, D2 = IN4002 (or equivalent) (per board)

HI-546/883 HI-547/883 CERAMIC LCC

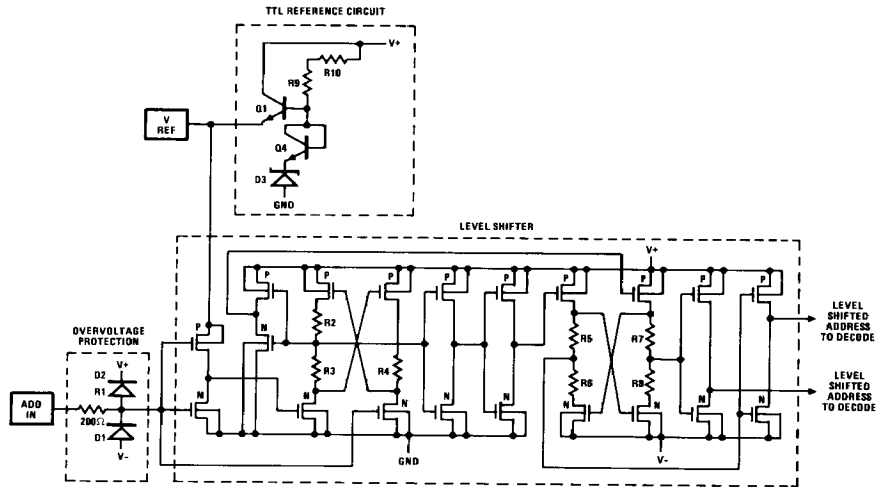


NOTES:

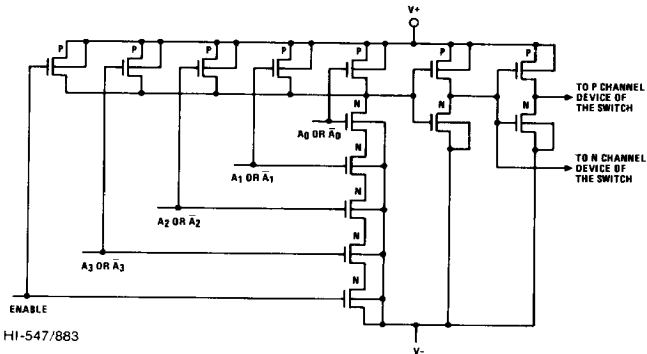
R1, R2 = $10k\Omega \pm 5\%$ 1/2 or 1/4W (per socket)
 C1, C2 = $0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
 D1, D2 = IN4002 (or equivalent) (per board)

Schematic Diagrams

ADDRESS INPUT BUFFER AND LEVEL SHIFTER

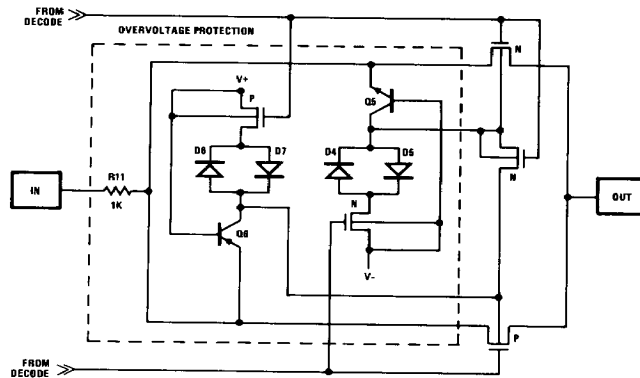


ADDRESS DECODER



Delete A_3 or $\bar{A}_3$ Inputs for HI-547/883

MULTIPLEX SWITCH



Die Characteristics

DIE DIMENSIONS: 83.9 x 159 x 19 mils

METALLIZATION

Type: Al

Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

GLASSIVATION

Type: Nitride

Thickness: $7\text{k}\text{\AA} \pm 0.7\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY: $1.4 \times 10^5 \text{ A/cm}^2$

TRANSISTOR COUNT:

HI-546/883 485

HI-547/883 485

PROCESS: CMOS-DI

DIE ATTACH

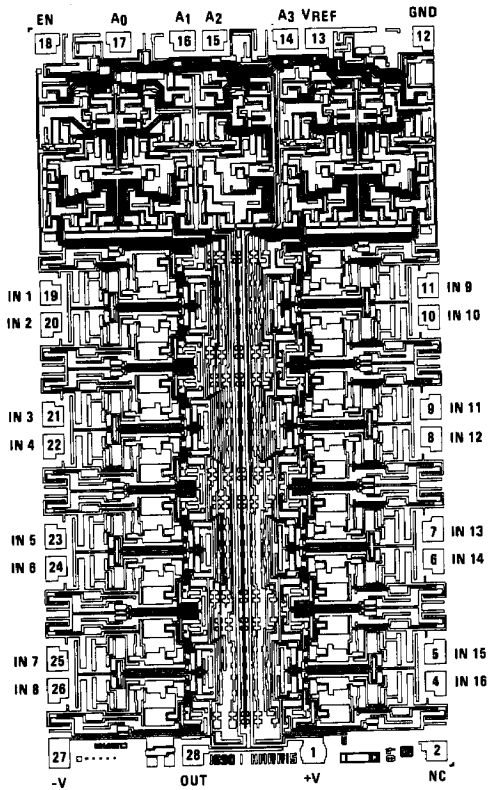
Material: Gold Silicon Eutectic Alloy

Temperature: Ceramic DIP — 460°C (Max)

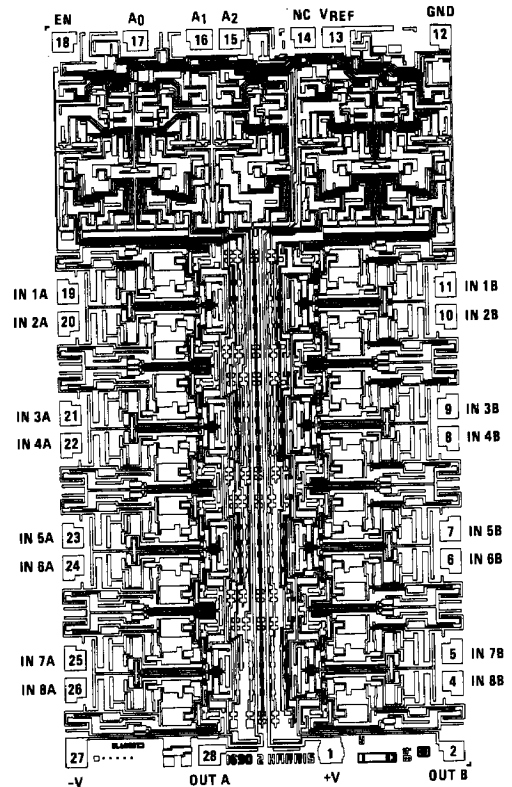
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

HI-546/883



HI-547/883



* INCREASE MAX LIMIT BY .003 INCHES

- INCREASE MAX LIMIT BY .003 INCHES
MEASURED AT CENTER OF FLAT FOR
SOLDER FINISH

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-4

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

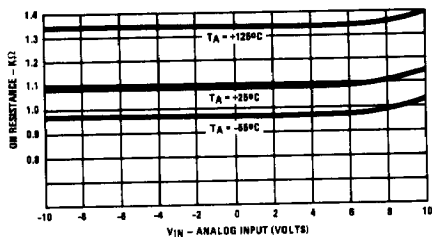
DESIGN INFORMATION

Single 16/Differential 8 Channel CMOS Analog Multiplexers With Active Overvoltage Protection

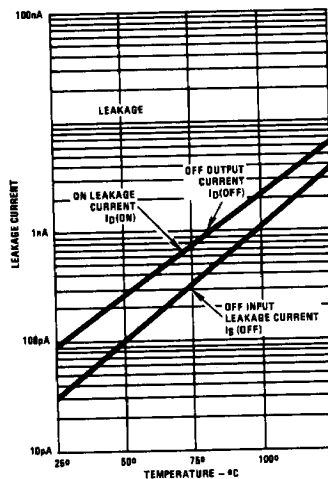
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = +4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$, $V_{\text{REF}} = \text{Open}$

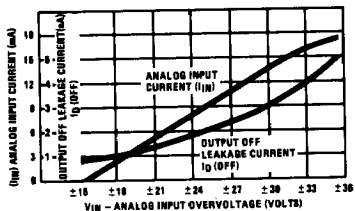
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



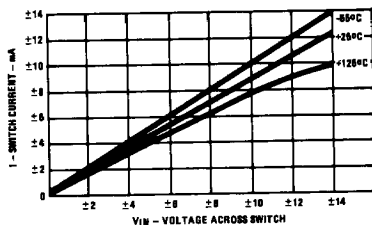
LEAKAGE CURRENT vs. TEMPERATURE



ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



ON CHANNEL CURRENT vs. VOLTAGE



SUPPLY CURRENT vs. TOGGLE FREQUENCY

