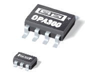


OPA300, OPA2300
OPA301, OPA2301

SBOS271B − MAY 2003 − REVISED JUNE 2005

Low-Noise, High-Speed, 16-Bit Accurate, CMOS OPERATIONAL AMPLIFIER

FEATURES

- **High Bandwidth: 150MHz**
- **16-Bit Settling in 150ns**
- **Low Noise: 3nV/√Hz**
- **Low Distortion: 0.003%**
- **Low Power: 9.5mA (typ) on 5.5V**
- **Shutdown to 5μA**
- **Unity-Gain Stable**
- **Excellent Output Swing: (V+) − 100mV to (V−) + 100mV**
- **Single Supply: +2.7V to +5.5V**
- **Tiny Packages: MSOP and SOT23**

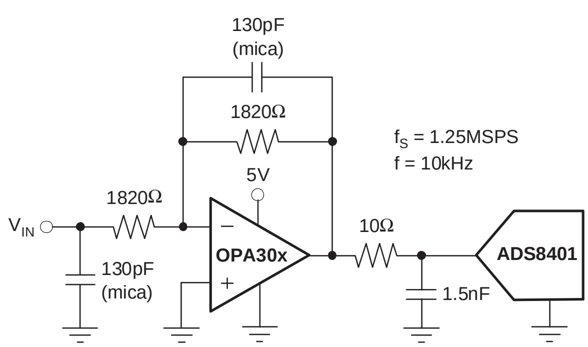
APPLICATIONS

- **16-Bit ADC Input Drivers**
- **Low-Noise Preamplifiers**
- **IF/RF Amplifiers**
- **Active Filtering**

DESCRIPTION

The OPA300 and OPA301 series high-speed, voltage-feedback, CMOS operational amplifiers are designed for 16-bit resolution systems. The OPA300/OPA301 series are unity-gain stable and feature excellent settling and harmonic distortion specifications. Low power applications benefit from low quiescent current. The OPA300 and OPA2300 feature a digital shutdown (Enable) function to provide additional power savings during idle periods. Optimized for single-supply operation, the OPA300/OPA301 series offer superior output swing and excellent common-mode range.

The OPA300 and OPA301 series op amps have 150MHz of unity-gain bandwidth, low 3nV/√Hz voltage noise, and 0.1% settling within 30ns. Single-supply operation from 2.7V (±1.35V) to 5.5V (±2.75V) and an available shutdown function that reduces supply current to 5μA are useful for portable low-power applications. The OPA300 and OPA301 are available in SO-8 and SOT-23 packages. The OPA2300 is available in MSOP-10, and the OPA2301 is available in SO-8 and MSOP-8. All versions are specified over the industrial temperature range of −40°C to +125°C.



Typical Application

SBOS271B − MAY 2003 − REVISED JUNE 2005

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA300	SO-8	D	300A
OPA300	SOT23-6	DBV	A52
OPA301	SO-8	D	301A
OPA301	SOT23-5	DBV	AUP
OPA2300	MSOP−10	DGS	C01
OPA2301	SO−8	D	OPA2301A
OPA2301	MSOP−8	DGK	C02

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

Power Supply V+ 7V
Signal Input Terminals(2), Voltage . . . . 0.5V to (V+) + 0.5V
Current . . . . ±10mA
Open Short-Circuit Current(3) . . . . Continuous
Operating Temperature Range . . . . −55°C to +125°C
Storage Temperature Range . . . . −60°C to +150°C
Junction Temperature . . . . +150°C
Lead Temperature (soldering, 10s) . . . . +300°C
ESD Ratings
Human Body Model (HBM) 4kV
Charged-Device Model (CDM) 500V

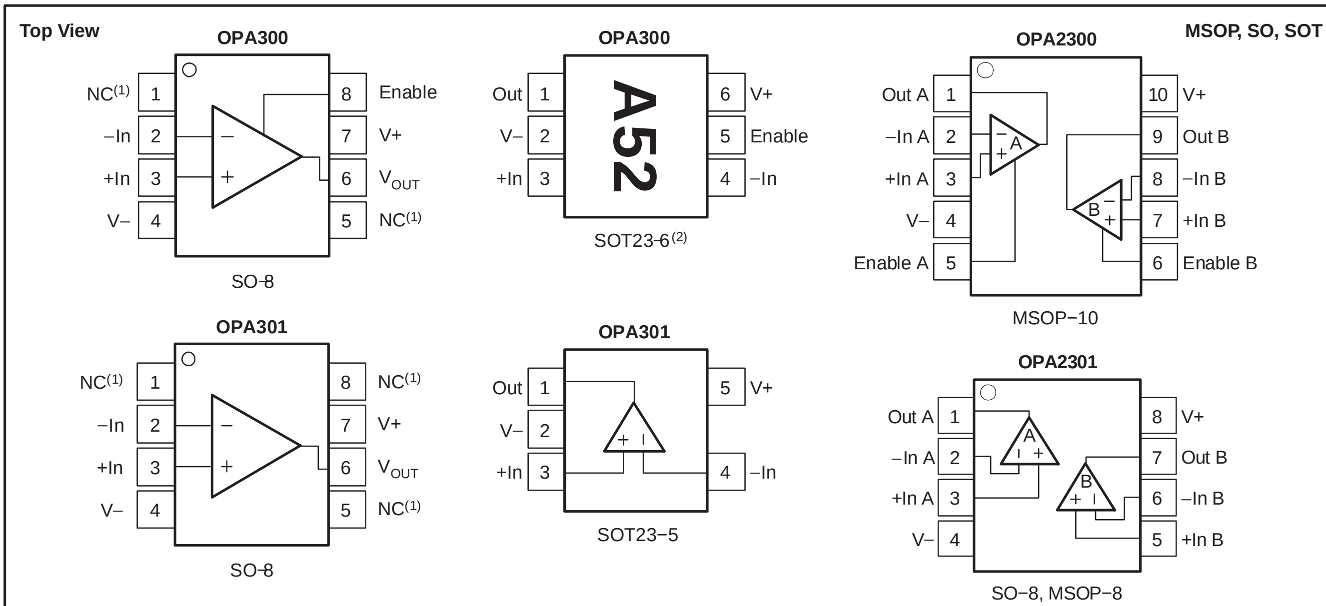
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground; one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN ASSIGNMENTS



NOTE: (1) Not connected. (2) SOT23-6 pin 1 oriented as shown with reference to package marking.

ELECTRICAL CHARACTERISTICS: V_S = 2.7V to 5.5V

Boldface limits apply over the temperature range, **T_A = −40°C to +125°C**.

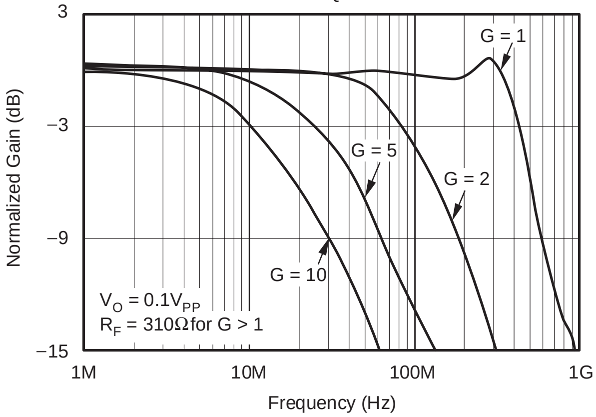
All specifications at T_A = +25°C, R_L = 2kΩ connected to V_S/2, V_{OUT} = V_S/2, and V_{CM} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA300, OPA301 OPA2300, OPA2301 MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = 5V		1	5	mV
Over Temperature					**7**	**mV**
Drift	**dV_{OS}/dT**			**2.5**		**μV/°C**
vs. Power Supply	**PSRR**	**V_S = 2.7V to 5.5V, V_{CM} < (V+) −0.9V**		**50**	**200**	**μV/V**
Channel Separation, dc				140		dB
f = 5MHz				100		dB
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) − 0.2		(V+) − 0.9	V
Common-Mode Rejection Ratio	**CMRR**	**(V−) − 0.2V < V_{CM} < (V+) − 0.9V**	**66**	**80**		**dB**
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.1	±5	pA
Input Offset Current	I_{OS}			±0.5	±5	pA
INPUT IMPEDANCE						
Differential				10^{13} || 3		Ω || pF
Common-Mode				10^{13} || 6		Ω || pF
NOISE						
Input Voltage Noise, f = 0.1Hz to 1MHz				40		μV_{PP}
Input Voltage Noise Density, f > 1MHz	e_n			3		$nV/\sqrt{Hz}$
Input Current Noise Density, f < 1kHz	i_n			1.5		$fA/\sqrt{Hz}$
Differential Gain Error		NTSC, R_L = 150Ω		0.01		%
Differential Phase Error		NTSC, R_L = 150Ω		0.1		°
OPEN-LOOP GAIN						
Open−Loop Voltage Gain	A_{OL}	V_S = 5V, R_L = 2kΩ, 0.1V < V_O < 4.9V	95	106		dB
Over Temperature		**V_S = 5V, R_L = 2kΩ, 0.1V < V_O < 4.9V**	**90**			**dB**
		V_S = 5V, R_L = 100Ω, 0.5V < V_O < 4.5V	95	106		dB
Over Temperature		**V_S = 5V, R_L = 100Ω, 0.5V < V_O < 4.5V**	**90**			**dB**
OUTPUT						
Voltage Output Swing from Rail		R_L = 2kΩ, A_{OL} > 95dB		75	100	mV
		R_L = 100Ω, A_{OL} > 95dB		300	500	mV
Short-Circuit Current	I_{SC}			70		mA
Capacitive Load Drive	C_{LOAD}			See Typical Characteristics		
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			150		MHz
Slew Rate	SR	G = +1		80		V/μs
Settling Time, 0.01%	t_S	V_S = 5V, 2V Step, G = +1		90		ns
0.1%				30		ns
Overload Recovery Time		Gain = −1		30		ns
Total Harmonic Distortion + Noise	THD+N	V_S = 5V, V_O = $3V_{PP}$, G = +1, f = 1kHz		0.003		%
POWER SUPPLY						
Specified Voltage Range	V_S		2.7		5.5	V
Operating Voltage Range				2.7 to 5.5		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		9.5	12	mA
Over Temperature					**13**	**mA**
SHUTDOWN						
t_{OFF}				40		ns
t_{ON}				5		μs
V_L (shutdown)			(V−) − 0.2		(V−) + 0.8	V
V_H (amplifier is active)			(V−) + 2.5		(V+) + 0.2	V
I_{QSD} (per amplifier)				3	10	μA
TEMPERATURE RANGE						
Specified Range			−40		+125	°C
Operating Range			−55		+125	°C
Storage Range			−60		+150	°C
Thermal Resistance	θ_{JA}					°C/W
SO-8, MSOP−8, MSOP-10				150		°C/W
SOT23-5, SOT23-6				200		°C/W

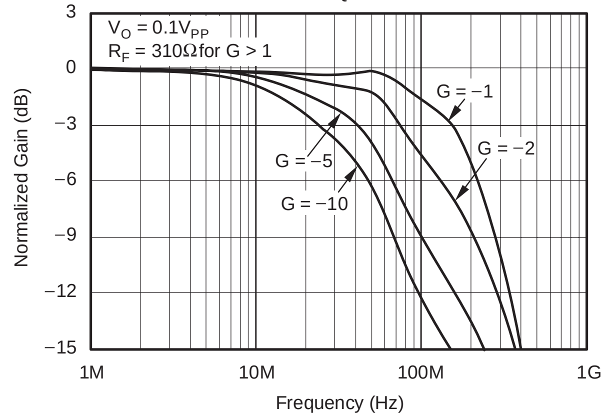
TYPICAL CHARACTERISTICS

All specifications at $T_A = 25°C$, $V_S = 5V$, and $R_L = 150\Omega$ connected to $V_S/2$ unless otherwise noted.

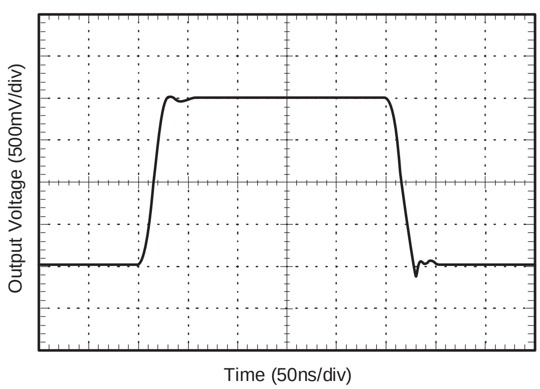
NONINVERTING GAIN SMALL−SIGNAL FREQUENCY RESPONSE



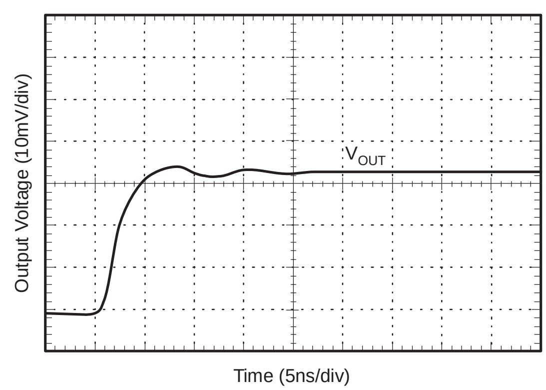
INVERTING GAIN SMALL−SIGNAL FREQUENCY RESPONSE



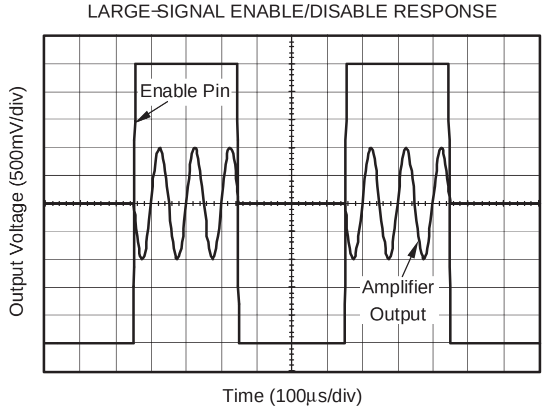
LARGE−SIGNAL STEP RESPONSE



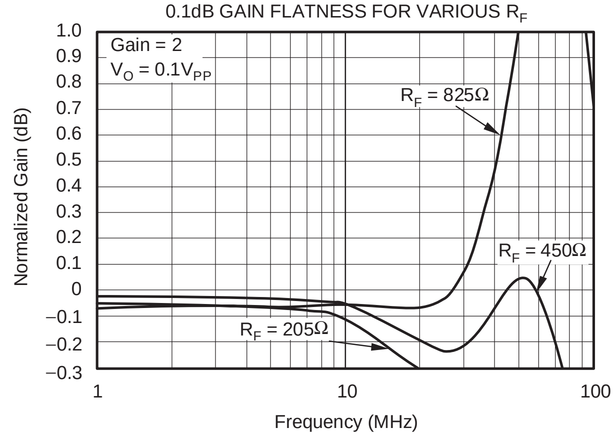
SMALL−SIGNAL STEP RESPONSE



LARGE−SIGNAL ENABLE/DISABLE RESPONSE

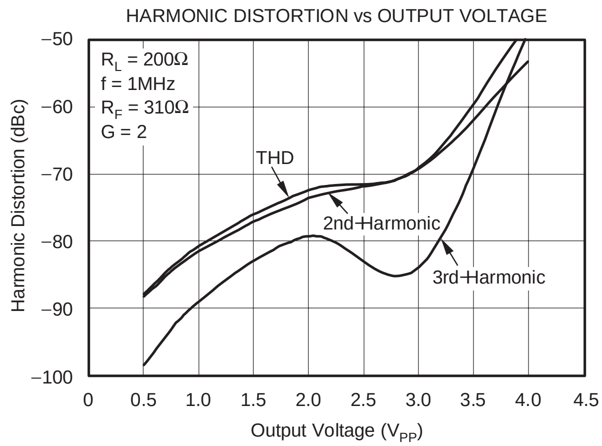


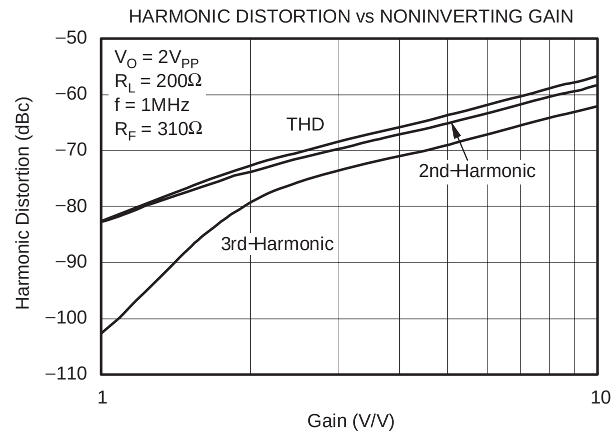
0.1dB GAIN FLATNESS FOR VARIOUS R_F

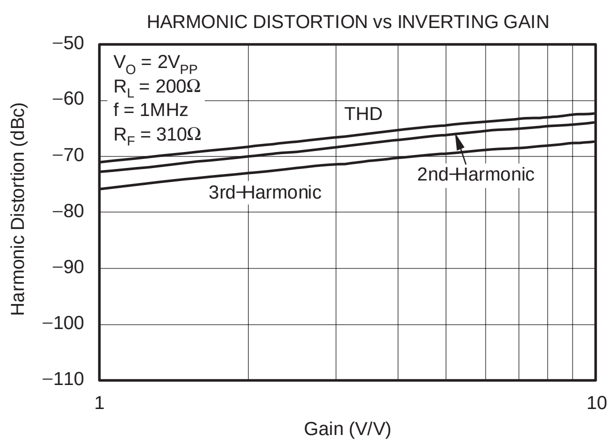


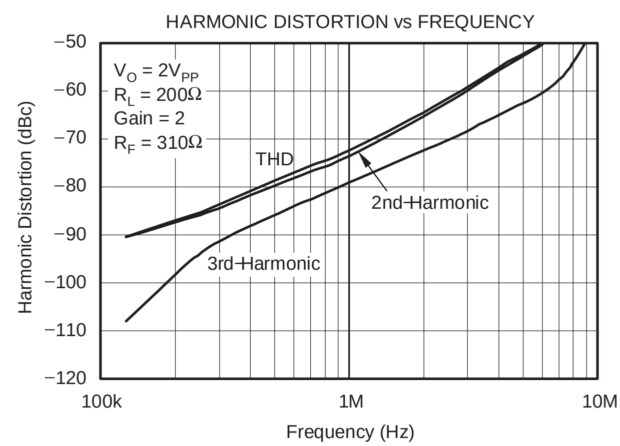
TYPICAL CHARACTERISTICS (continued)

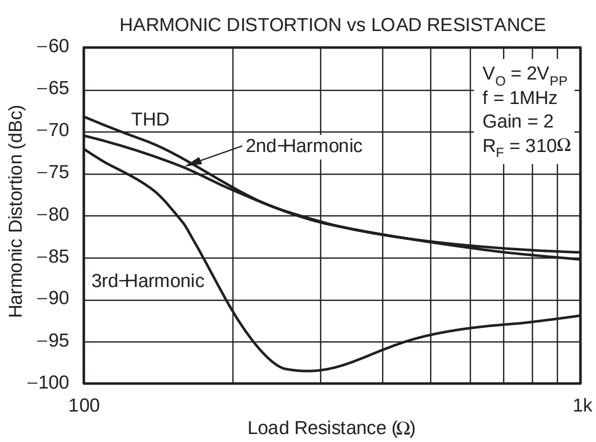
All specifications at T_A = 25°C, V_S = 5V, and R_L = 150Ω connected to V_S/2 unless otherwise noted.

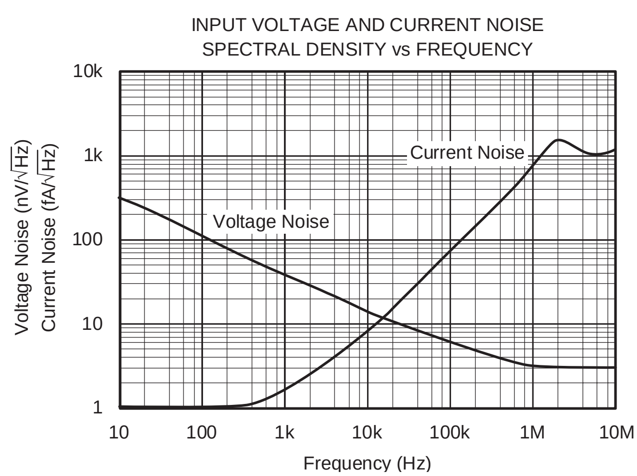








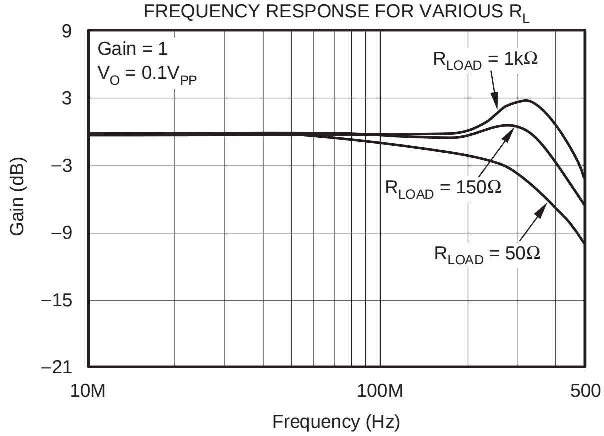




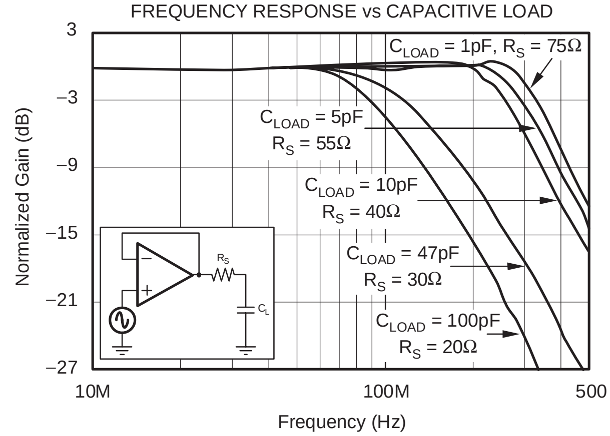
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_S = 5V, and R_L = 150Ω connected to V_S/2 unless otherwise noted.

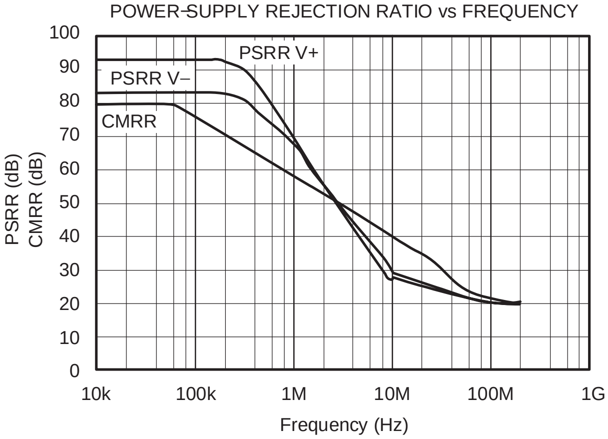
FREQUENCY RESPONSE FOR VARIOUS R_L



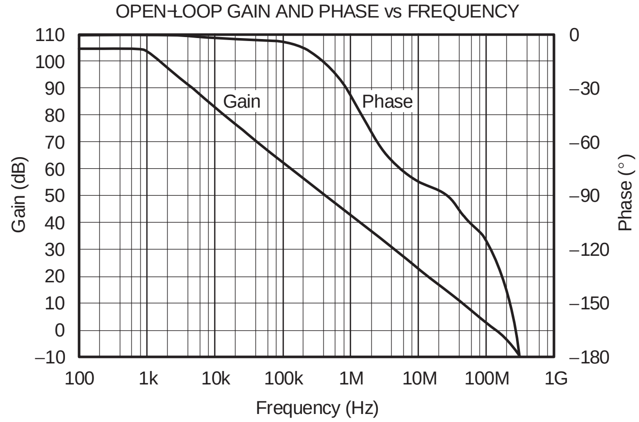
FREQUENCY RESPONSE vs CAPACITIVE LOAD



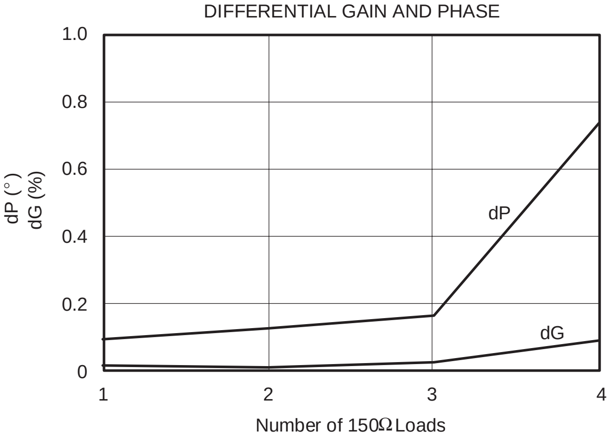
COMMON−MODE REJECTION RATIO AND
POWER−SUPPLY REJECTION RATIO vs FREQUENCY



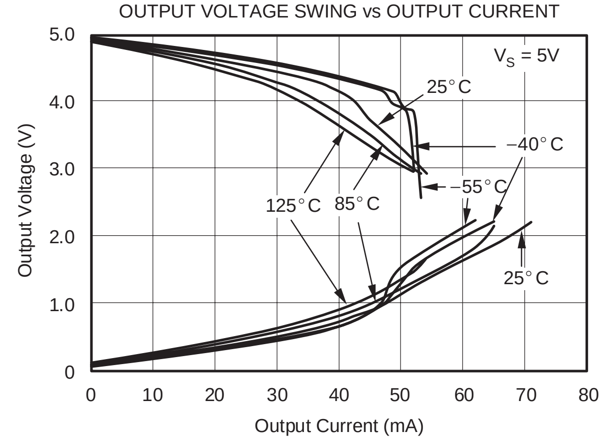
OPEN−LOOP GAIN AND PHASE vs FREQUENCY



COMPOSITE VIDEO
DIFFERENTIAL GAIN AND PHASE



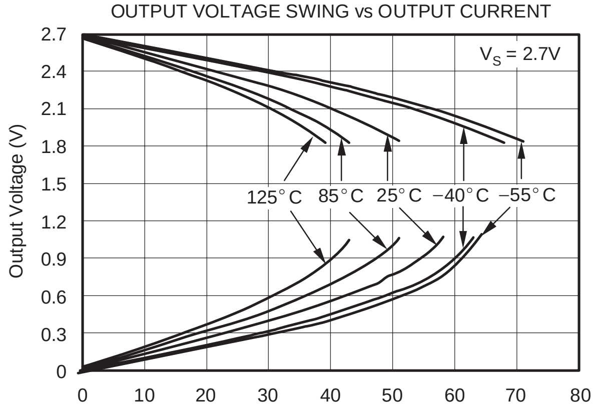
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



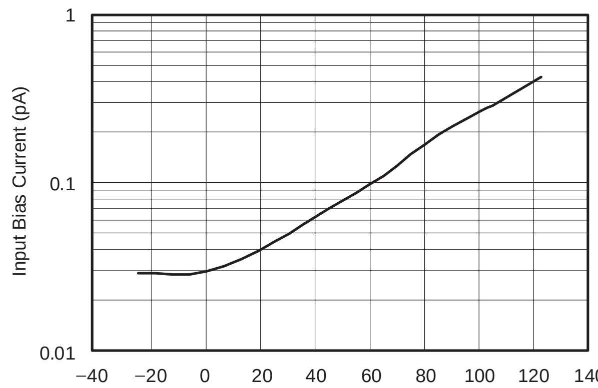
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_S = 5V, and R_L = 150Ω connected to V_S/2 unless otherwise noted.

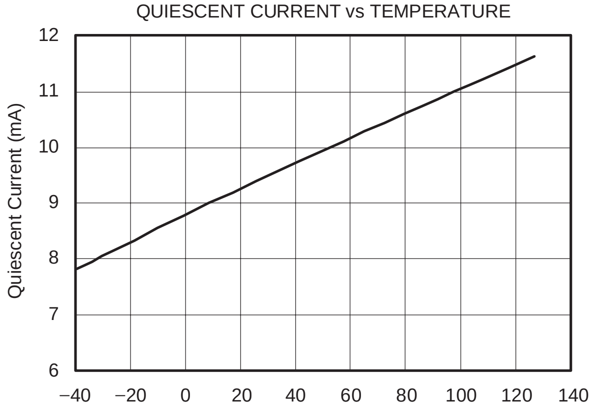
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



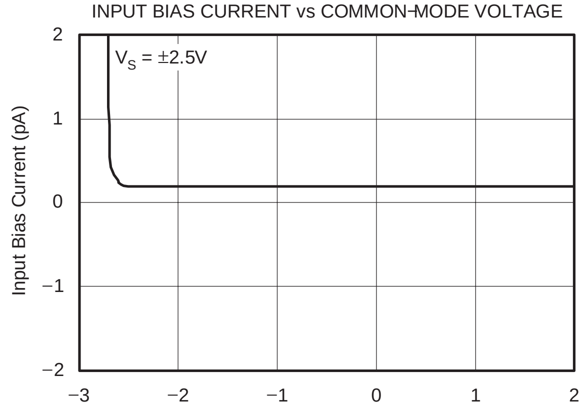
INPUT BIAS CURRENT vs TEMPERATURE



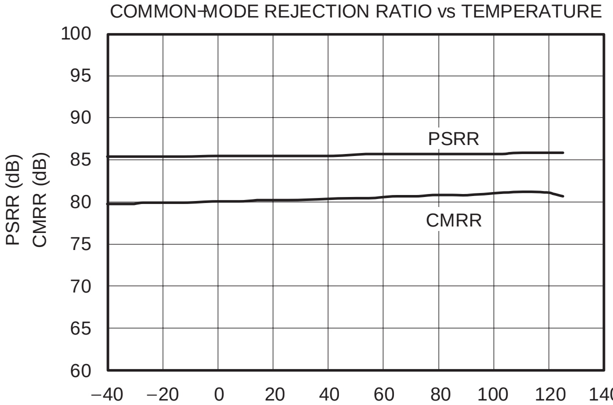
QUIESCENT CURRENT vs TEMPERATURE



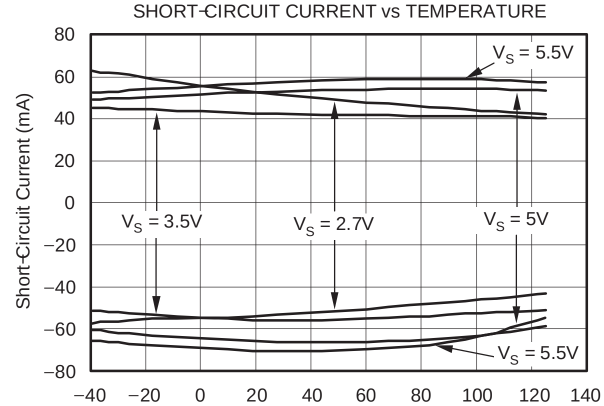
INPUT BIAS CURRENT vs COMMON−MODE VOLTAGE



POWER−SUPPLY REJECTION RATIO AND
COMMON−MODE REJECTION RATIO vs TEMPERATURE



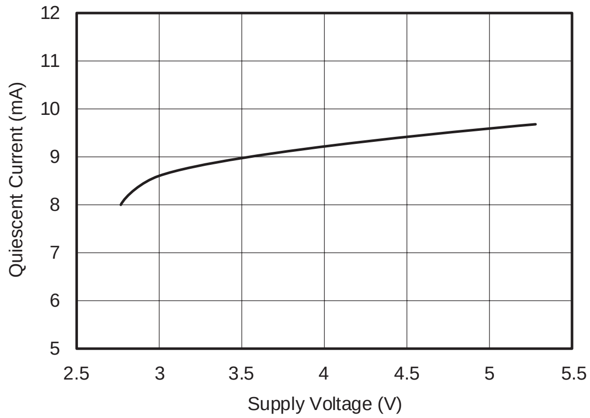
SHORT−CIRCUIT CURRENT vs TEMPERATURE



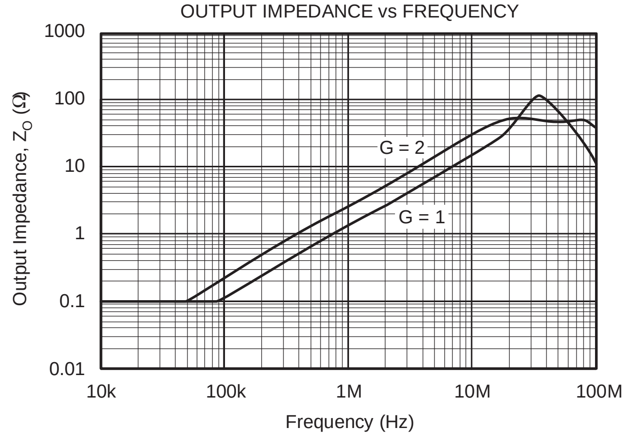
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_S = 5V, and R_L = 150Ω connected to V_S/2 unless otherwise noted.

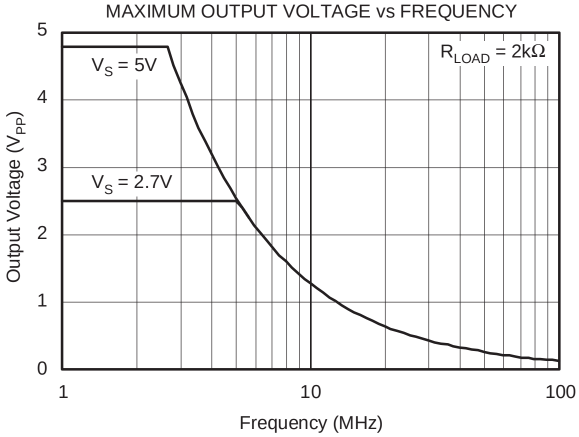
QUIESCENT CURRENT vs SUPPLY VOLTAGE



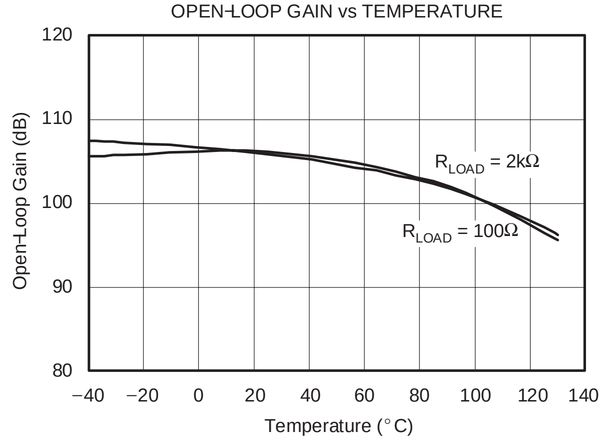
OUTPUT IMPEDANCE vs FREQUENCY



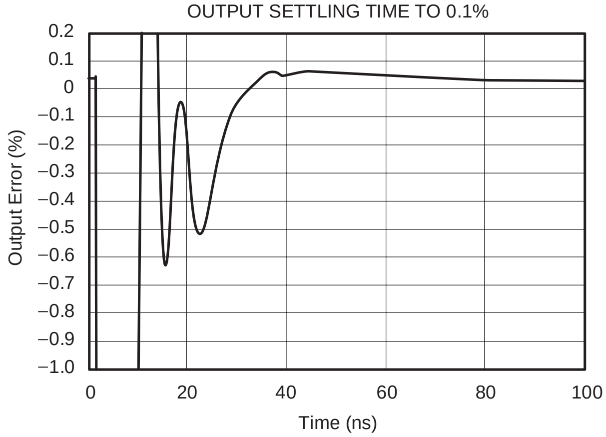
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



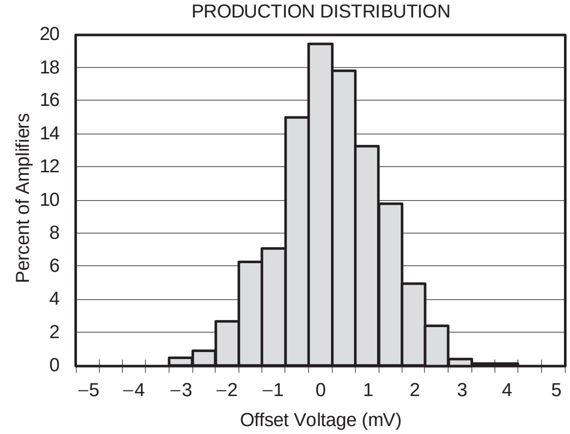
OPEN-LOOP GAIN vs TEMPERATURE



OUTPUT SETTLING TIME TO 0.1%

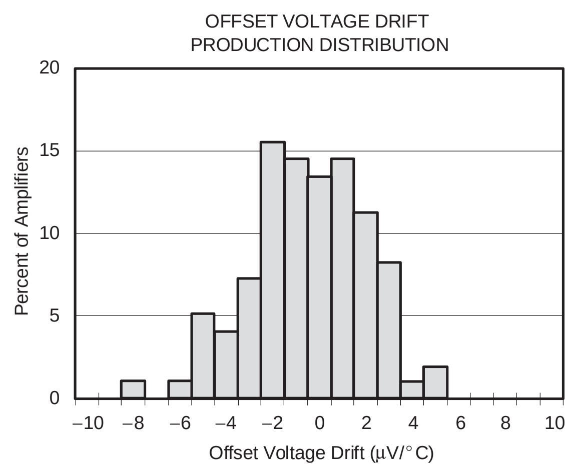


OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_S = 5V, and R_L = 150Ω connected to V_S/2 unless otherwise noted.



APPLICATIONS INFORMATION

The OPA300 and OPA301 series of single-supply CMOS op amps are designed to interface with high-speed 16-bit analog-to-digital converters (ADCs). Featuring wide 150MHz bandwidth, fast 150ns settling time to 16 bits, and high open loop gain, this series offers excellent performance in a small SO-8 and tiny SOT23 packages.

THEORY OF OPERATION

The OPA300 and OPA301 series op amps use a classic two-stage topology, shown in Figure 1. The differential input pair is biased to maximize slew rate without compromising stability or bandwidth. The folded cascode adds the signal from the input pair and presents a differential signal to the class AB output stage. The class AB output stage allows rail- to-rail output swing, with high-impedance loads (> 2kΩ), typically 100mV from the supply rails. With 10Ω loads, a useful output swing can be achieved and still maintain high open-loop gain. See the typical characteristic *Output Voltage Swing vs Output Current.*

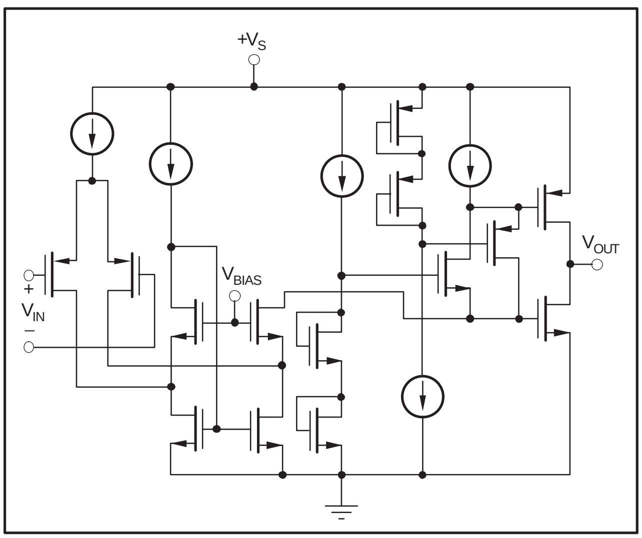


Figure 1. OPA30x Classic Two-Stage Topology

OPERATING VOLTAGE

OPA300/OPA301 series op amp parameters are fully specified from +2.7V to +5.5V. Supply voltages higher than 5.5V (absolute maximum) can cause permanent damage to the amplifier. Many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

PCB LAYOUT

As with most high-speed operational amplifiers, board layout requires special attention to maximize AC and DC performance. Extensive use of ground planes, short lead lengths, and high-quality bypass capacitors will minimize leakage that can compromise signal quality. Guard rings applied with potential as near to the input pins as possible help minimize board leakage.

INPUT AND ESD PROTECTION

All OPA300/OPA301 series op amps' pins are static-protected with internal ESD protection diodes tied to the supplies, as shown in Figure 2. These diodes will provide overdrive protection if the current is externally limited to 10mA, as stated in the Absolute Maximum Ratings. Any input current beyond the Absolute Maximum Ratings, or long-term operation at maximum ratings, will shorten the lifespan of the amplifier.

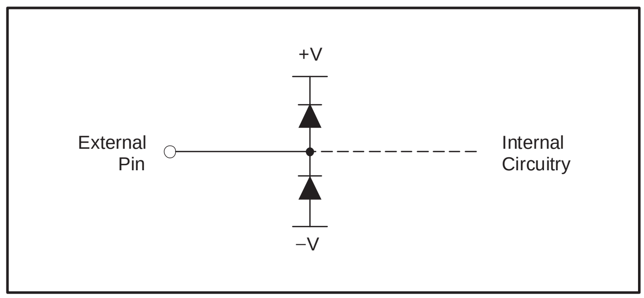


Figure 2. ESD Protection Diodes

ENABLE FUNCTION

The shutdown function of the OPA300 and OPA2300 is referenced to the negative supply voltage of the operational amplifier. A logic level HIGH enables the op amp. A valid logic HIGH is defined as 2.5V above the negative supply applied to the enable pin. A valid logic LOW is defined as < 0.8V above the negative supply pin. If dual or split power supplies are used, care should be taken to ensure logic input signals are properly referred to the negative supply voltage. If this pin is not connected to a valid high or low voltage, the internal circuitry will pull the node high and enable the part to function.

The logic input is a high-impedance CMOS input. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10μs; disable time is 1μs. When disabled, the output assumes a high-impedance state. This allows the OPA300 to be operated as a gated amplifier, or to have its output multiplexed onto a common analog output bus.

DRIVING CAPACITIVE LOADS

When using high-speed operational amplifiers, it is extremely important to consider the effects of capacitive loading on amplifier stability. Capacitive loading will interact with the output impedance of the operational amplifier, and depending on the capacitor value, may significantly decrease the gain bandwidth, as well as introduce peaking. To reduce the effects of capacitive loading and allow for additional capacitive load drive, place a series resistor between the output and the load. This will reduce available bandwidth, but permit stable operation with capacitive loading. Figure 3 illustrates the recommended relationship between the resistor and capacitor values.

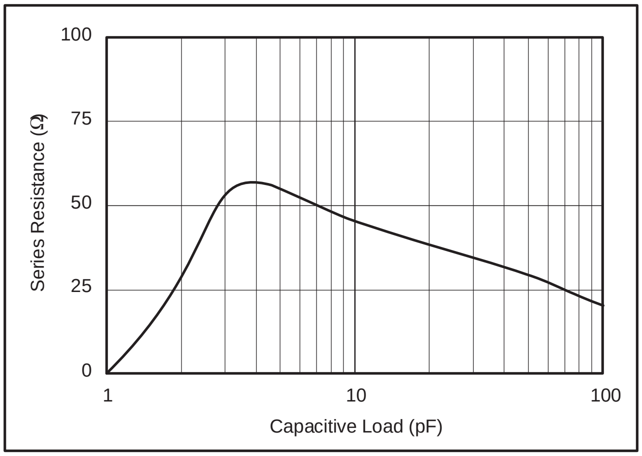


Figure 3. Recommended R_S and C_L Combinations

Amplifiers configured in unity gain are most susceptible to stability issues. The typical characteristic, *Frequency Response vs Capacitive Load,* describes the relationship between capacitive load and stability for the OPA300/OPA301 series. In unity gain, the OPA300/OPA301 series is capable of driving a few picofarads of capacitive load without compromising stability. Board level parasitic capacitance can often fall into the range of a picofarad or more, and should be minimized through good circuit-board layout practices to avoid compromising the stability of the OPA300/OPA301. For more information on detecting parasitics during testing, see the Application Note *Measuring Board Parasitics in High-Speed Analog Design* (SBOA094), available at the TI web site www.ti.com.

DRIVING A 16-BIT ADC

The OPA300/OPA301 series feature excellent THD+noise, even at frequencies greater than 1MHz, with a 16-bit settling time of 150ns. Figure 4 shows a total single supply solution for high-speed data acquisition. The OPA300/OPA301 directly drives the ADS8401, a 1.25 mega sample per second (MSPS) 16-bit data converter. The OPA300/OPA301 is configured in an inverting gain of 1, with a 5V single supply. Results of the OPA300/OPA301 performance are summarized in Table 1.

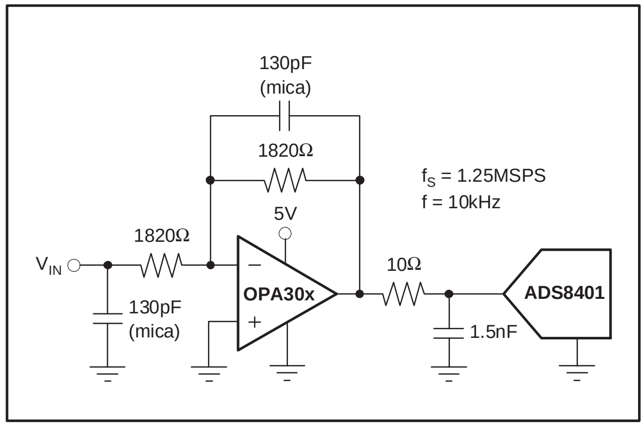


Figure 4. The OPA30x Drives the 16-Bit ADS8401

PARAMETER	RESULTS (f = 10kHz)
THD	−99.3dB
SFDR	101.2dB
THD+N	84.2dB
SNR	84.3dB

Table 1. OPA30x Performance Results Driving a 1.25MSPS ADS8401

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
OPA2300AIDGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2300AIDGSRG4	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2300AIDGST	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2300AIDGSTG4	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2301AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2301AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2301AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2301AIDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2301AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2301AIDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2301AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2301AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA300AID	ACTIVE	SOIC	D	8	100	TBD	CU NIPDAU	Level-3-235C-168 HR
OPA300AIDBVR	ACTIVE	SOT-23	DBV	6	3000	TBD	CU SNPB	Level-2-240C-1 YEAR
OPA300AIDBVT	ACTIVE	SOT-23	DBV	6	250	TBD	CU SNPB	Level-2-240C-1 YEAR
OPA300AIDR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-3-235C-168 HR
OPA301AID	ACTIVE	SOIC	D	8	100	TBD	CU NIPDAU	Level-3-240C-168 HR
OPA301AIDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-235C-UNLIM
OPA301AIDBVT	ACTIVE	SOT-23	DBV	5	250	TBD	CU NIPDAU	Level-1-235C-UNLIM
OPA301AIDR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-3-240C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder

temperature.

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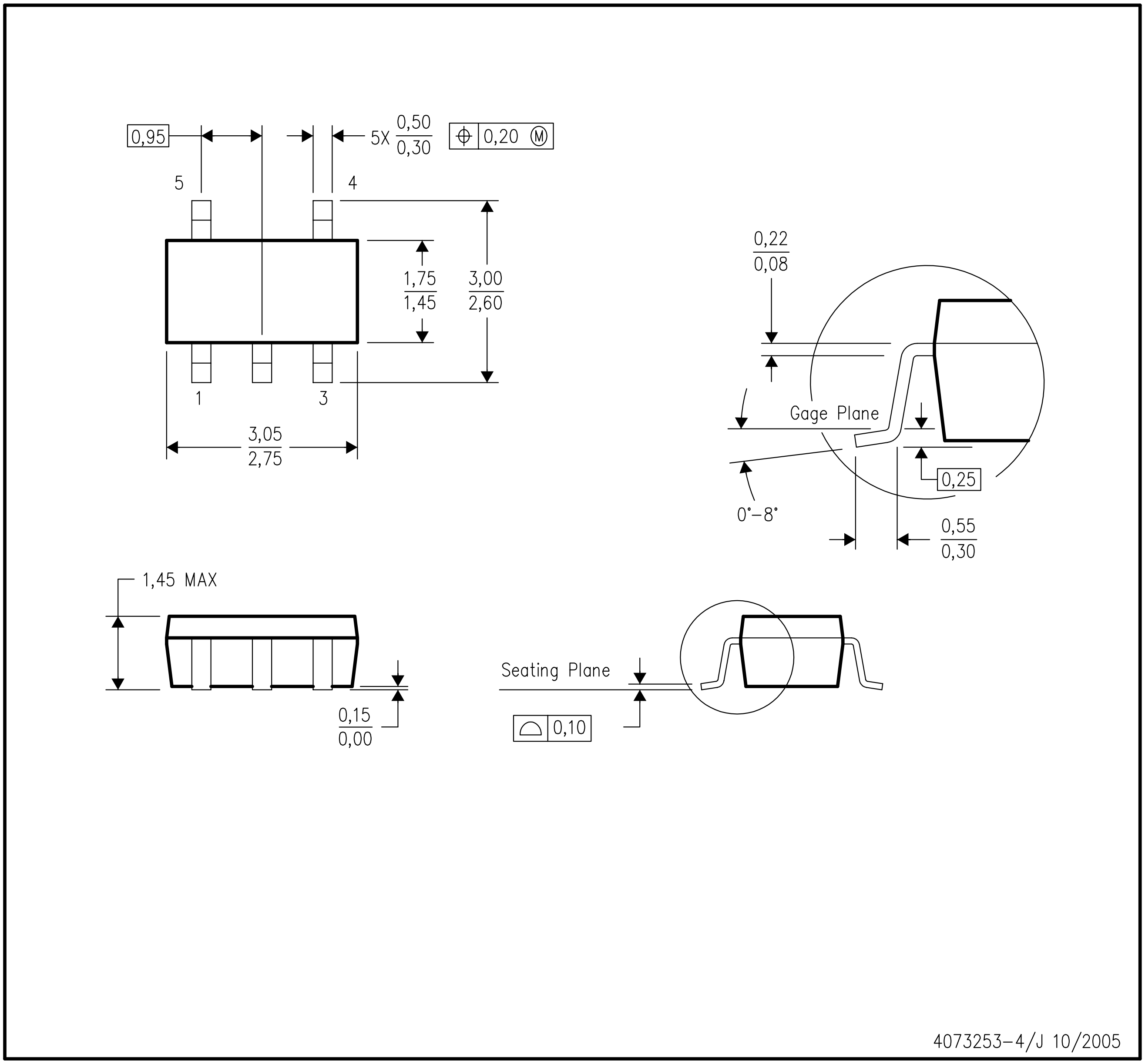
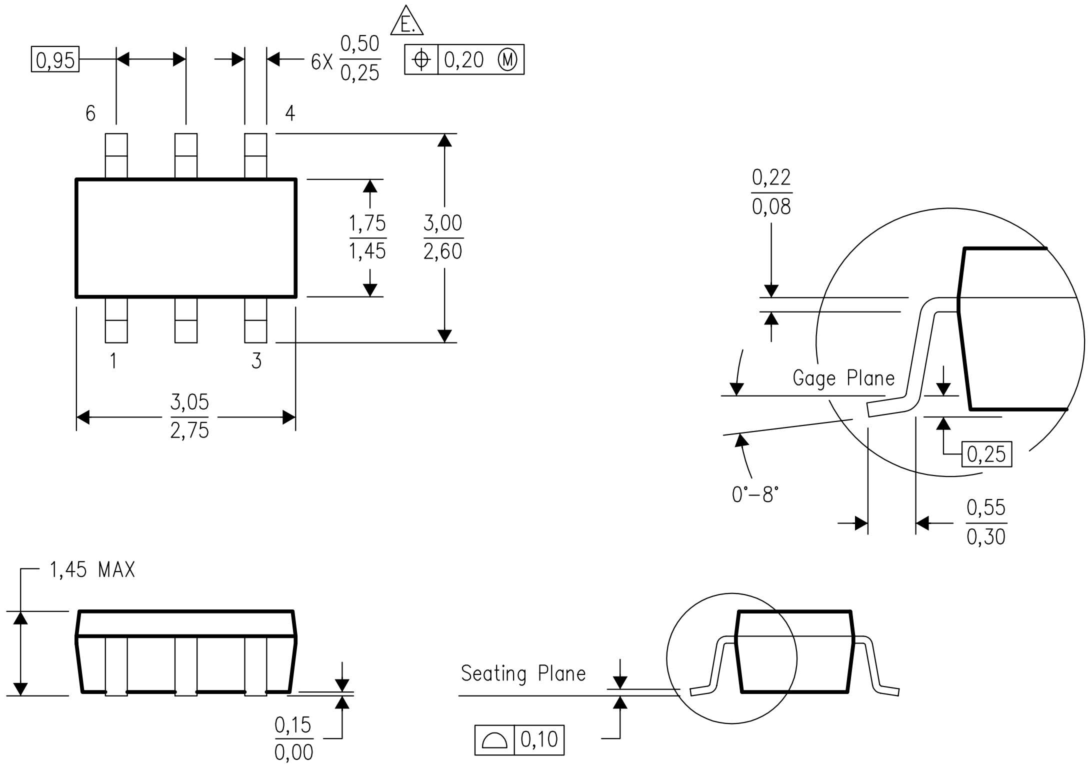
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



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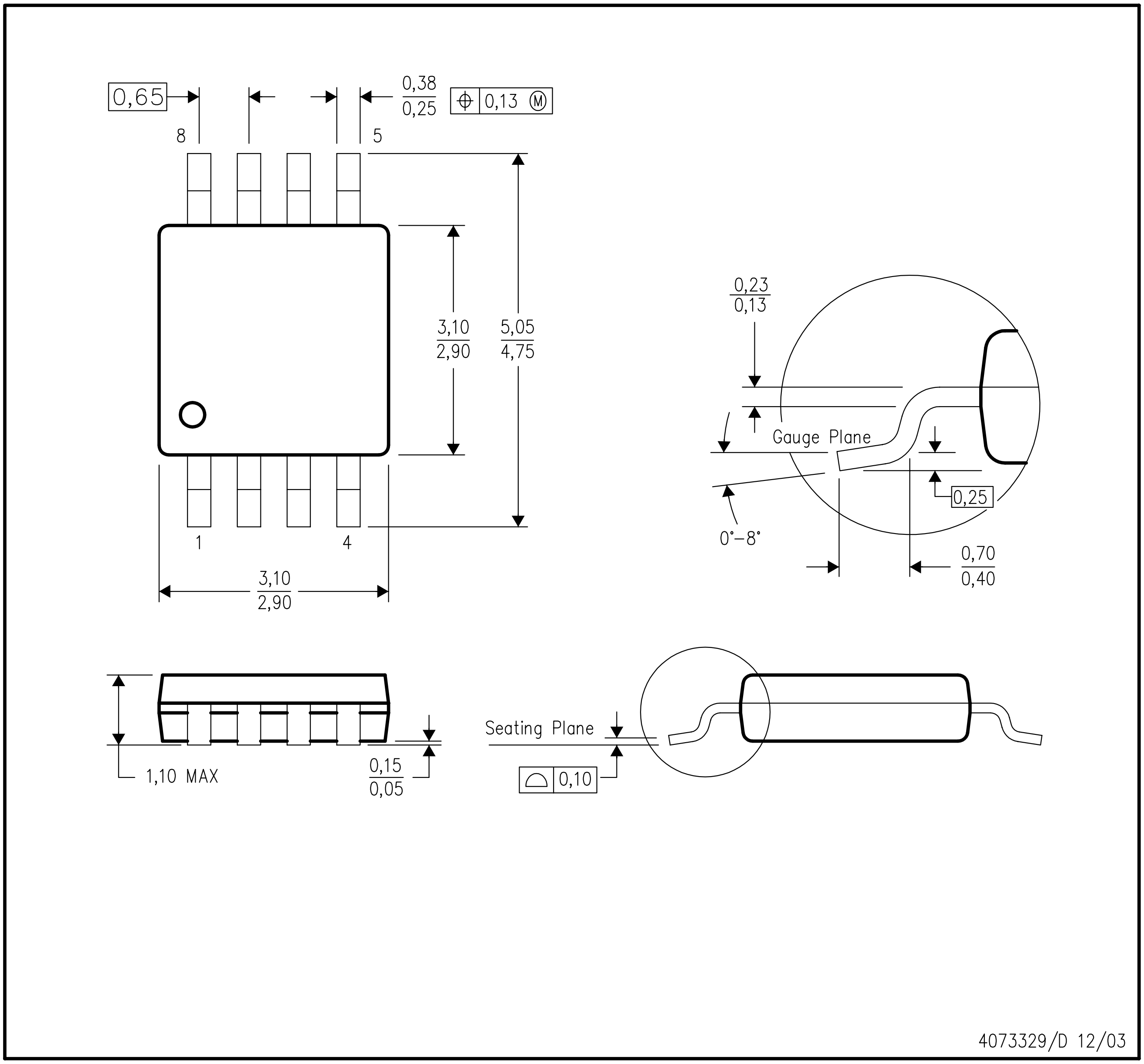
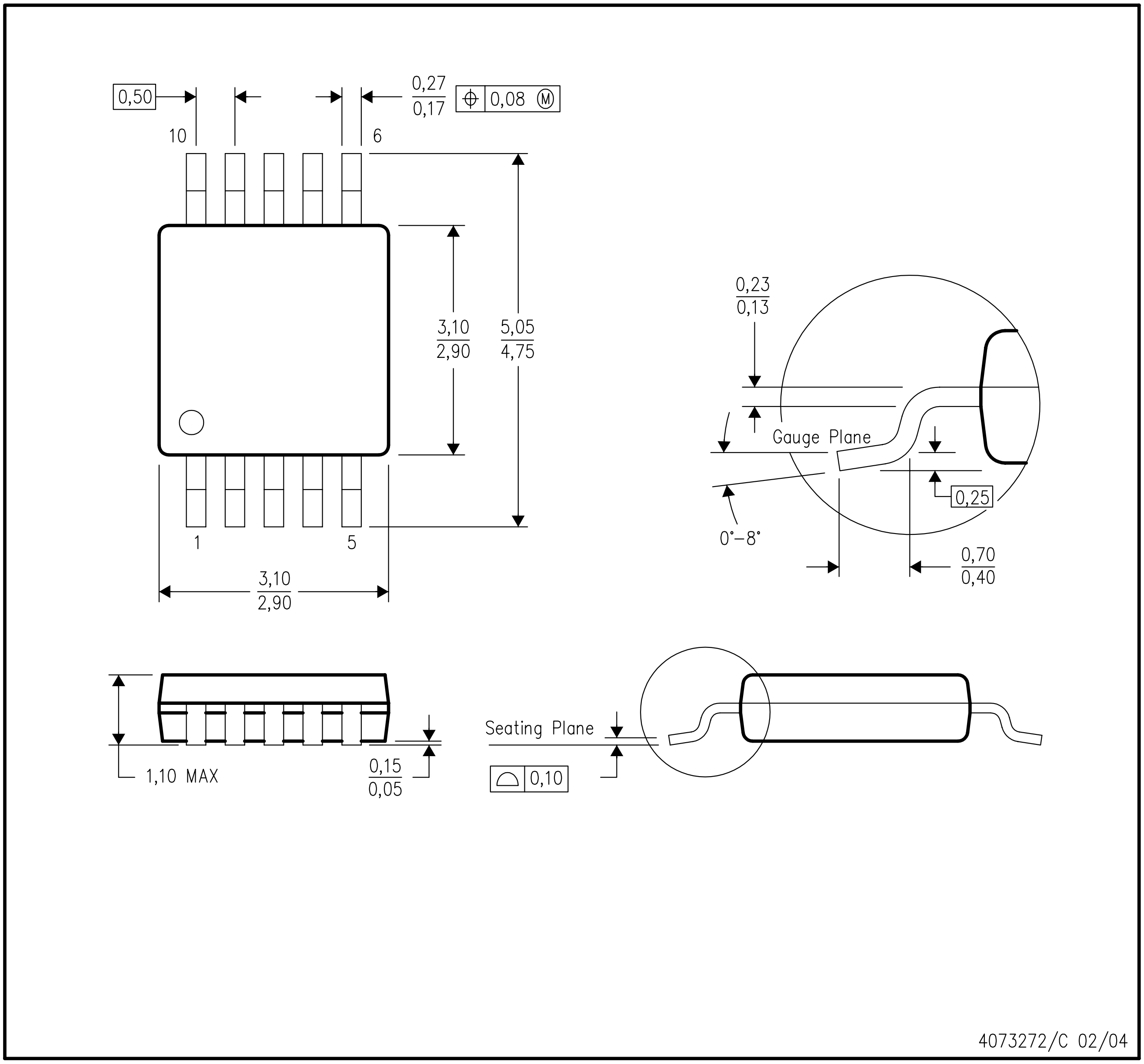
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



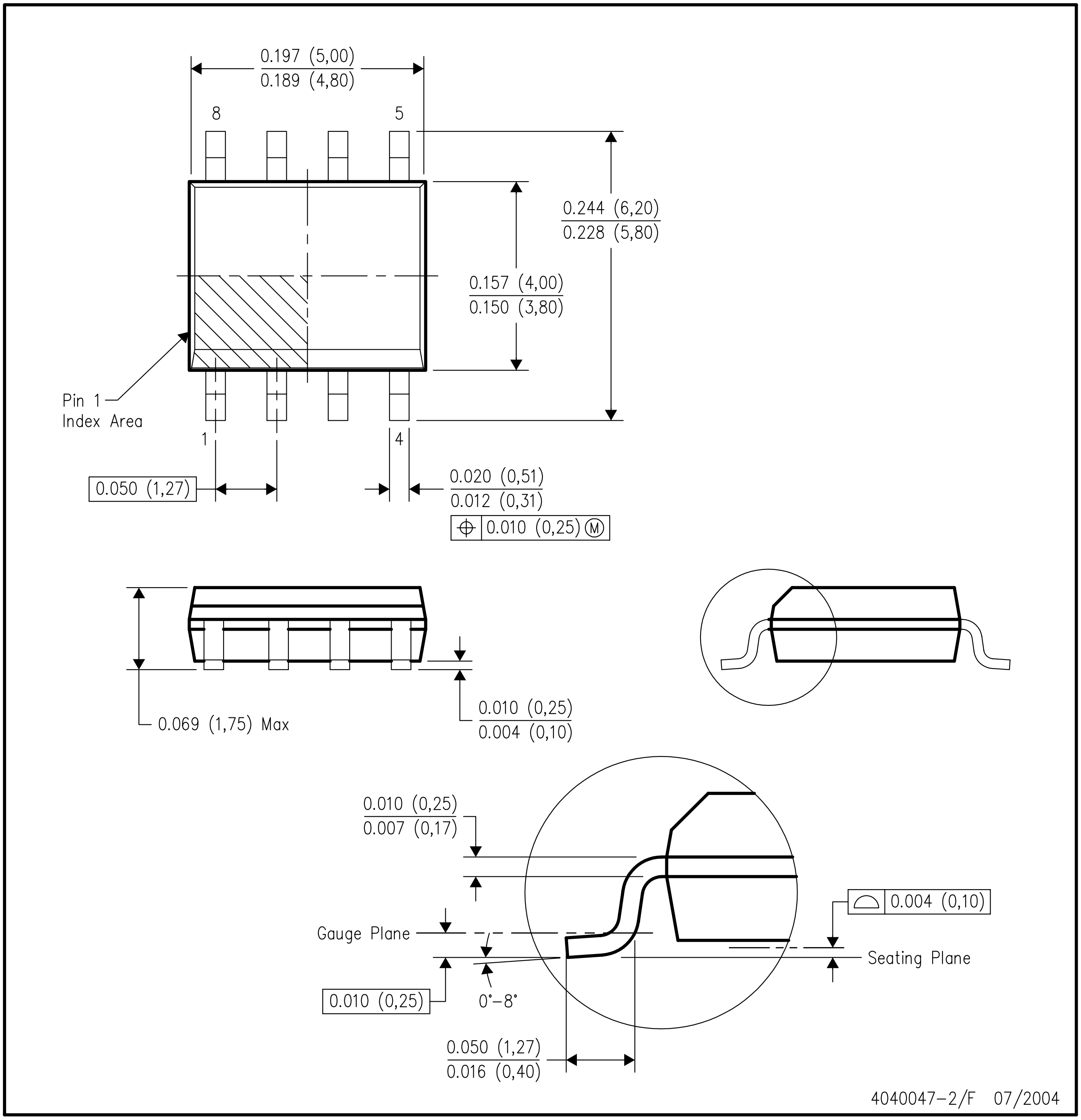
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation AA.

DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation BA.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AA.

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