

7542 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0006-0200Z
Rev.2.00
2003.04.21

DESCRIPTION

The 7542 Group is the 8-bit microcomputer based on the 740 family core technology.

The 7542 Group has serial I/Os, 8-bit timers, 16-bit timers, and an A-D converter, and is useful for control of home electric appliances and office automation equipment.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time .. **0.25 μ s (Target Spec.)**
(at 8 MHz oscillation frequency, double-speed mode for the shortest instruction)
- Memory size
 - Flash memory version: ROM 32K + 4K bytes
 - RAM 1024 bytes
 - Mask ROM version: ROM 8K to 16K bytes
 - RAM 384 to 512 bytes
 - RSS version RAM 1024 bytes
- Programmable I/O ports 29 (25 in 32-pin version)
- Interrupts 18 sources, 16 vectors
(14 sources, 14 vectors in 32-pin version)
- Timers 8-bit \times 2
..... 16-bit \times 2
- Output compare 4-channel
- Input capture 2-channel
- Serial I/O 8-bit \times 2 (UART or Clock-synchronized)
- A-D converter 10-bit \times 8 channels
..... (6 channels in 32-pin version)
- Clock generating circuit Built-in type
(low-power dissipation by a ring oscillator)
(connected to external ceramic resonator or quartz-crystal oscillator permitting RC oscillation)

- Watchdog timer 16-bit \times 1
- Power source voltage
 - XIN oscillation frequency at ceramic oscillation, in double-speed mode
At 8 MHz **TBD**
 - XIN oscillation frequency at ceramic oscillation, in high-speed mode
At 8 MHz 4.0 to 5.5 V
 - At 4 MHz 2.4 to 5.5 V
 - At 2 MHz 2.2 to 5.5 V
 - XIN oscillation frequency at RC oscillation in high-speed mode or middle-speed mode
At 4 MHz 4.0 to 5.5 V
 - At 2 MHz 2.4 to 5.5 V
 - At 1 MHz 2.2 to 5.5 V
- Power dissipation **TBD**
- Operating temperature range -20 to 85 °C
(-40 to 85 °C for extended operating temperature version)
(-40 to 125 °C for extended operating temperature 125 °C version (**Note 1**))

Notes 1: In this version, the operating temperature range and total time are limited as follows;

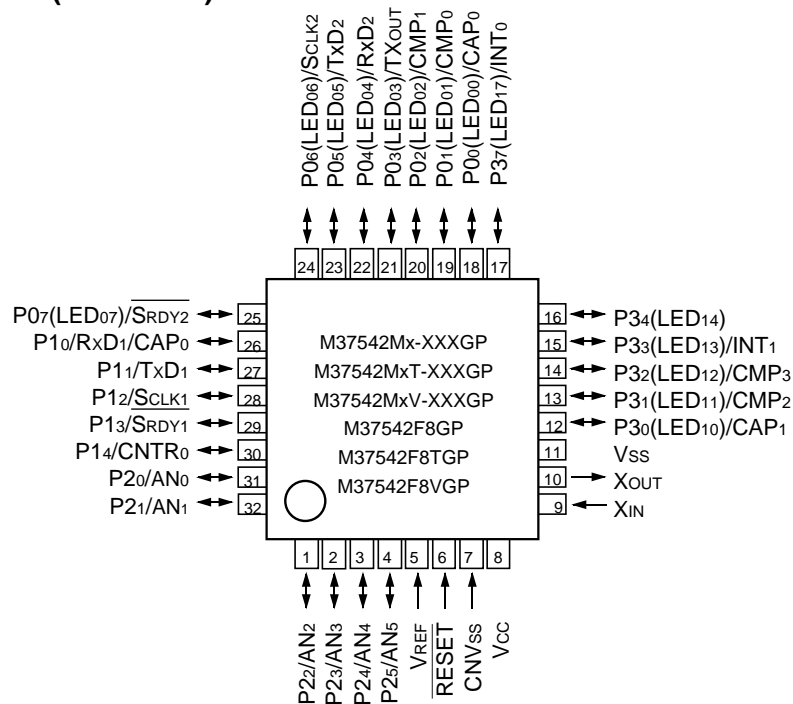
55 °C to 85 °C: within total 6000 hours,
85 °C to 125 °C: within total 1000 hours.

2: This is not a final specification. Some parametric limits are subject to change. Please contact Renesas or an authorized Renesas product distributor in the case of examination of use.

APPLICATION

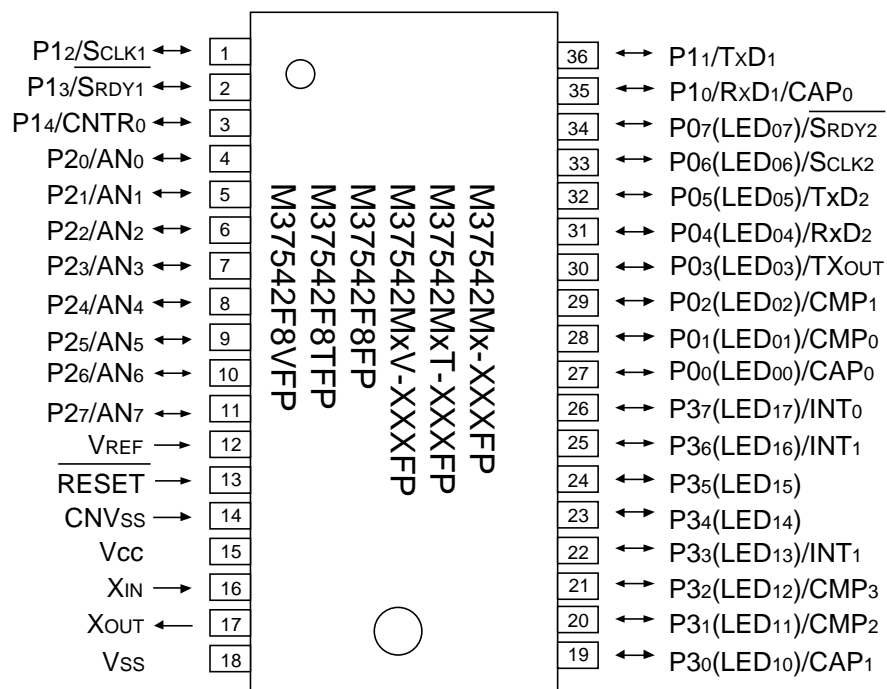
Office automation equipment, factory automation equipment, home electric appliances, consumer electronics, car, etc.

PIN CONFIGURATION (TOP VIEW)



Package type: 32P6U-A

Fig. 1 Pin configuration (Package type: 32P6U-A)



Package type: 36P2R-A

Fig. 2 Pin configuration (Package type: 36P2R-A)

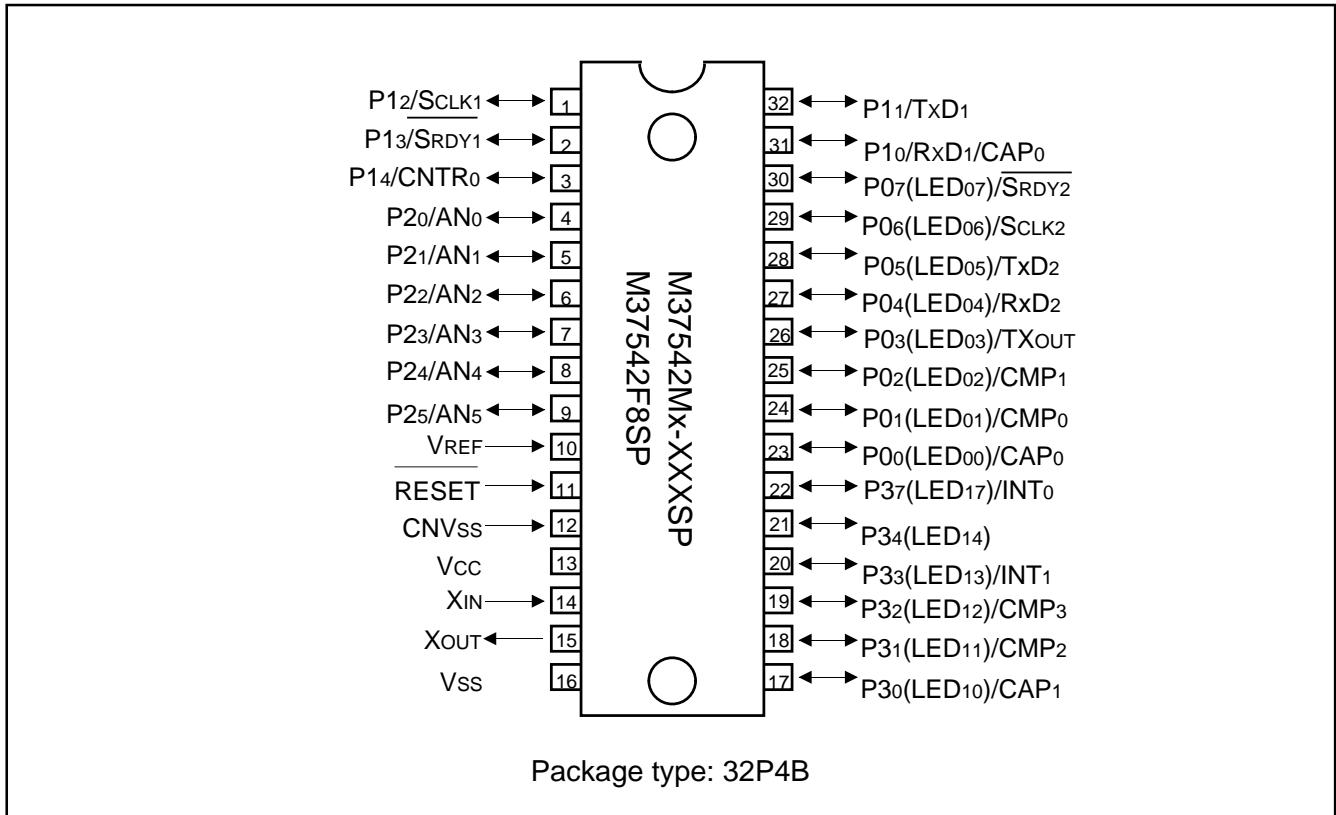


Fig. 3 Pin configuration (Package type: 32P4B)

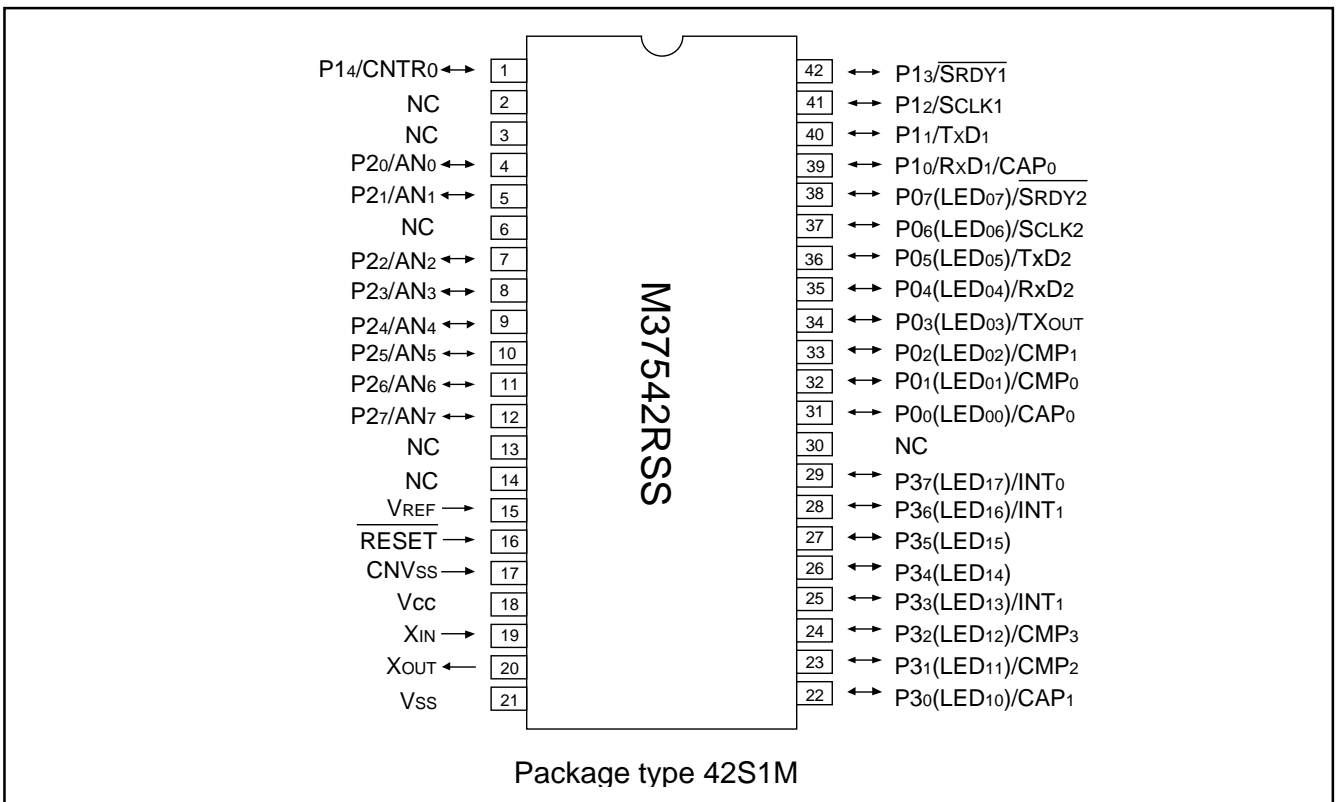


Fig. 4 Pin configuration (Package type: 42S1M)

FUNCTIONAL BLOCK

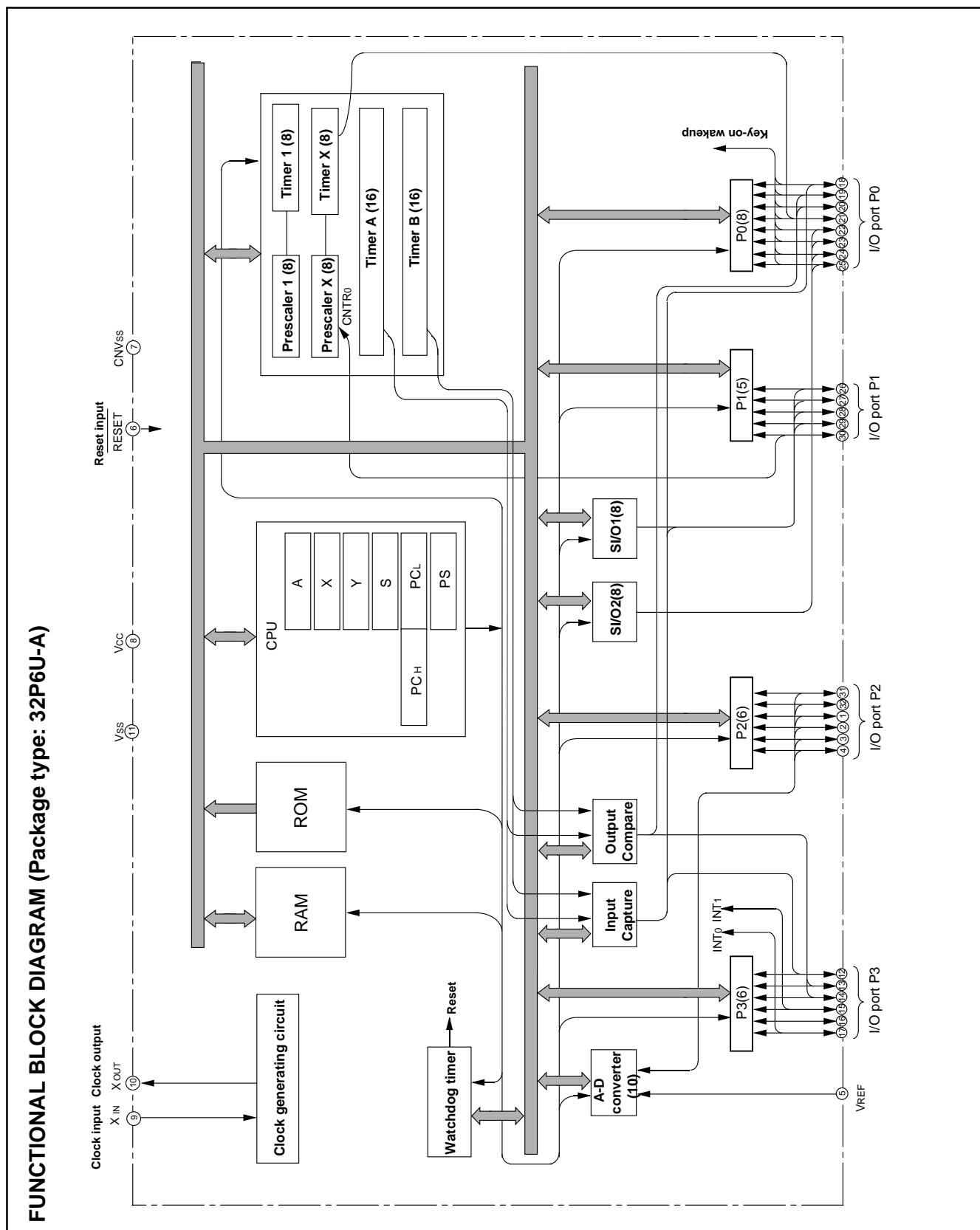


Fig. 5 Functional block diagram (Package type: 32P6U-A)

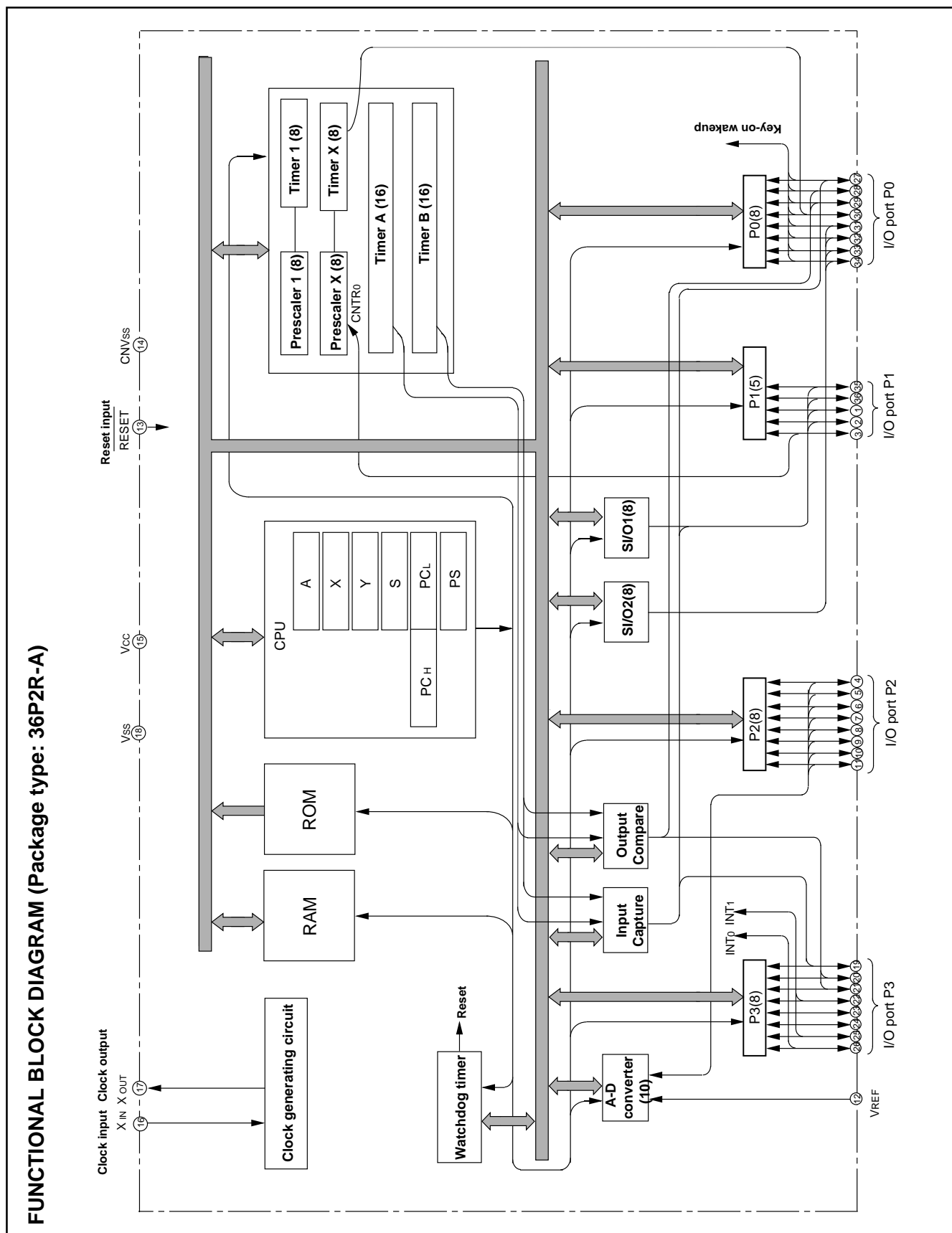


Fig. 6 Functional block diagram (Package type: 36P2R-A)

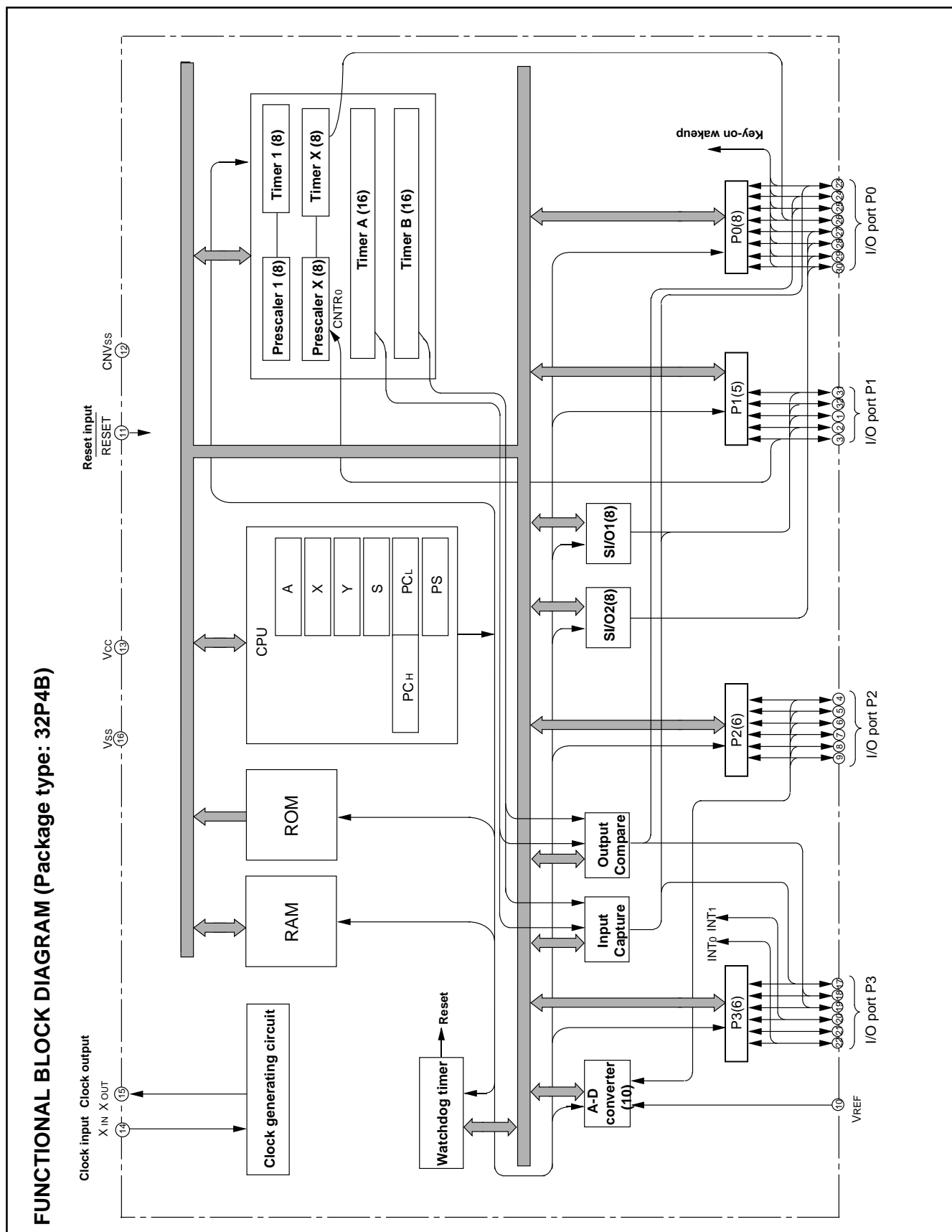


Fig. 7 Functional block diagram (Package type: 32P4B)

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	Function expect a port function	
Vcc, Vss	Power source (Note 1)	•Apply voltage of 2.2 to 5.5 V to Vcc, and 0 V to Vss.		
VREF	Analog reference voltage	•Reference voltage input pin for A-D converter.		
CNVss	CNVss	•Chip operating mode control pin, which is always connected to Vss.		
RESET	Reset input	•Reset input pin for active "L"		
XIN	Clock input	•Input and output pins for main clock generating circuit. •Connect a ceramic resonator or quartz crystal oscillator between the XIN and XOUT pins. •For using RC oscillator, short between the XIN and XOUT pins, and connect the capacitor and resistor. •If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. •When the ring oscillator is selected as the main clock, connect XIN pin to VCC and leave XOUT open.		
XOUT	Clock output			
P00(LED00)/CAP0	I/O port P0	•8-bit I/O port.	• Capture function pin	• Key-input (key-on wake up interrupt input) pin
P01(LED01)/CMP0		•I/O direction register allows each pin to be individually programmed as either input or output.	• Compare function pin	
P02(LED02)/CMP1		•CMOS compatible input level	• Timer X function pin	
P03(LED03)/TXOUT		•CMOS 3-state output structure	• Serial I/O2 function pin	
P04(LED04)/RxD2		•Whether a built-in pull-up resistor is to be used or not can be determined by program.		
P05(LED05)/TxD2		• High drive capacity for LED drive port can be selected by program.		
P06(LED06)/SCLK2				
P07(LED07)/SRDY2				
P10/RxD1/CAP0	I/O port P1	•5-bit I/O port	• Serial I/O1 function pin	
P11/TxD1		•I/O direction register allows each pin to be individually programmed as either input or output.	• Capture function pin	
P12/SCLK1		•CMOS compatible input level	• Serial I/O1 function pin	
P13/SRDY1		•CMOS 3-state output structure		
P14/CNTR0		•CMOS/TTL level can be switched for P10, P12 and P13	• Timer X function pin	
P20/AN0–P27/AN7	I/O port P2 (Note 2)	•8-bit I/O port having almost the same function as P0 •CMOS compatible input level •CMOS 3-state output structure	• Input pins for A-D converter	
P30(LED10)/CAP1	I/O port P3 (Note 3)	•8-bit I/O port	• Capture function pin	
P31(LED11)/CMP2		•I/O direction register allows each pin to be individually programmed as either input or output.	• Compare function pin	
P32(LED12)/CMP3		•CMOS compatible input level (CMOS/TTL level can be switched for P36 and P37).	• Interrupt input pin	
P33(LED13)/INT1		•CMOS 3-state output structure		
P34(LED14)		•Whether a built-in pull-up resistor is to be used or not can be determined by program.		
P35(LED15)		• High drive capacity for LED drive port can be selected by program.		
P36(LED16)/INT1			• Interrupt input pin	
P37(LED17)/INT0				

Notes 1: Vcc = 2.4 to 5.5 V for the extended operating temperature version and the extended operating temperature 125 °C version.

2: P26/AN6 and P27/AN7 do not exist for the 32-pin version, so that Port P2 is a 6-bit I/O port.

3: P35 and P36/INT1 do not exist for the 32-pin version, so that Port P3 is a 6-bit I/O port.

GROUP EXPANSION

Renesas plans to expand the 7542 group as follow:

Memory type

Support for Mask ROM version, Flash memory version, and Emulator MCU .

Memory size

Flash memory size 32 K + 4 K bytes
Mask ROM size 8 K to 16 K bytes
RAM size 384 to 1024 bytes

Package

32P4B 32-pin plastic molded SDIP
32P6U-A 0.8 mm-pitch 32-pin plastic molded LQFP
36P2R-A 0.8 mm-pitch 36-pin plastic molded SSOP
42S1M 42-pin shrink ceramic PIGGY BACK

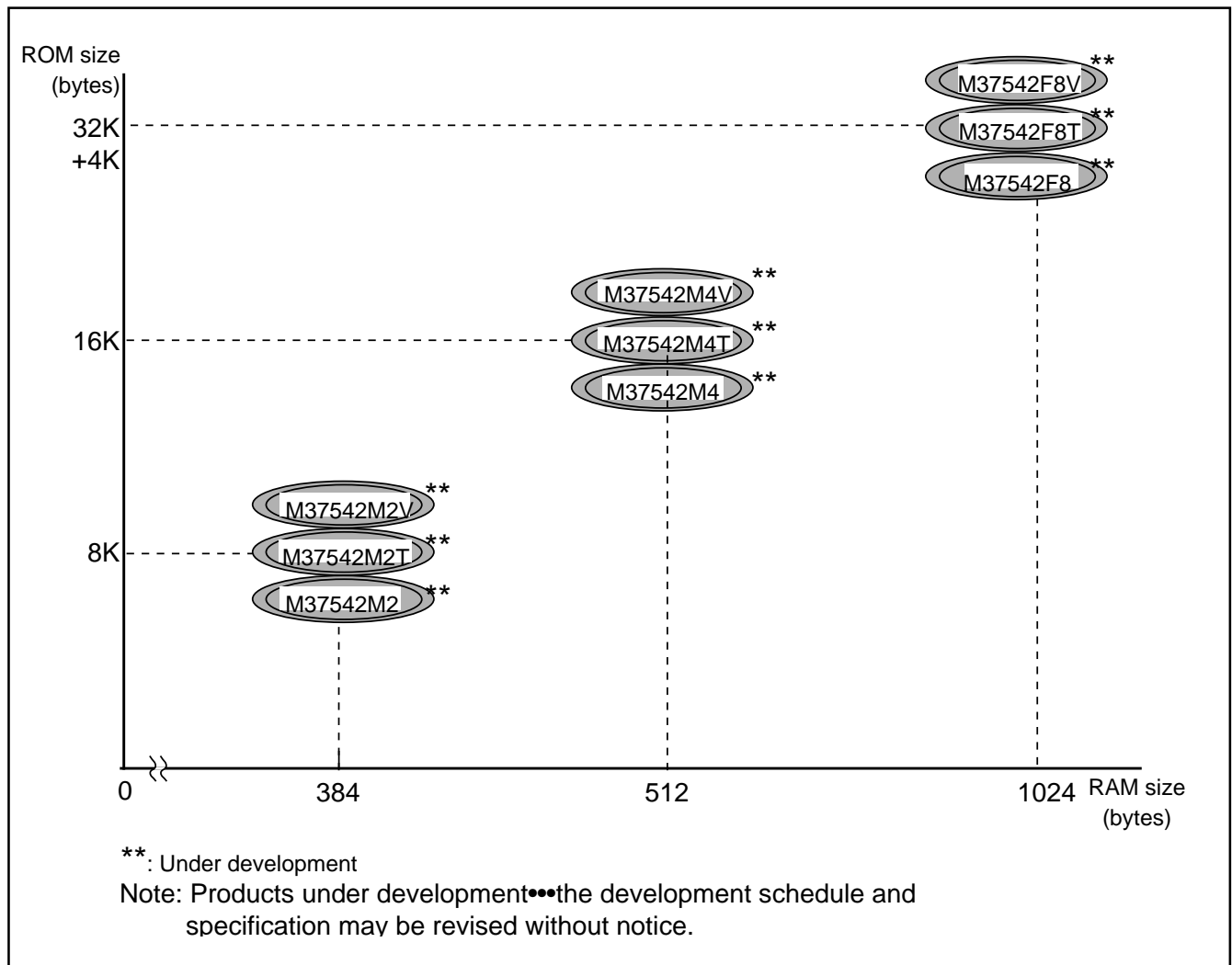


Fig. 8 Memory expansion plan

Currently supported products are listed below.

Table 2 List of supported products

Product	ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M37542M2-XXXSP	8192 (8062)	384	32P4B	Mask ROM version
M37542M2-XXXFP			36P2R-A	Mask ROM version
M37542M2T-XXXFP				Mask ROM version (extended operating temperature version)
M37542M2V-XXXFP				Mask ROM version (extended operating temperature 125 °C version)
M37542M2-XXXGP			32P6U-A	Mask ROM version
M37542M2T-XXXGP				Mask ROM version (extended operating temperature version)
M37542M2V-XXXGP				Mask ROM version (extended operating temperature 125 °C version)
M37542M4-XXXSP	16384 (16254)	512	32P4B	Mask ROM version
M37542M4-XXXFP			36P2R-A	Mask ROM version
M37542M4T-XXXFP				Mask ROM version (extended operating temperature version)
M37542M4V-XXXFP				Mask ROM version (extended operating temperature 125 °C version)
M37542M4-XXXGP			32P6U-A	Mask ROM version
M37542M4T-XXXGP				Mask ROM version (extended operating temperature version)
M37542M4V-XXXGP				Mask ROM version (extended operating temperature 125 °C version)
M37542F8SP	32768 + 4096 (32638)	1024	32P4B	Flash memory version
M37542F8FP			36P2R-A	Flash memory version
M37542F8TFP				Flash memory version (extended operating temperature version)
M37542F8VFP				Flash memory version (extended operating temperature 125 °C version)
M37542F8GP			32P6U-A	Flash memory version
M37542F8TGP				Flash memory version (extended operating temperature version)
M37542F8VGP				Flash memory version (extended operating temperature 125 °C version)
M37542RSS	—————	1024	42S1M	Emulator MCU

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The MCU uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the SERIES 740 <SOFTWARE> USER'S MANUAL for details on each instruction set.

Machine-resident 740 family instructions are as follows:

1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions can be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.

Accumulator (A)

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

Index register X (X), Index register Y (Y)

Both index register X and index register Y are 8-bit registers. In the index addressing modes, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address.

When the T flag in the processor status register is set to "1", the value contained in index register X becomes the address for the second OPERAND.

Stack pointer (S)

The stack pointer is an 8-bit register used during subroutine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines.

The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Selection Bit. If the Stack Page Selection Bit is "0", then the RAM in the zero page is used as the stack area. If the Stack Page Selection Bit is "1", then RAM in page 1 is used as the stack area.

The Stack Page Selection Bit is located in the SFR area in the zero page. Note that the initial value of the Stack Page Selection Bit varies with each microcomputer type. Also some microcomputer types have no Stack Page Selection Bit and the upper eight bits of the stack address are fixed. The operations of pushing register contents onto the stack and popping them from the stack are shown in Fig. 9.

Program counter (PC)

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

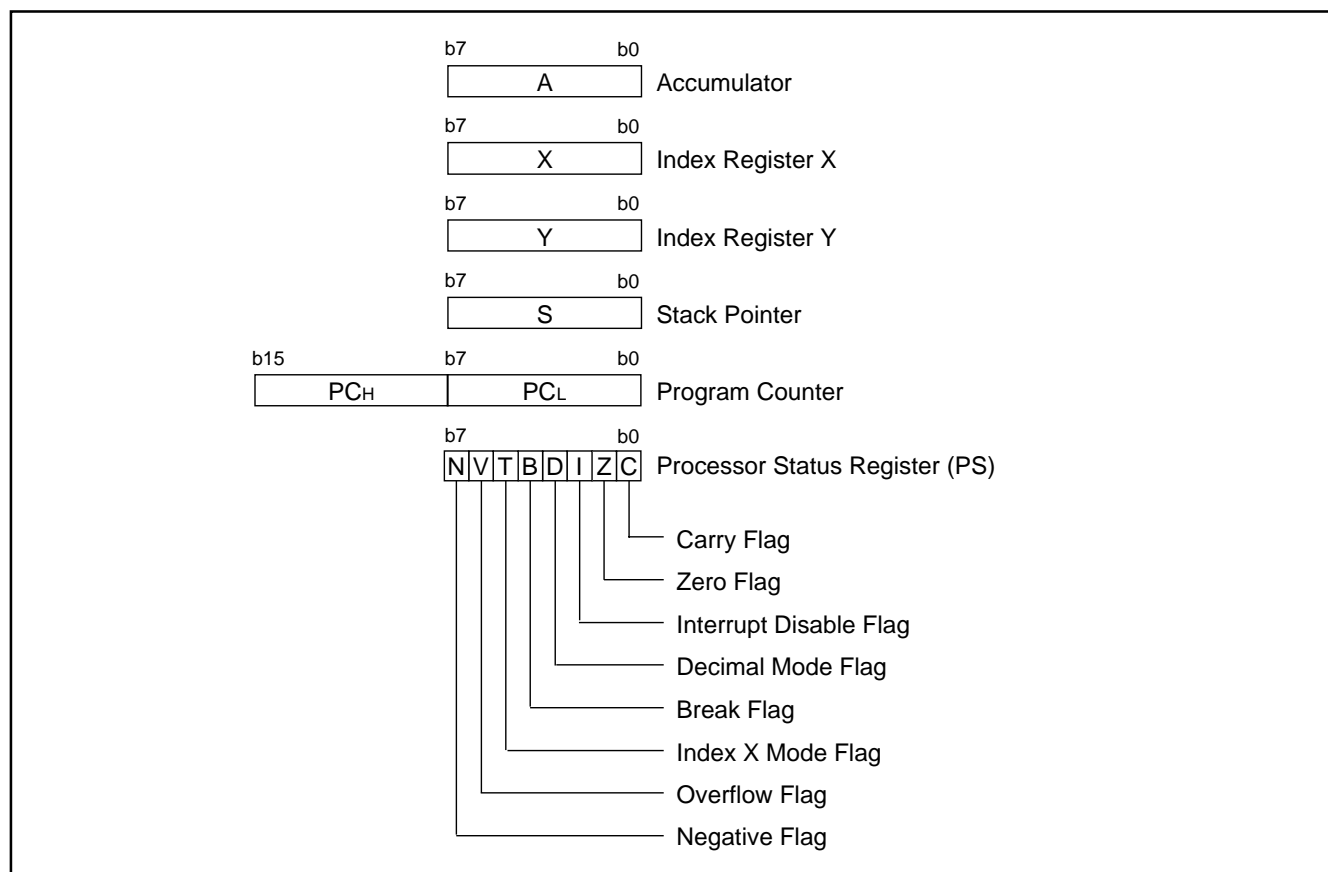


Fig. 9 740 Family CPU register structure

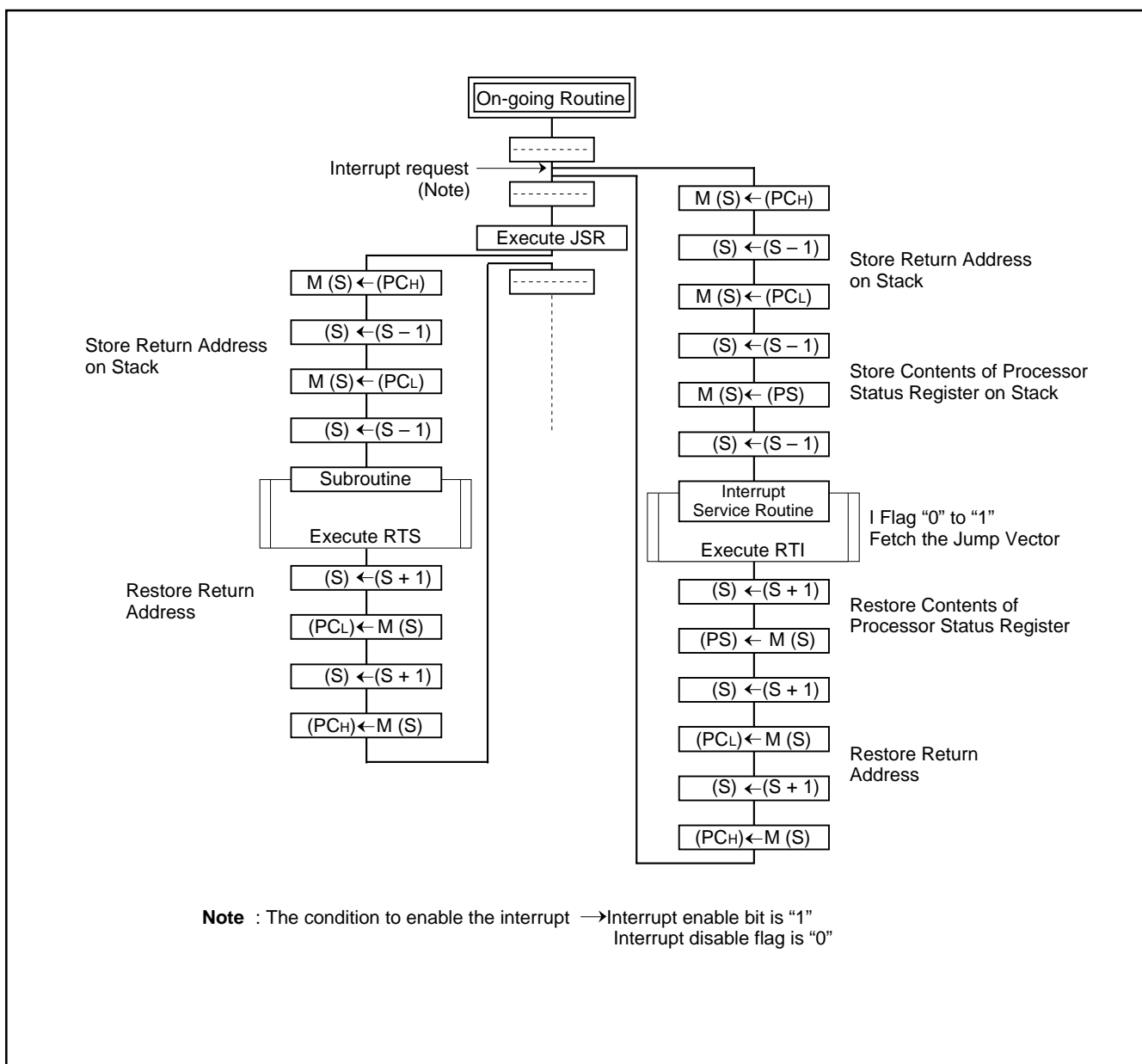


Fig. 10 Register push and pop at interrupt generation and subroutine call

Table 3 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

Processor status register (PS)

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

After reset, the Interrupt disable (I) flag is set to "1", but all other flags are undefined. Since the Index X mode (T) and Decimal mode (D) flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

(1) Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

(2) Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

(3) Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is "1".

When an interrupt occurs, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is serviced.

(4) Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".

Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

(5) Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1". The saved processor status is the only place where the break flag is ever set.

(6) Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory, e.g. the results of an operation between two memory locations is stored in the accumulator. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations, i.e. between memory and memory, memory and I/O, and I/O and I/O. In this case, the result of an arithmetic operation performed on data in memory location 1 and memory location 2 is stored in memory location 1. The address of memory location 1 is specified by index register X, and the address of memory location 2 is specified by normal addressing modes.

(7) Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

(8) Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 4 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU mode register] CPUM

The CPU mode register contains the stack page selection bit, etc..
This register is allocated at address 003B16.

Switching method of CPU mode register

Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.

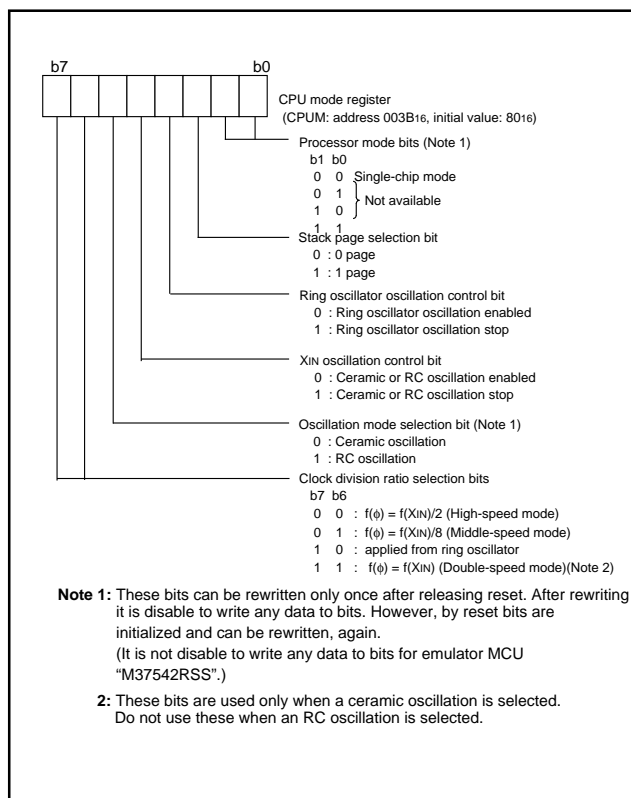


Fig. 11 Structure of CPU mode register

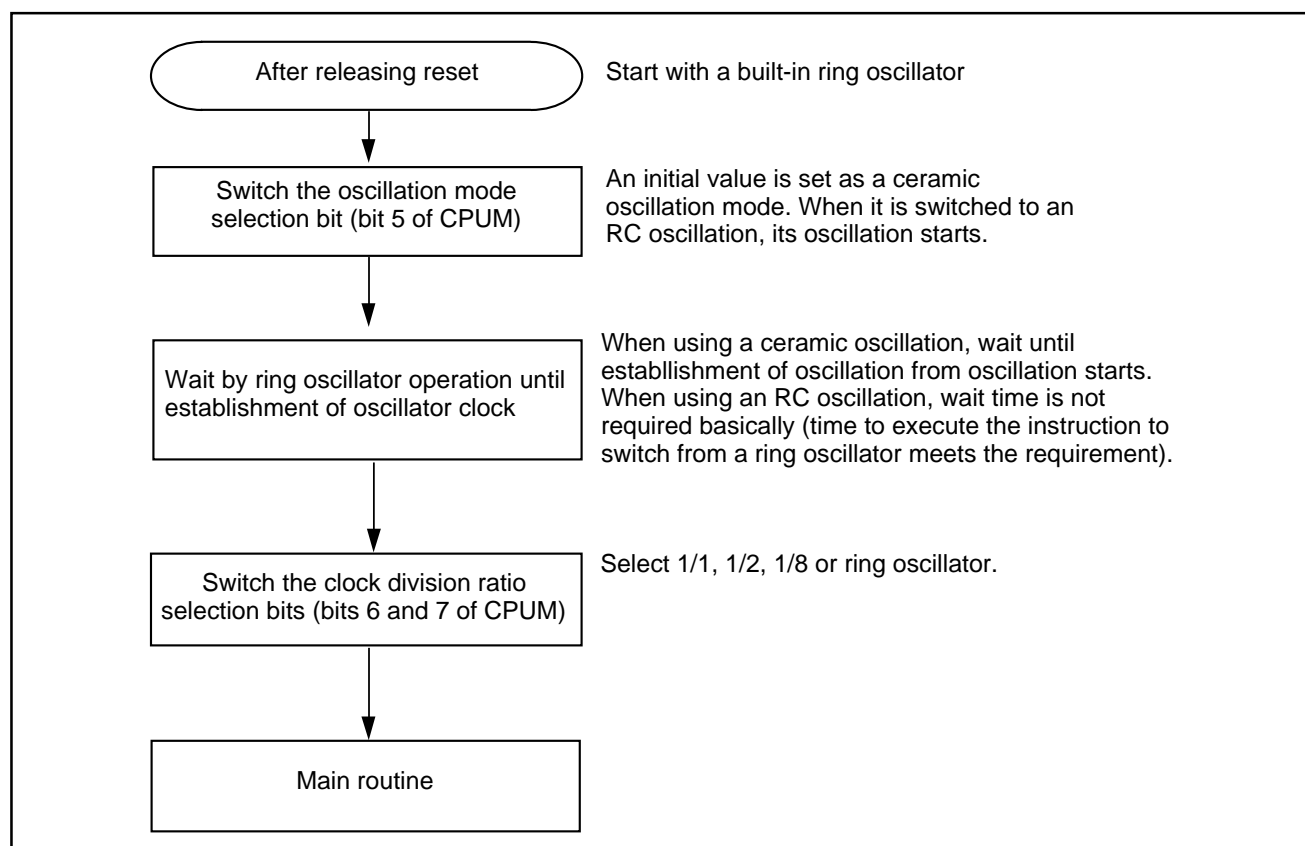


Fig. 12 Switching method of CPU mode register

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

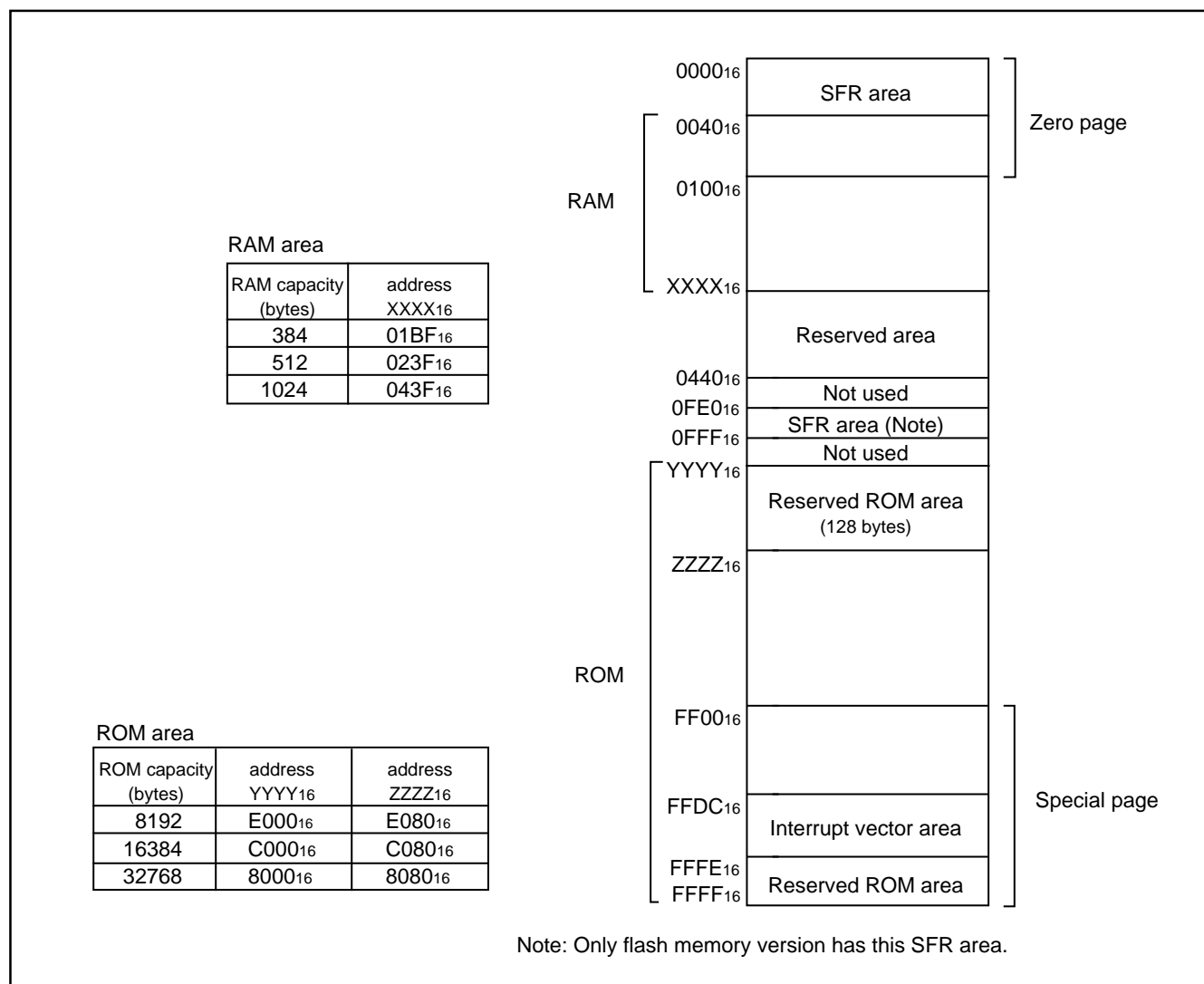


Fig. 13 Memory map diagram

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Capture mode register (CAPM)
0001 ₁₆	Port P0 direction register (P0D)	0021 ₁₆	Compare output mode register (CMOM)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Capture/compare status register (CCSR)
0003 ₁₆	Port P1 direction register (P1D)	0023 ₁₆	Compare interrupt source set register (CISR)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Timer A (low-order) (TAL)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer A (high-order) (TAH)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Timer B (low-order) (TBL)
0007 ₁₆	Port P3 direction register (P3D)	0027 ₁₆	Timer B (high-order) (TBH)
0008 ₁₆	Reserved	0028 ₁₆	Prescaler 1 (PRE1)
0009 ₁₆	Reserved	0029 ₁₆	Timer 1 (T1)
000A ₁₆	Interrupt source set register (INTSET)	002A ₁₆	Timer count source set register (TCSS)
000B ₁₆	Interrupt source discrimination register (INTDIS)	002B ₁₆	Timer X mode register (TXM)
000C ₁₆	Capture register 0 (low-order) (CAP0L)	002C ₁₆	Prescaler X (PREX)
000D ₁₆	Capture register 0 (high-order) (CAP0H)	002D ₁₆	Timer X (TX)
000E ₁₆	Capture register 1 (low-order) (CAP1L)	002E ₁₆	Transmit 2 / Receive 2 buffer register (TB2/RB2)
000F ₁₆	Capture register 1 (high-order) (CAP1H)	002F ₁₆	Serial I/O2 status register (SIO2STS)
0010 ₁₆	Compare register (low-order) (CMPL)	0030 ₁₆	Serial I/O2 control register (SIO2CON)
0011 ₁₆	Compare register (high-order) (CMPH)	0031 ₁₆	UART2 control register (UART2CON)
0012 ₁₆	Capture/compare register R/W pointer (CCRP)	0032 ₁₆	Baud rate generator 2 (BRG2)
0013 ₁₆	Capture software trigger register (CSTR)	0033 ₁₆	Reserved
0014 ₁₆	Compare register re-load register (CMPR)	0034 ₁₆	A-D control register (ADCON)
0015 ₁₆	Port P0P3 drive capacity control register (DCCR)	0035 ₁₆	A-D conversion register (low-order) (ADL)
0016 ₁₆	Pull-up control register (PULL)	0036 ₁₆	A-D conversion register (high-order) (ADH)
0017 ₁₆	Port P1P3 control register (P1P3C)	0037 ₁₆	Ring oscillation division ratio selection register (RODR)
0018 ₁₆	Transmit 1 /Receive 1 buffer register (TB1/RB1)	0038 ₁₆	MISRG
0019 ₁₆	Serial I/O1 status register (SIO1STS)	0039 ₁₆	Watchdog timer control register (WDTCON)
001A ₁₆	Serial I/O1 control register (SIO1CON)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	UART1 control register (UART1CON)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Baud rate generator 1 (BRG1)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	Timer A, B mode register (TABM)	003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆	Capture/compare port register (CCPR)	003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	Timer source selection register (TMSR)	003F ₁₆	Interrupt control register 2 (ICON2)
		0FE0 ₁₆	Flash memory control register 0 (FMCR0) (Note 2)
		0FE1 ₁₆	Flash memory control register 1 (FMCR1) (Note 2)

Notes 1: Do not access to the SFR area including nothing.
2: Only flash memory version has this SFR area.

Fig. 14 Memory map of special function register (SFR)

I/O Ports

[Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output. When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port.

When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.

If a pin set to input is written to, only the port latch is written to and the pin remains floating.

Note: P26/AN6, P27/AN7, P35 and P36 do not exist for the 32-pin version.

Accordingly, the following settings are required;

- Select P33 for the INT1 function.
- Set direction registers of ports P26 and P27 to output.
- Set direction registers of ports P35 and P36 to output.

[Port P0P3 drive capacity control register] DCCR

By setting the Port P0P3 drive capacity control register (address 001516), the drive capacity of the N-channel output transistor for the port P0 and port P3 can be selected.

[Pull-up control register] PULL

By setting the pull-up control register (address 001616), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

[Port P1P3 control register] P1P3C

By setting the port P1P3 control register (address 001716), a CMOS input level or a TTL input level can be selected for ports P10, P12, P13, P36, and P37 by program.

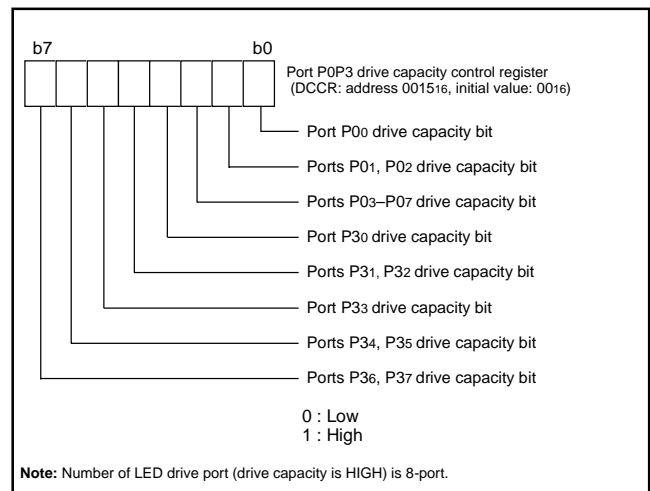


Fig. 15 Structure of port P0P3 drive capacity control register

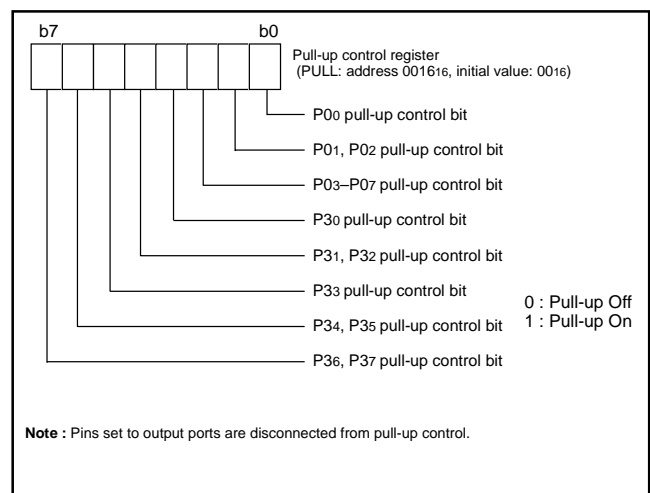


Fig. 16 Structure of pull-up control register

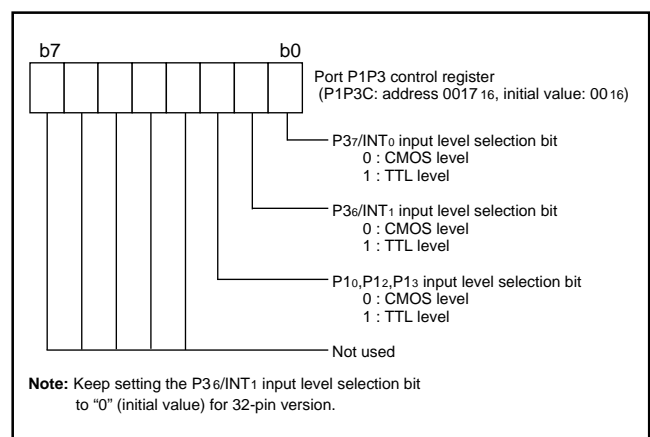


Fig. 17 Structure of port P1P3 control register

Table 5 I/O port function table

Pin	Name	I/O format	Non-port function	SFRs related each pin	Diagram No.
P00(LED00)/CAP0	I/O port P0	•CMOS compatible input level (Note 1) •CMOS 3-state output	• Capture function input • Key input interrupt	Capture/Compare port register Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register	(1)
P01(LED01)/CMP0 P02(LED02)/CMP1			• Compare function output • Key input interrupt	Capture/Compare port register Pull-up control register Port P0P3 drive capacity control register	(2)
P03(LED03)/TXOUT			• Timer X function output • Key input interrupt	Timer X mode register Pull-up control register Port P0P3 drive capacity control register	(3)
P04(LED04)/Rx D2			• Serial I/O2 function input/output • Key input interrupt	Serial I/O2 control register Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register	(4)
P05(LED05)/Tx D2				Serial I/O2 control register Pull-up control register Port P0P3 drive capacity control register	(5)
P06(LED06)/SCLK2				Serial I/O2 control register Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register	(6)
P07(LED07)/SRDY2				Serial I/O2 control register Pull-up control register Port P0P3 drive capacity control register	(7)
P10/RxD1/CAP0	I/O port P1		• Serial I/O1 function input • Capture function input	Serial I/O1 control register Capture/Compare port register Port P1P3 control register	(8)
P11/TxD1			• Serial I/O1 function input/output	Serial I/O1 control register	(9)
P12/SCLK1				Serial I/O1 control register Port P1P3 control register	(10)
P13/SRDY1				Serial I/O1 control register Port P1P3 control register	(11)
P14/CNTR0			• Timer X function input/output • External interrupt input	Timer X mode register	(12)
P20/AN0–P27/AN7	I/O port P2 (Note 2)		• A-D conversion input	A-D control register	(13)
P30(LED10)/CAP1	I/O port P3 (Note 3)		• Capture function input	Capture/Compare port register Pull-up control register Port P0P3 drive capacity control register	(14)
P31(LED11)/CMP2 P32(LED12)/CMP3			• Compare function output	Capture/Compare port register Pull-up control register Port P0P3 drive capacity control register	(15)
P33(LED13)/INT1			• External interrupt input	Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register	(16)
P34(LED14) P35(LED15)				Pull-up control register Port P0P3 drive capacity control register	(17)
P36(LED16)/INT1 P37(LED17)/INT0			• External interrupt input	Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register Port P1P3 control register	(18) (19)

Notes 1: Ports P10, P12, P13, P36, and P37 are CMOS/TTL level.**2:** P26/AN6 and P27/AN7 do not exist for the 32-pin version.**3:** P35 and P36/INT1 do not exist for the 32-pin version.

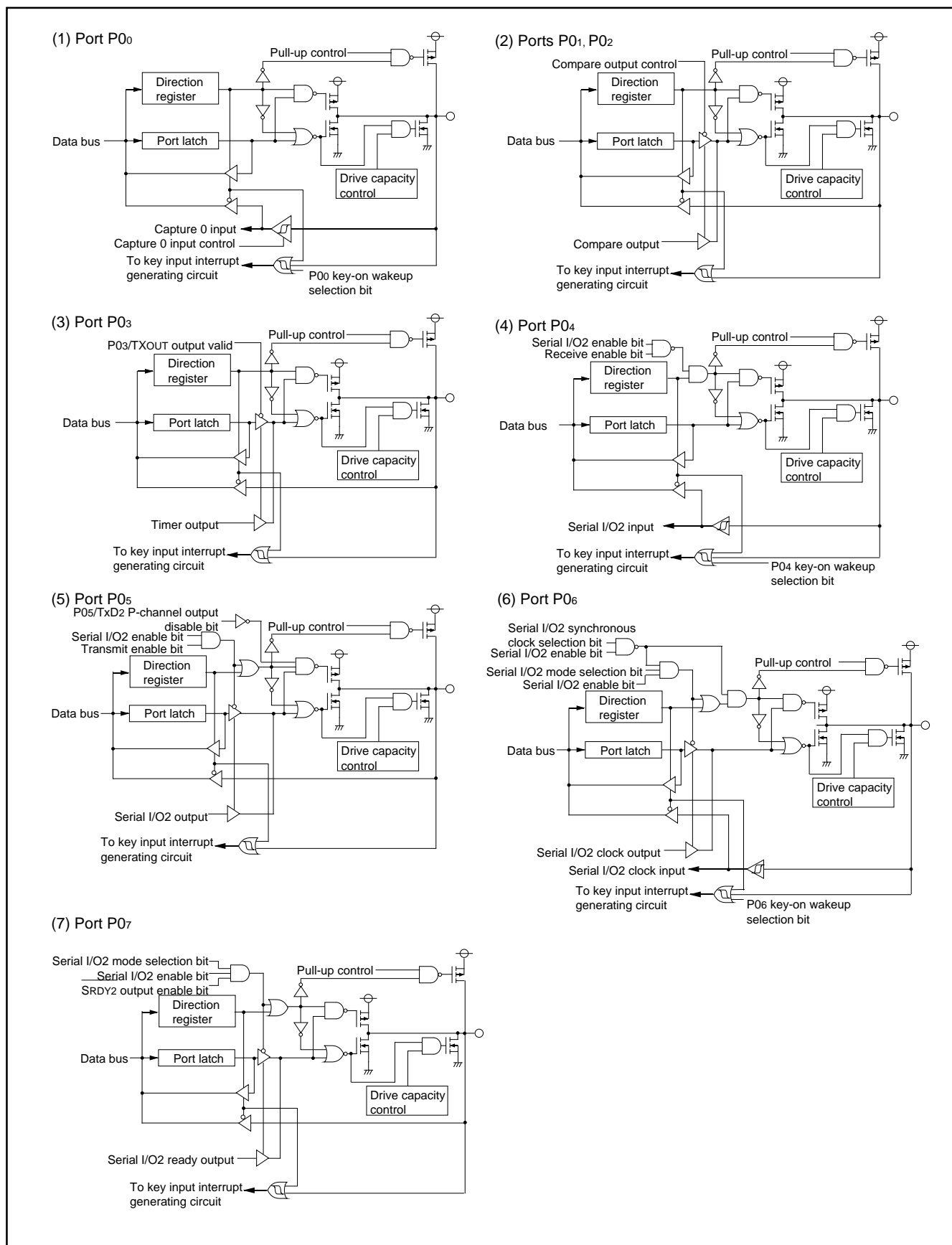
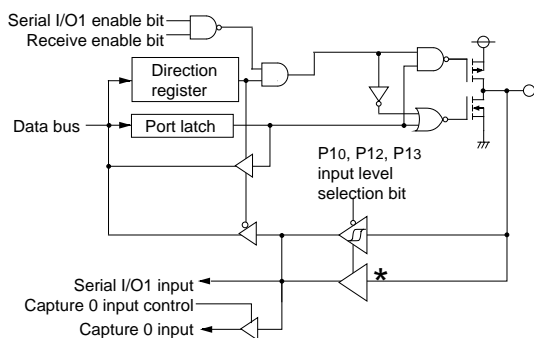
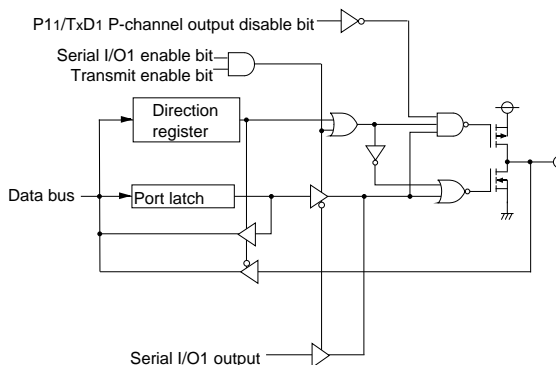


Fig. 18 Block diagram of ports (1)

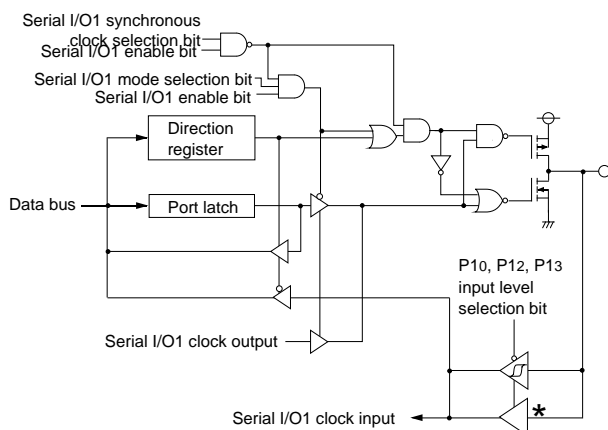
(8) Port P10



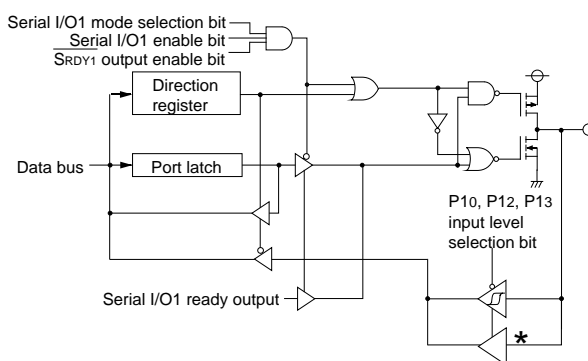
(9) Port P11



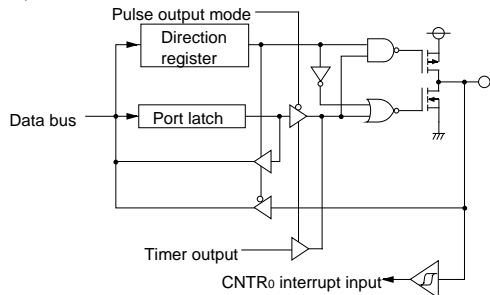
(10) Port P12



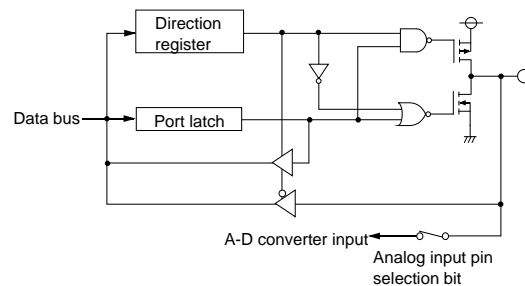
(11) Port P13



(12) Port P14

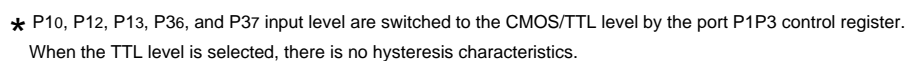


(13) Ports P20–P27



* P10, P12, P13, P36, and P37 input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 19 Block diagram of ports (2)



Interrupts

Interrupts occur by 18 different sources : 6 external sources, 11 internal sources and 1 software source.

Interrupt control

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit, and they are controlled by the interrupt disable flag. When the interrupt enable bit and the interrupt request bit are set to "1" and the interrupt disable flag is set to "0", an interrupt is accepted.

The interrupt request bit can be cleared by program but not be set.

The interrupt enable bit can be set and cleared by program.

The reset and BRK instruction interrupt can never be disabled with any flag or bit. All interrupts except these are disabled when the interrupt disable flag is set.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. Concurrently with the push operation, the interrupt destination address is read from the vector table into the program counter.

[Interrupt source set register] INTSET

When two interrupt sources are assigned to the same interrupt vector, the valid/invalid of each interrupt is set by this register.

When both two interrupt sources are set to be valid, which interrupt request occurs is confirmed by the next interrupt source discrimination register.

[Interrupt source discrimination register] INTDIS

When two interrupt sources are assigned to the same interrupt vector, which interrupt source occurs is confirmed by this register. If an interrupt request of a key-on wakeup, UART1 bus collision detection, A-D conversion or timer 1 occurs, an interrupt discrimination bit is set to "1" regardless of valid/invalid state by the interrupt source set register.

However, when the interrupt valid bit of an interrupt source set register is "0" (invalid), the interrupt request bit of an interrupt control register is not set to "1."

Moreover, since an interrupt discrimination bit is not automatically cleared to "0" by interrupt, please clear it by program.

An interrupt discrimination bit can be cleared to "0" by program but not be set to "1."

[Interrupt edge selection register] INTEDGE

The valid edge of external interrupt INT0 and INT1 can be selected by the interrupt edge selection bit, respectively.

For the external interrupt INT1, the external input pin P33/INT1 or P36/INT1 can be selected by the INT1 input port selection bit.

However, since there is no P36/INT1 pin in the 32-pin version, select P33/INT1 pin. By the key-on wakeup selection bit, enable/disable of a key-on wakeup of P00, P04, and P06 pins can be selected, respectively.

■ Notes on use

(1) When setting the followings, the interrupt request bit may be set to "1".

•When switching external interrupt active edge

Related register:

Interrupt edge selection register (address 003A16)

Timer X mode register (address 002B16)

Capture mode register (address 002016)

When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

- ① Set the corresponding interrupt enable bit to "0" (disabled).
- ② Set the interrupt edge select bit (active edge switch bit, trigger mode bit).
- ③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- ④ Set the corresponding interrupt enable bit to "1" (enabled).

(2) Use a LDM instruction to clear an interrupt discrimination bit.

LDM #0n, \$0Bn

Set the following values to "n"

"0": an interrupt discrimination bit to clear

"1": other interrupt discrimination bits

Ex.) When a key-on wakeup interrupt discrimination bit is cleared;

LDM #00001110B and \$0B.

Table 6 Interrupt vector address and priority

Interrupt source	Priority	Vector addresses (Note 1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset input	Non-maskable
Serial I/O1 receive	2	FFFB ₁₆	FFFA ₁₆	At completion of serial I/O1 data receive	Valid only when serial I/O1 is selected
Serial I/O1 transmit	3	FFF9 ₁₆	FFF8 ₁₆	At completion of serial I/O1 transmit shift or when transmit buffer is empty	Valid only when serial I/O1 is selected
Serial I/O2 receive	4	FFF7 ₁₆	FFF6 ₁₆	At completion of serial I/O2 data receive	Valid only when serial I/O2 is selected
Serial I/O2 transmit	5	FFF5 ₁₆	FFF4 ₁₆	At completion of serial I/O2 transmit shift or when transmit buffer is empty	Valid only when serial I/O2 is selected
INT ₀	6	FFF3 ₁₆	FFF2 ₁₆	At detection of either rising or falling edge of INT ₀ input	External interrupt (active edge selectable)
INT ₁	7	FFF1 ₁₆	FFF0 ₁₆	At detection of either rising or falling edge of INT ₁ input	External interrupt (active edge selectable)
Key-on wake-up/ UART1 bus collision detection (Note 3)	8	FFEF ₁₆	FFEE ₁₆	At falling of conjunction of input logical level for port P0 (at input) _____ At detection of UART1 bus collision detection	External interrupt (valid at falling, when key-on wakeup interrupt is enabled) _____ When UART1 bus collision detection interrupt is enabled.
CNTR ₀	9	FFED ₁₆	FFEC ₁₆	At detection of either rising or falling edge of CNTR ₀ input	External interrupt (active edge selectable)
Capture 0	10	FFEB ₁₆	FFEA ₁₆	At detection of either rising or falling edge of Capture 0 input	External interrupt (active edge selectable)
Capture 1	11	FFE9 ₁₆	FFE8 ₁₆	At detection of either rising or falling edge of Capture 1 input	External interrupt (active edge selectable)
Compare	12	FFE7 ₁₆	FFE6 ₁₆	At compare matched	Compare interrupt source is selected.
Timer X	13	FFE5 ₁₆	FFE4 ₁₆	At timer X underflow	
Timer A	14	FFE3 ₁₆	FFE2 ₁₆	At timer A underflow	
Timer B	15	FFE1 ₁₆	FFE0 ₁₆	At timer B underflow	
A-D conversion/ Timer 1 (Note 4)	16	FFDF ₁₆	FFDE ₁₆	At completion of A-D conversion _____ At timer 1 underflow _____	When A-D conversion interrupt is enabled. _____ STP release timer underflow _____ (When Timer 1 interrupt is enabled)
BRK instruction	17	FFDD ₁₆	FFDC ₁₆	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addresses contain internal jump destination addresses.**2:** Reset function in the same way as an interrupt with the highest priority.**3:** Key-on wakeup interrupt and UART1 bus collision detection interrupt can be enabled by setting of interrupt source set register. The occurrence of these interrupts are discriminated by interrupt source discrimination register.**4:** A-D conversion interrupt and Timer 1 interrupt can be enabled by setting of interrupt source set register. The occurrence of these interrupts are discriminated by interrupt source discrimination register.

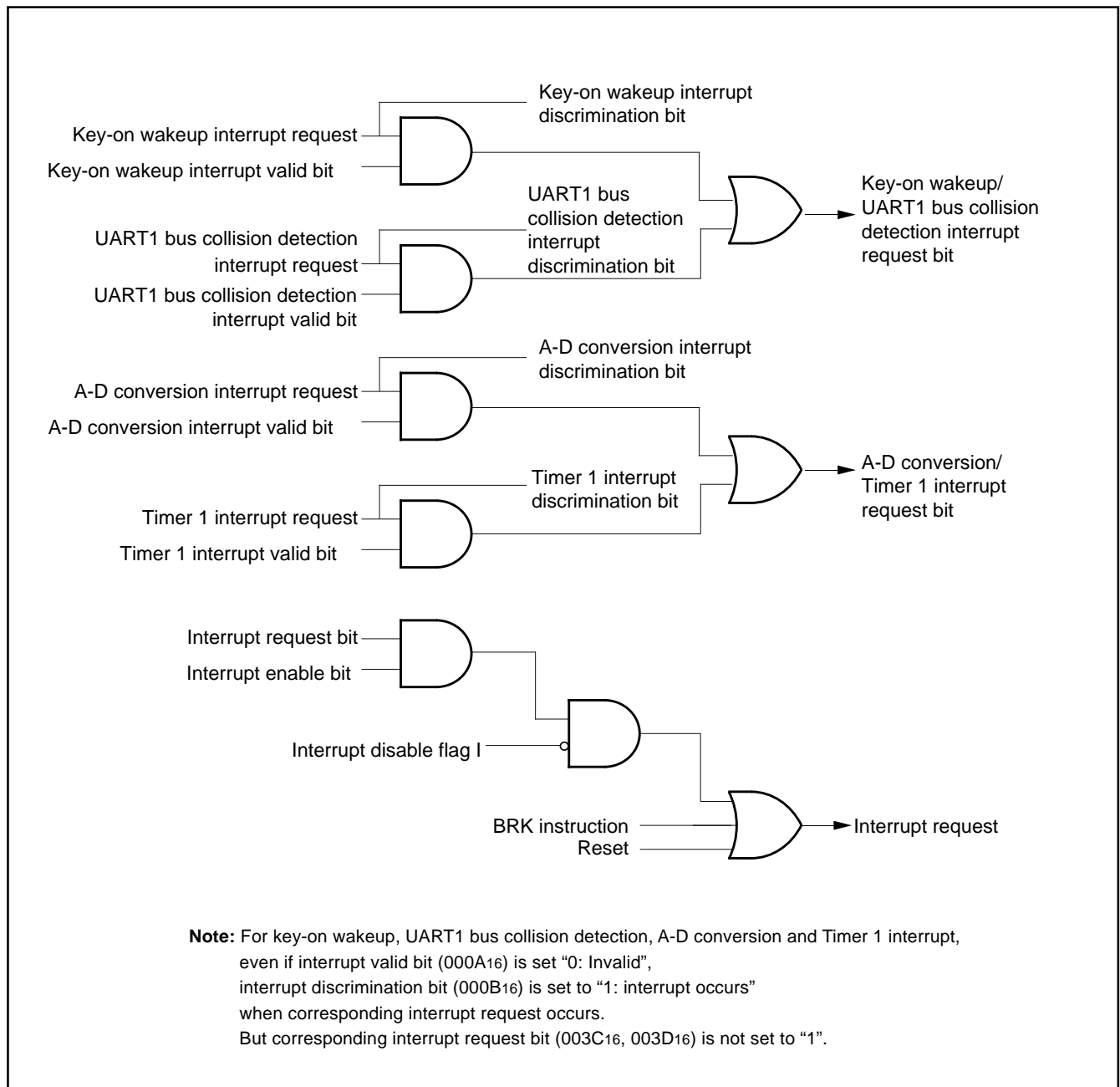


Fig. 21 Interrupt control

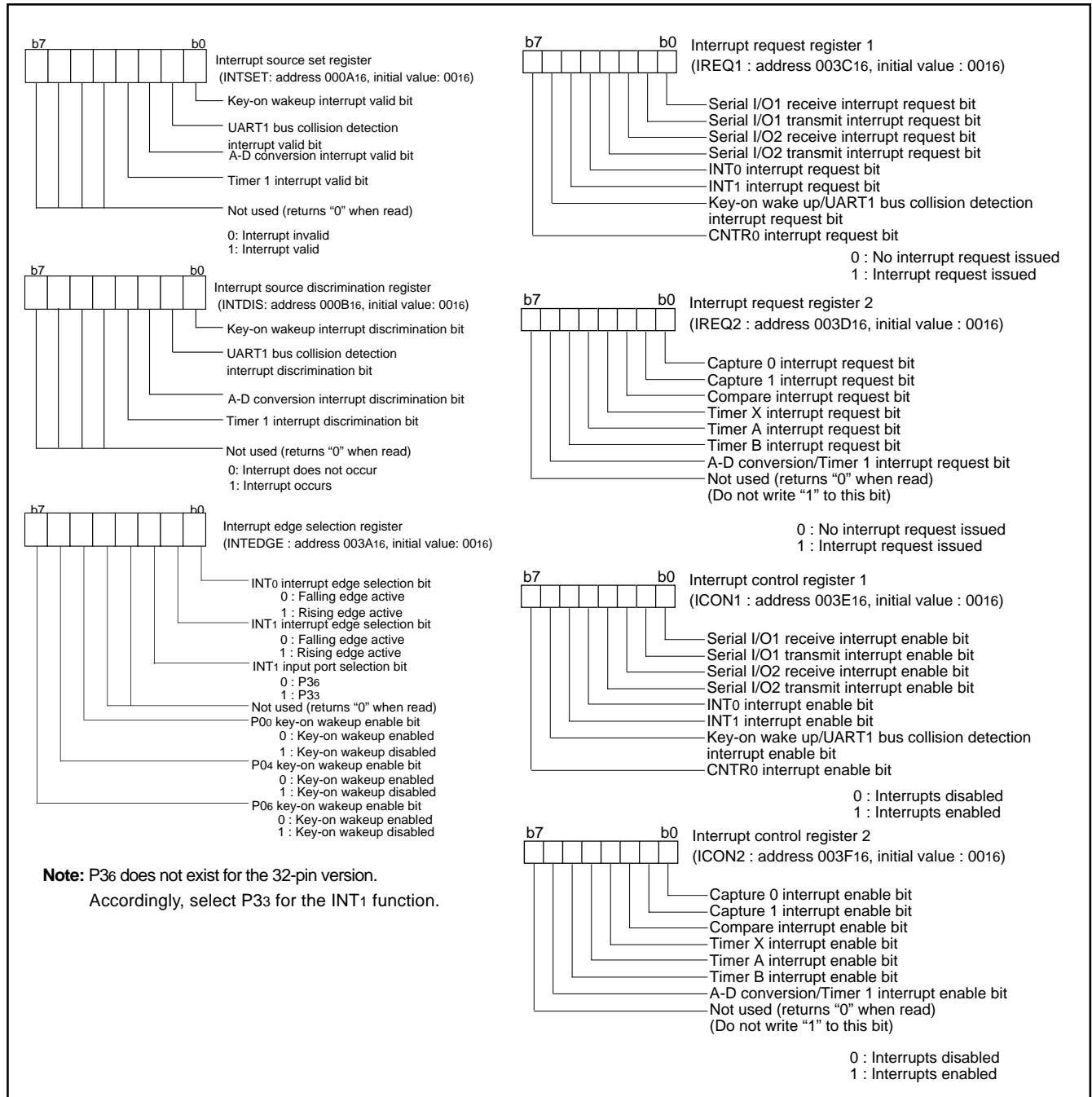


Fig. 22 Structure of Interrupt-related registers

In other words, it is generated when the AND of input level goes from “1” to “0”. An example of using a key input interrupt is shown in Figure 21, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports P00 to P03 as input ports.

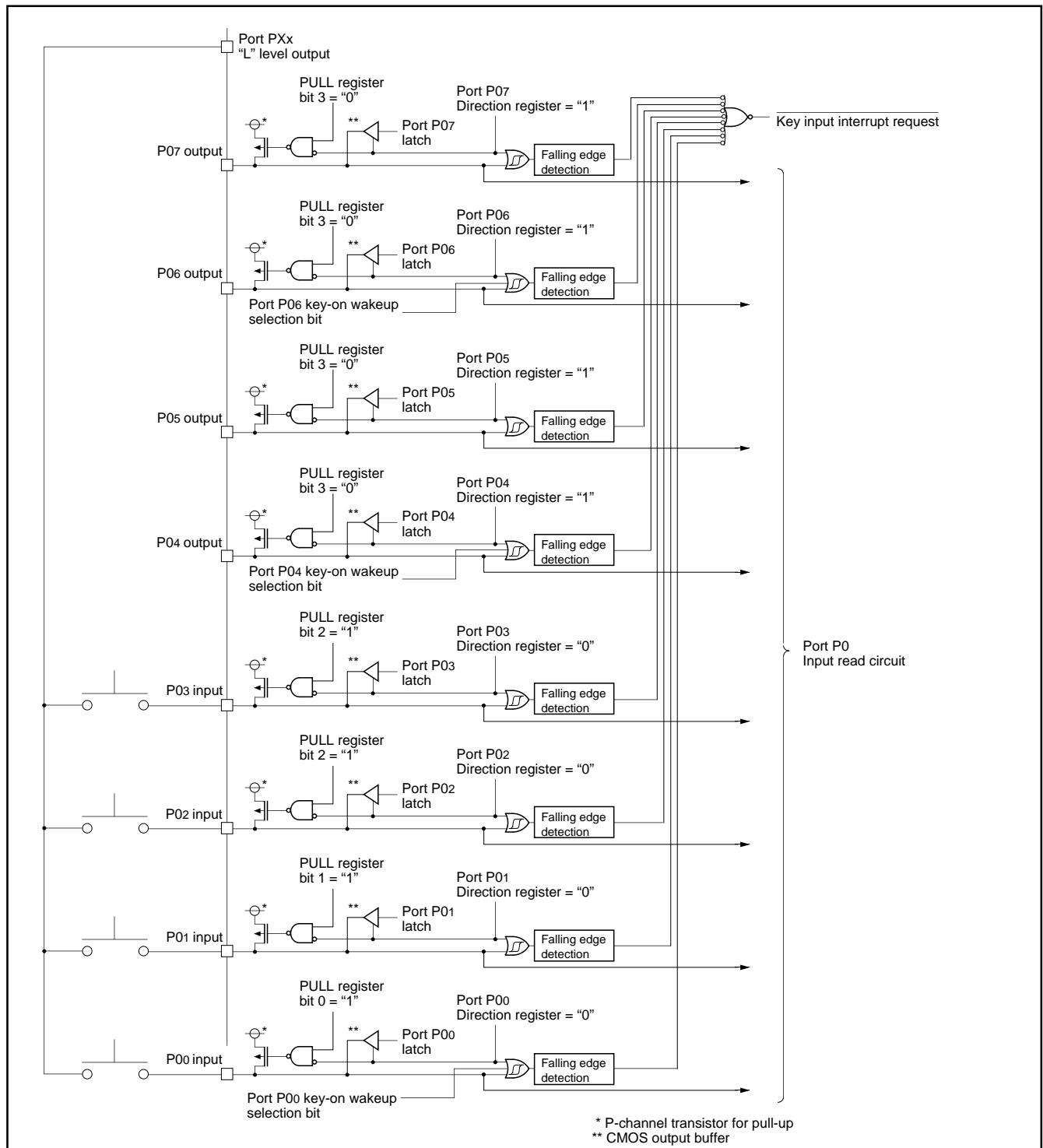


Fig. 23 Connection example when using key input interrupt and port P0 block diagram

Timers

The 7542 Group has 4 timers: timer 1, timer X, timer A and timer B.

The division ratio of every timer and prescaler is $1/(n+1)$ provided that the value of the timer latch or prescaler is n .

All the timers are down count timers. When a timer reaches "0", an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to "1".

• Frequency divider for timer

According to the clock division selection bits (b7 and b6) of CPU mode register (003B16), the count source of frequency divider is set as follows;

b7b6 = "00"(high-speed), "01"(middle-speed), "11"(double-speed): XIN
b7b6 = "10"(Ring oscillator): Ring oscillator

●Timer 1

Timer 1 is an 8-bit timer and counts the prescaler output.

When Timer 1 underflows, the timer 1 interrupt request bit is set to "1".

Prescaler 1 is an 8-bit prescaler and counts the signal which is the oscillation frequency divided by 16.

Prescaler 1 and Timer 1 have the prescaler 1 latch and the timer 1 latch to retain the reload value, respectively. The value of prescaler 1 latch is set to Prescaler 1 when Prescaler 1 underflows. The value of timer 1 latch is set to Timer 1 when Timer 1 underflows.

When writing to Prescaler 1 (PRE1) is executed, the value is written to both the prescaler 1 latch and Prescaler 1.

When writing to Timer 1 (T1) is executed, the value is written to both the timer 1 latch and Timer 1.

When reading from Prescaler 1 (PRE1) and Timer 1 (T1) is executed, each count value is read out.

Timer 1 always operates in the timer mode.

Prescaler 1 counts the signal which is the oscillation frequency divided by 16. Each time the count clock is input, the contents of Prescaler 1 is decremented by 1. When the contents of Prescaler 1 reach "0016", an underflow occurs at the next count clock, and the prescaler 1 latch is reloaded into Prescaler 1 and count continues. The division ratio of Prescaler 1 is $1/(n+1)$ provided that the value of Prescaler 1 is n .

The contents of Timer 1 is decremented by 1 each time the underflow signal of Prescaler 1 is input. When the contents of Timer 1 reach "0016", an underflow occurs at the next count clock, and the timer 1 latch is reloaded into Timer 1 and count continues. The division ratio of Timer 1 is $1/(m+1)$ provided that the value of Timer 1 is m . Accordingly, the division ratio of Prescaler 1 and Timer 1 is $1/((n+1) \times (m+1))$ provided that the value of Prescaler 1 is n and the value of Timer 1 is m .

Timer 1 cannot stop counting by software.

●Timer X

Timer X is an 8-bit timer and counts the prescaler X output.

When Timer X underflows, the timer X interrupt request bit is set to "1".

Prescaler X is an 8-bit prescaler and counts the signal selected by the timer X count source selection bit.

Prescaler X and Timer X have the prescaler X latch and the timer X latch to retain the reload value, respectively. The value of prescaler X latch is set to Prescaler X when Prescaler X underflows. The value of timer X latch is set to Timer X when Timer X underflows.

When writing to Prescaler X (PREX) is executed, the value is written to both the prescaler X latch and Prescaler X.

When writing to Timer X (TX) is executed, the value is written to both the timer X latch and Timer X.

When reading from Prescaler X (PREX) and Timer X (TX) is executed, each count value is read out.

Timer X can be selected in one of 4 operating modes by setting the timer X operating mode bits of the timer X mode register.

(1) Timer mode

Prescaler X counts the count source selected by the timer X count source selection bits. Each time the count clock is input, the contents of Prescaler X is decremented by 1. When the contents of Prescaler X reach "0016", an underflow occurs at the next count clock, and the prescaler X latch is reloaded into Prescaler X and count continues. The division ratio of Prescaler X is $1/(n+1)$ provided that the value of Prescaler X is n .

The contents of Timer X is decremented by 1 each time the underflow signal of Prescaler X is input. When the contents of Timer X reach "0016", an underflow occurs at the next count clock, and the timer X latch is reloaded into Timer X and count continues. The division ratio of Timer X is $1/(m+1)$ provided that the value of Timer X is m . Accordingly, the division ratio of Prescaler X and Timer X is $1/((n+1) \times (m+1))$ provided that the value of Prescaler X is n and the value of Timer X is m .

(2) Pulse output mode

In the pulse output mode, the waveform whose polarity is inverted each time timer X underflows is output from the CNTR0 pin.

The output level of CNTR0 pin can be selected by the CNTR0 active edge switch bit. When the CNTR0 active edge switch bit is "0", the output of CNTR0 pin is started at "H" level. When this bit is "1", the output is started at "L" level.

Also, the inverted waveform of pulse output from CNTR0 pin can be output from TXOUT pin by setting "1" to the P03/TXOUT output valid bit.

When using a timer in this mode, set the port P14 and P03 direction registers to output mode.

(3) Event counter mode

The timer A counts signals input from the P14/CNTR0 pin.

Except for this, the operation in event counter mode is the same as in timer mode.

The active edge of CNTR0 pin input signal can be selected from rising or falling by the CNTR0 active edge switch bit.

(4) Pulse width measurement mode

In the pulse width measurement mode, the pulse width of the signal input to P14/CNTR0 pin is measured.

The operation of Timer X can be controlled by the level of the signal input from the CNTR0 pin.

When the CNTR0 active edge switch bit is "0", the signal selected by the timer X count source selection bit is counted while the input signal level of CNTR0 pin is "H". The count is stopped while the pin is "L". Also, when the CNTR0 active edge switch bit is "1", the signal selected by the timer X count source selection bit is counted while the input signal level of CNTR0 pin is "L". The count is stopped while the pin is "H".

Timer X can stop counting by setting "1" to the timer X count stop bit in any mode.

Also, when Timer X underflows, the timer X interrupt request bit is set to "1".

Note on Timer X is described below;

■ Note on Timer X**(1) CNTR0 interrupt active edge selection-1**

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

When this bit is "0", the CNTR0 interrupt request bit is set to "1" at the falling edge of CNTR0 pin input signal. When this bit is "1", the CNTR0 interrupt request bit is set to "1" at the rising edge of CNTR0 pin input signal.

(2) CNTR0 interrupt active edge selection-2

According to the setting value of CNTR0 active edge switch bit, the interrupt request bit may be set to "1".

When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

- ① Set the corresponding interrupt enable bit to "0" (disabled).
- ② Set the active edge switch bit.
- ③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- ④ Set the corresponding interrupt enable bit to "1" (enabled).

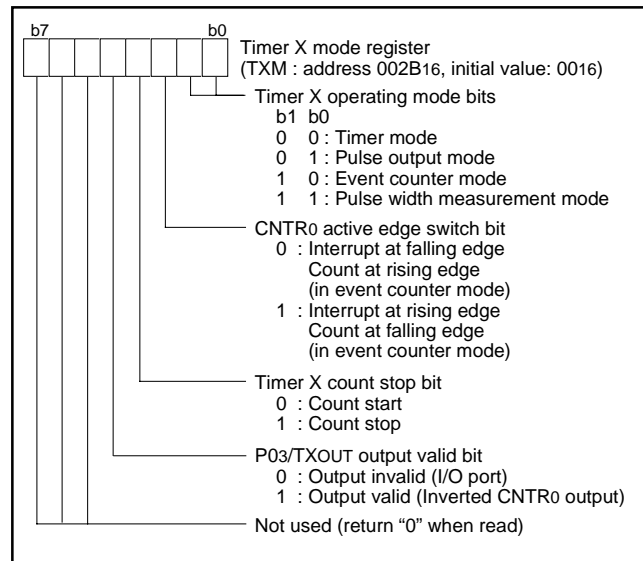


Fig. 24 Structure of timer X mode register

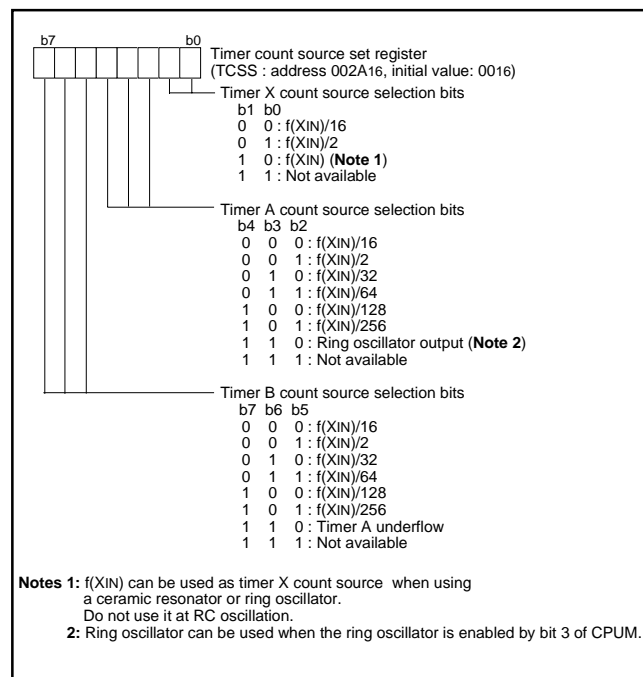


Fig. 25 Timer count source set register

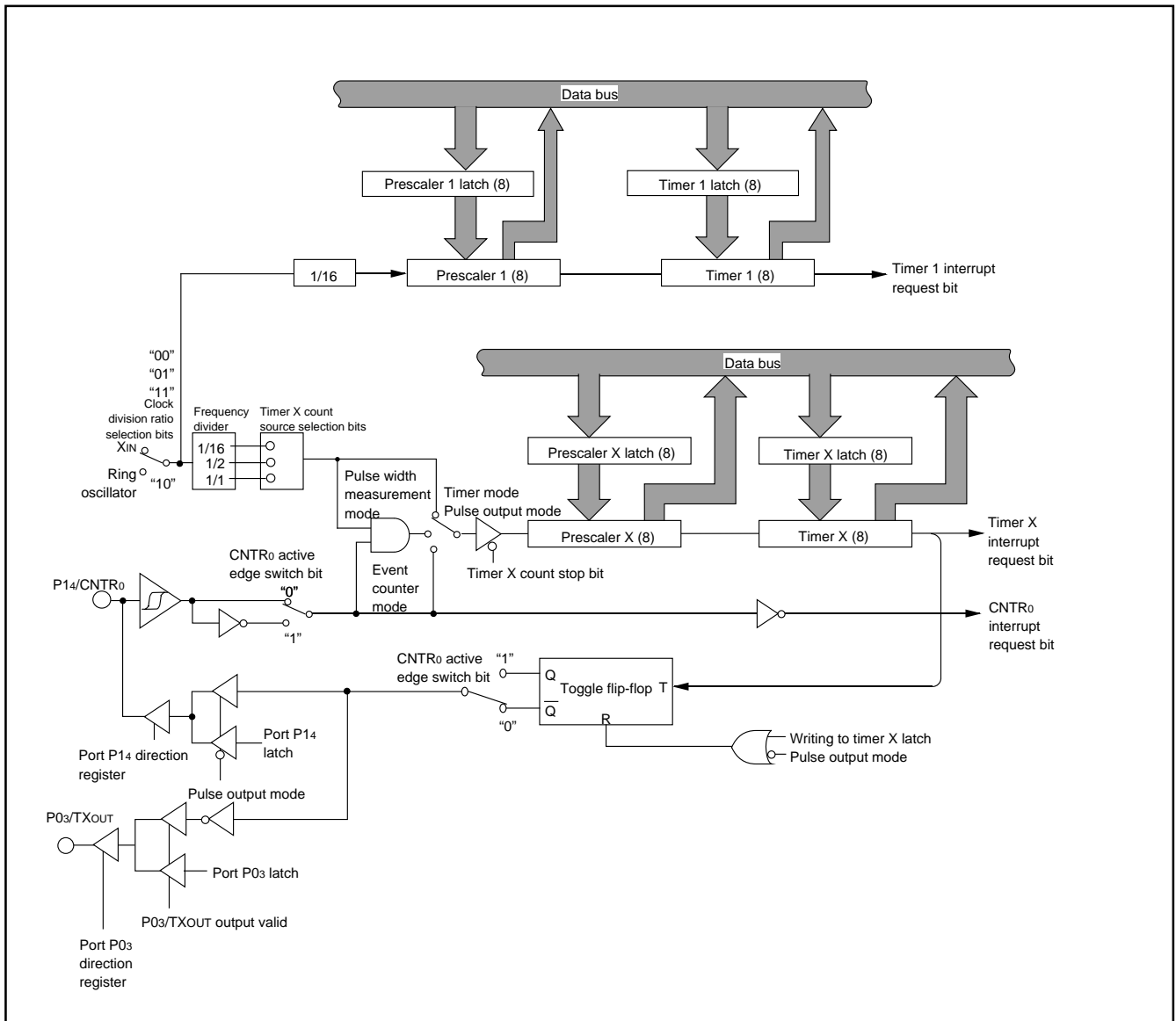


Fig. 26 Block diagram of timer 1 and timer X

●Timer A,B

Timer A and Timer B are 16-bit timers and counts the signal which is the oscillation frequency selected by setting of the timer count source set register (TCSS). Timer A and Timer B have the same function except of the count source clock selection.

The count source clock of Timer A is selected from among 1/2, 1/16, 1/32, 1/64, 1/128, 1/256 of f(XIN) clock and ring oscillator clock.

The count source clock of Timer B is selected from among 1/2, 1/16, 1/32, 1/64, 1/128, 1/256 of f(XIN) clock and Timer A underflow.

Timer A (B) consists of the low-order of Timer A: TAL (Timer B: TBL) and the high-order of Timer A: TAH (Timer B: TBH). Timer A (B) is decremented by 1 when each time of the count clock is input. When the contents of Timer A (B) reach "0000₁₆", an underflow occurs at the next count clock, and the timer latch is reloaded into timer. When Timer A (B) underflows, the Timer A (B) interrupt request bit is set to "1".

Timer A (B) has the Timer A (B) latch to retain the load value. The value of timer A (B) latch is set to Timer A (B) at the timing of Timer A (B) underflow. The division ratio of Timer A (B) is 1/(n+1) provided that the value of Timer A (B) is n.

When writing to both the low-order of Timer A (B) and the high order of Timer A (B) is executed, writing to "latch only" or "latch and timer" can be selected by the setting value of the timer A (B) write control bit.

When reading from Timer A (B) register is executed, the count value of Timer A (B) is read out.

Be sure to write to/read out the low-order of Timer A (B) and the high-order of Timer A (B) in the following order;

- Read

Read the high-order of Timer A (B) first, and the low-order of Timer A (B) next and be sure to read both high-order and low-order.

- Write

Write to the low-order of Timer A (B) first, and the high-order of Timer A (B) next and be sure to write both low-order and high order.

Timer A and Timer B can be used for the timing timer of Input capture and Output compare function.

■ Notes on Timer A, B

(1) Setting of timer value

When "1: Write to only latch" is set to the timer A (B) write control bit, written data to timer register is set to only latch even if timer is stopped. Accordingly, in order to set the initial value for timer when it is stopped, set "0: Write to latch and timer simultaneously" to timer A (B) write control bit.

(2) Read/write of timer A

Stop timer A to read/write its data when the system is in the following state;

- CPU operation clock source: XIN oscillation
- Timer A count source: Ring oscillator output

(3) Read/write of timer B

Stop timer B to read/write its data when the system is in the following state;

- CPU operation clock source: XIN oscillation
- Timer B count source: Timer A underflow
- Timer A count source: Ring oscillator output

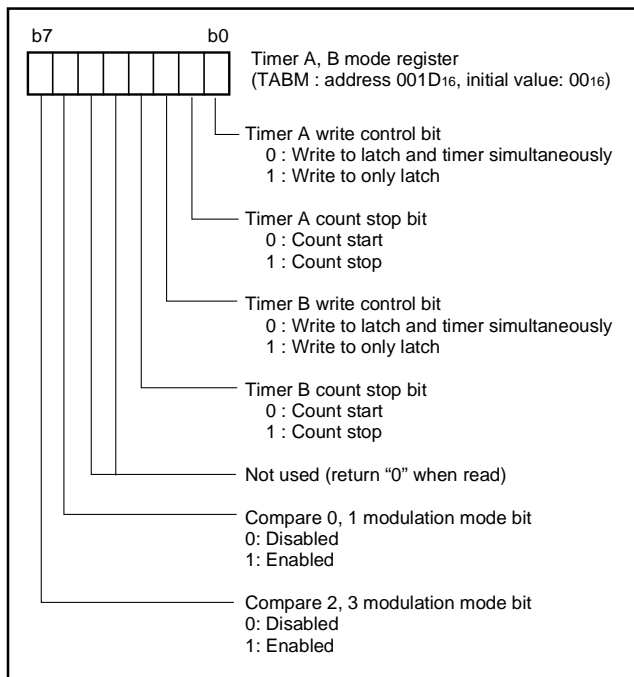


Fig. 27 Structure of timer A, B mode register

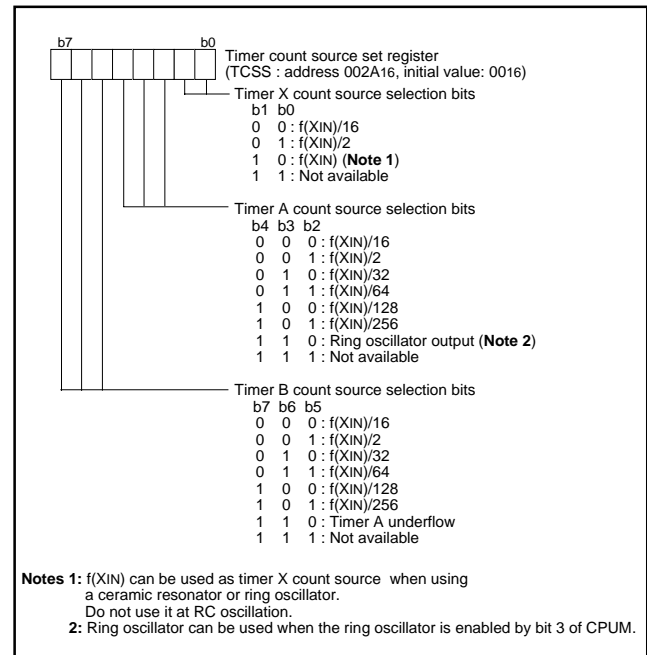


Fig. 28 Timer count source set register

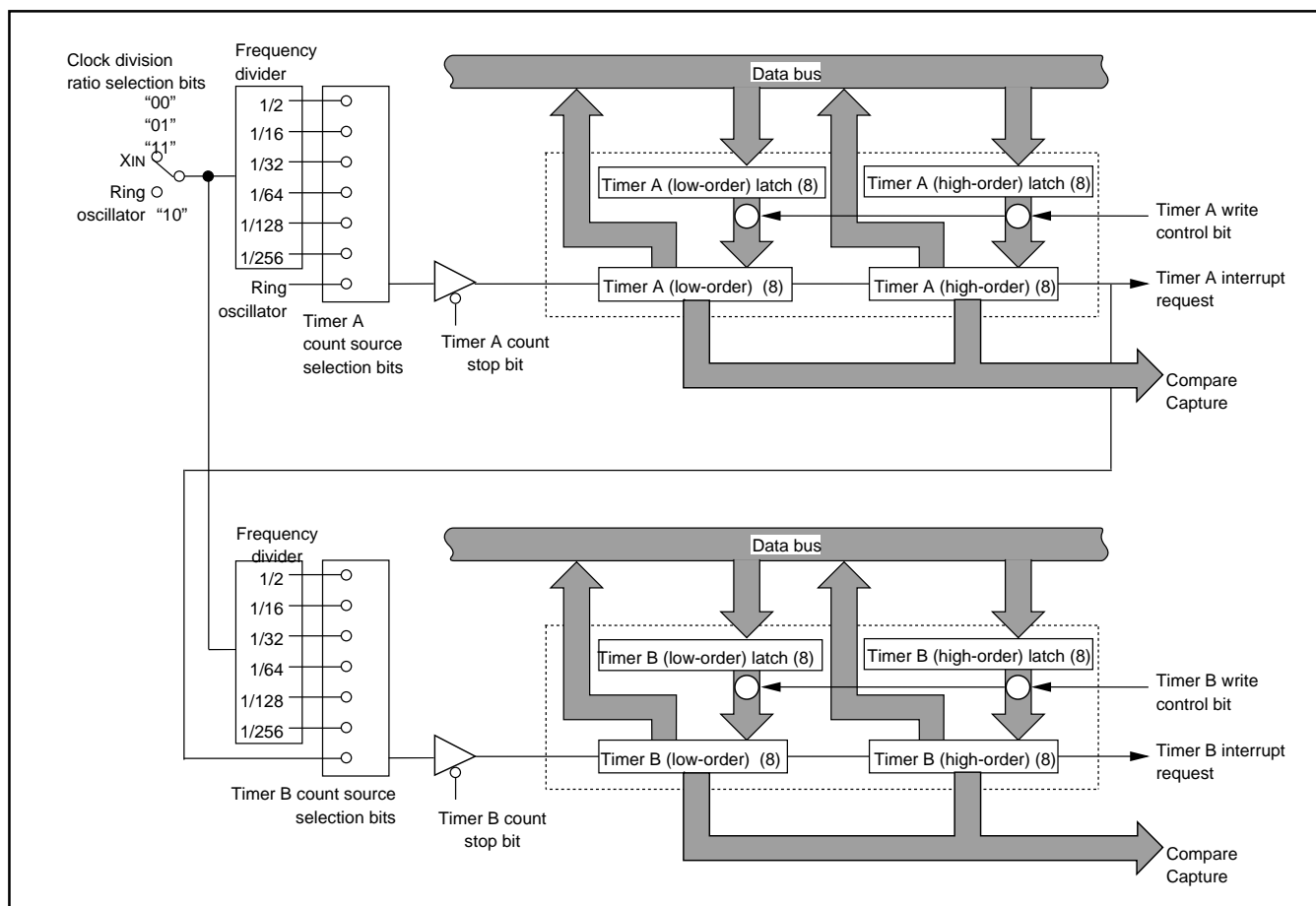


Fig. 29 Block diagram of timer A and timer B

Output compare

7542 group has 4-output compare channels. Each channel (0 to 3) has the same function and can be used to output waveform by using count value of either Timer A or Timer B.

The source timer for each channel is selected by setting value of the compare x ($x = 0, 1, 2, 3$) timer source bit. Timer A and Timer B can be selected for the source timer to each channel, respectively.

To use each compare channel, set "1" to the compare x output port bit and set the port direction register corresponding to compare channel to output mode.

The compare value for each channel is set to the compare register (low-order) and compare register (high-order).

Writing to the register for each channel is controlled by setting value of compare register write pointer. Writing to each register is in the following order;

1. Set the value of corresponded output compare channel to the compare register write pointer.
2. Write a value to the compare register (low-order) and compare register (high-order).
3. Set "1" to the compare latch y ($y = 00, 01, 10, 11, 20, 21, 30, 31$) re-load bit.

When "1" is set to the compare latch y re-load bit, the value set to the compare register is loaded to compare latch when the next timer underflow.

When count value of timer and setting value of compare latch is matched, compare output trigger occurs.

When "1: Enabled" is set to the compare trigger x enable bit, the output waveform from port is inverted by compare trigger.

When "0: Disabled" is set to the compare trigger x enable bit, the output waveform is not inverted, so port output can be fixed to "H" or "L".

When "0: Positive" is set to the compare x output level latch, the compare output waveform is turned to "H level" at compare latch $x0$'s match and turned to "L level" at compare latch $x1$'s match.

When "1: Negative" is set to the compare x output level latch, the compare output waveform is turned to "L level" at compare latch $x0$'s match and turned to "H level" at compare latch $x1$'s match.

The compare output level of each channel can be confirmed by reading the compare x output status bit.

Compare output interrupt is available when match of each compare channel and timer count value. The interrupt request from each channel can be disabled or enabled by setting value of compare latch y interrupt source bit.

Compare 0,1 (2,3) modulation mode

In compare modulation mode, modulation waveform can be generated by using compare channel 0 and 1, or compare channel 2 and 3. To use this mode,

- Set "1: Enabled" to the compare 0,1 (2, 3) modulation mode bit.
- Set Timer A underflow for Timer B count source.
- Set Timer A for the timer source of compare channel 0 (2).
- Set Timer B for the timer source of compare channel 1 (3).

In this mode, AND waveform of compare 0 (1) and compare 2 (3) is generated from Port P01 and P31, respectively. Accordingly, in order to use this mode, set "1" to the compare 0 output port bit or compare 2 output port bit.

Notes on Output Compare

- When the selected source timer of each compare channel is stopped, written data to compare register is loaded to the compare latch simultaneously.
- Do not write the same data to both of compare latch $x0$ and $x1$.
- When setting value of the compare latch is larger than timer setting value, compare match signal is not generated. Accordingly, the output waveform is fixed to "L" or "H" level.
However, when setting value of another compare latch is smaller than timer setting value, this compare match signal is generated. Accordingly, compare match interrupt occurs.
- When the compare x trigger enable bit is cleared to "0" (disabled), the match trigger to the waveform output circuit is disabled, and the output waveform can be fixed to "L" or "H" level.
However, in this case, the compare match signal is generated. Accordingly, compare match interrupt occurs.

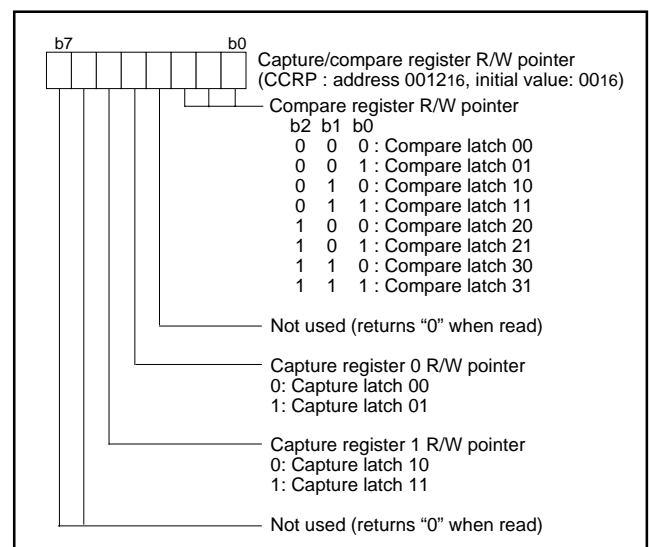


Fig. 30 Structure of capture/compare register R/W pointer

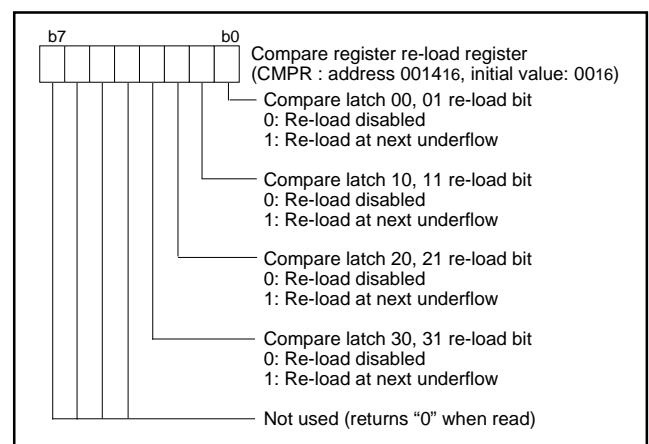


Fig. 31 Structure of compare register re-load register

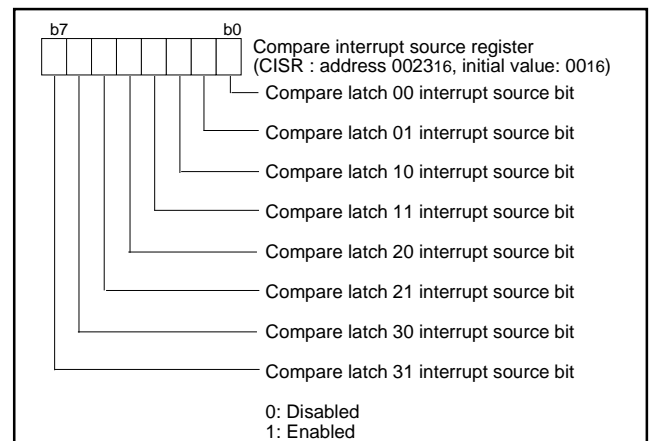
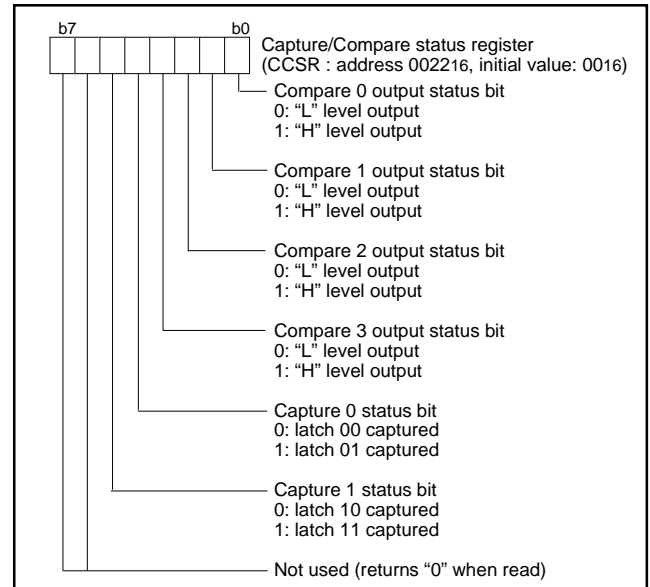
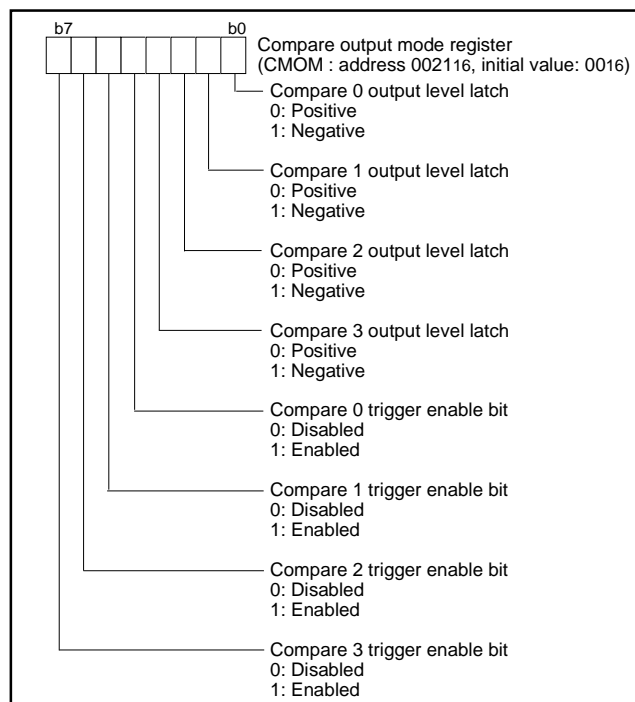
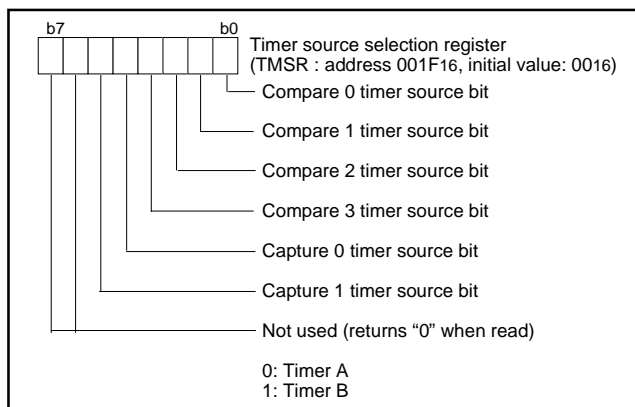
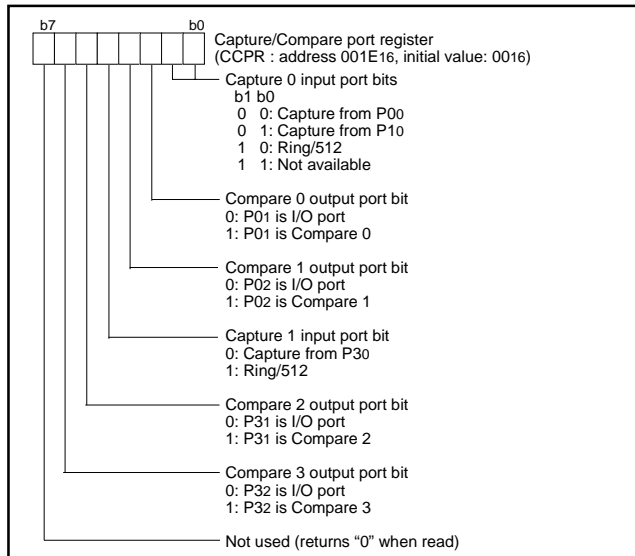


Fig. 34 Structure of compare output mode register

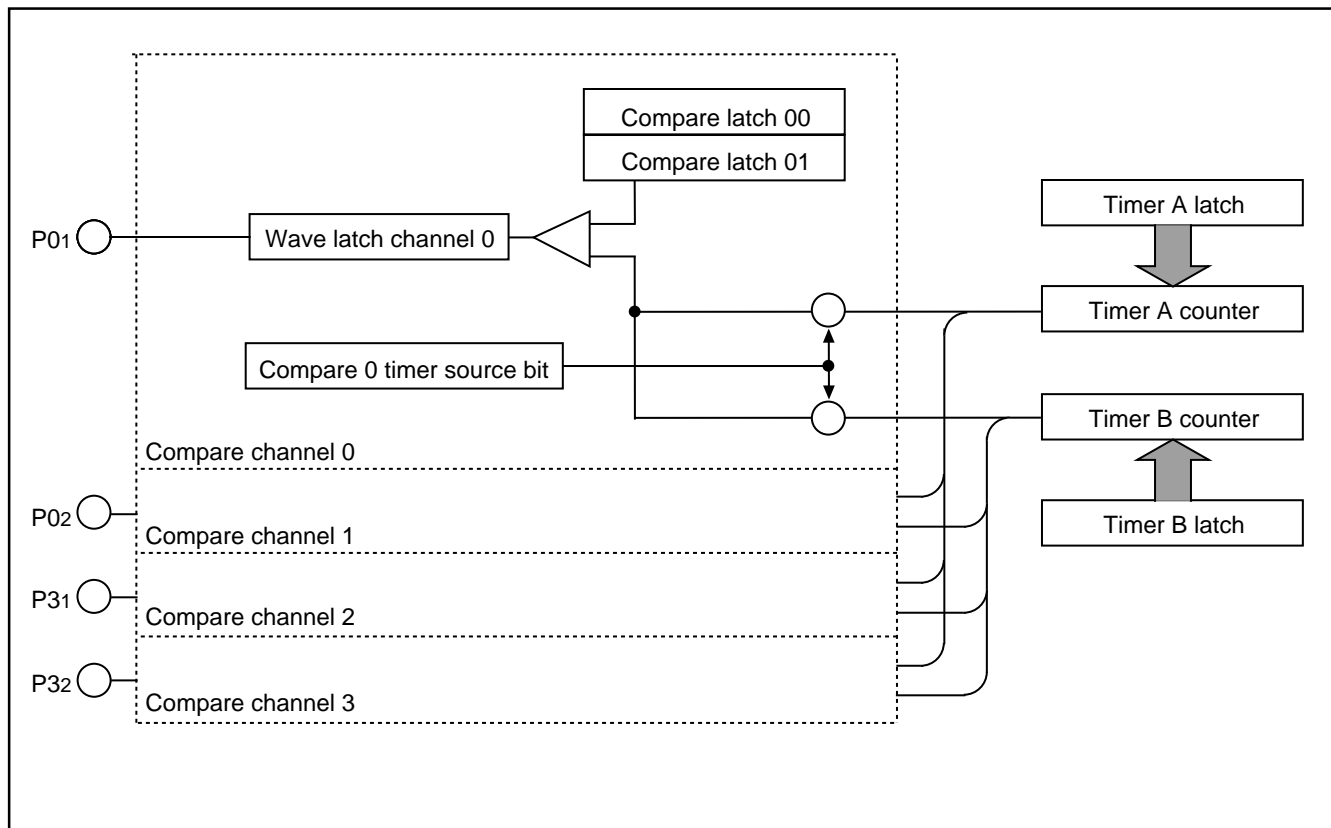


Fig. 37 Block diagram of output compare

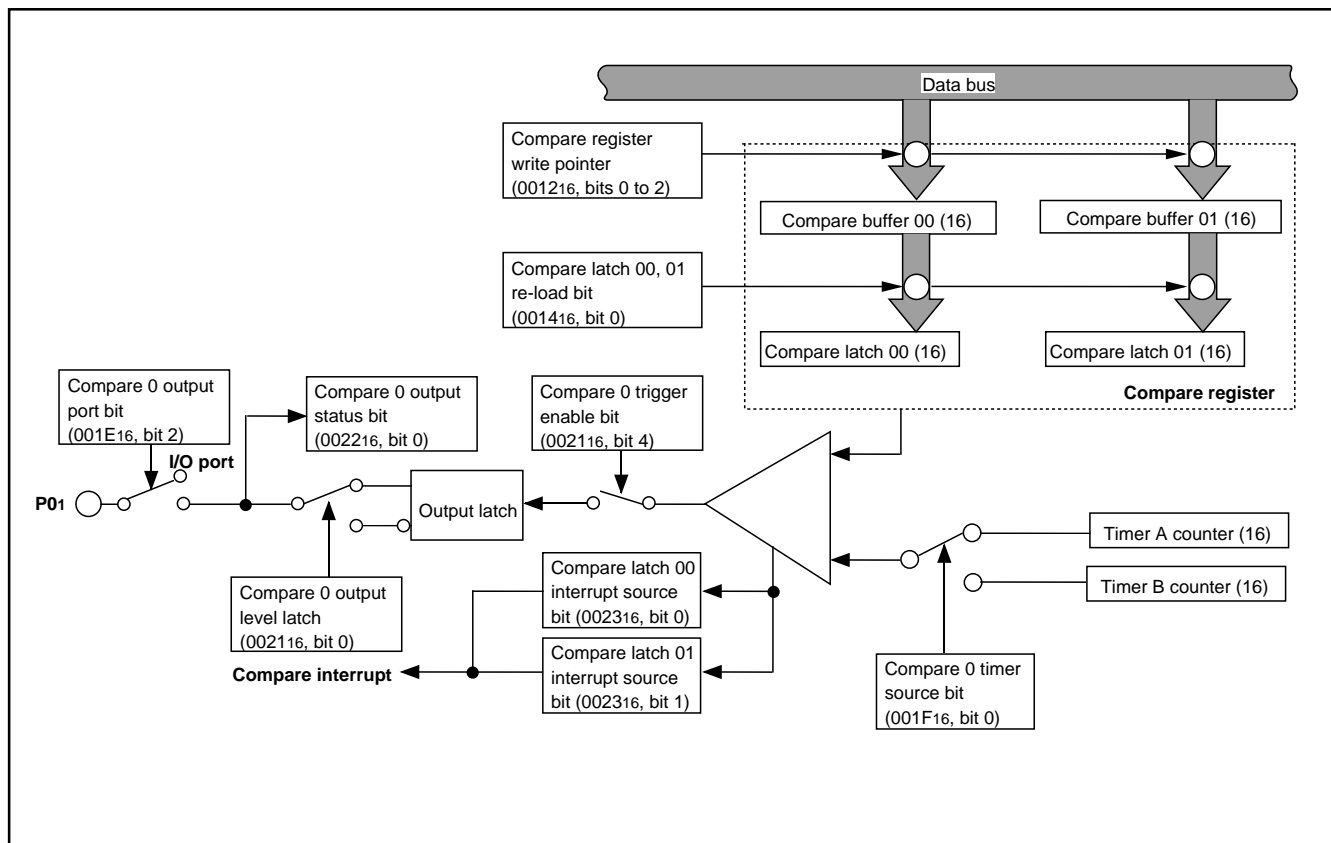


Fig. 38 Block diagram of compare channel 0

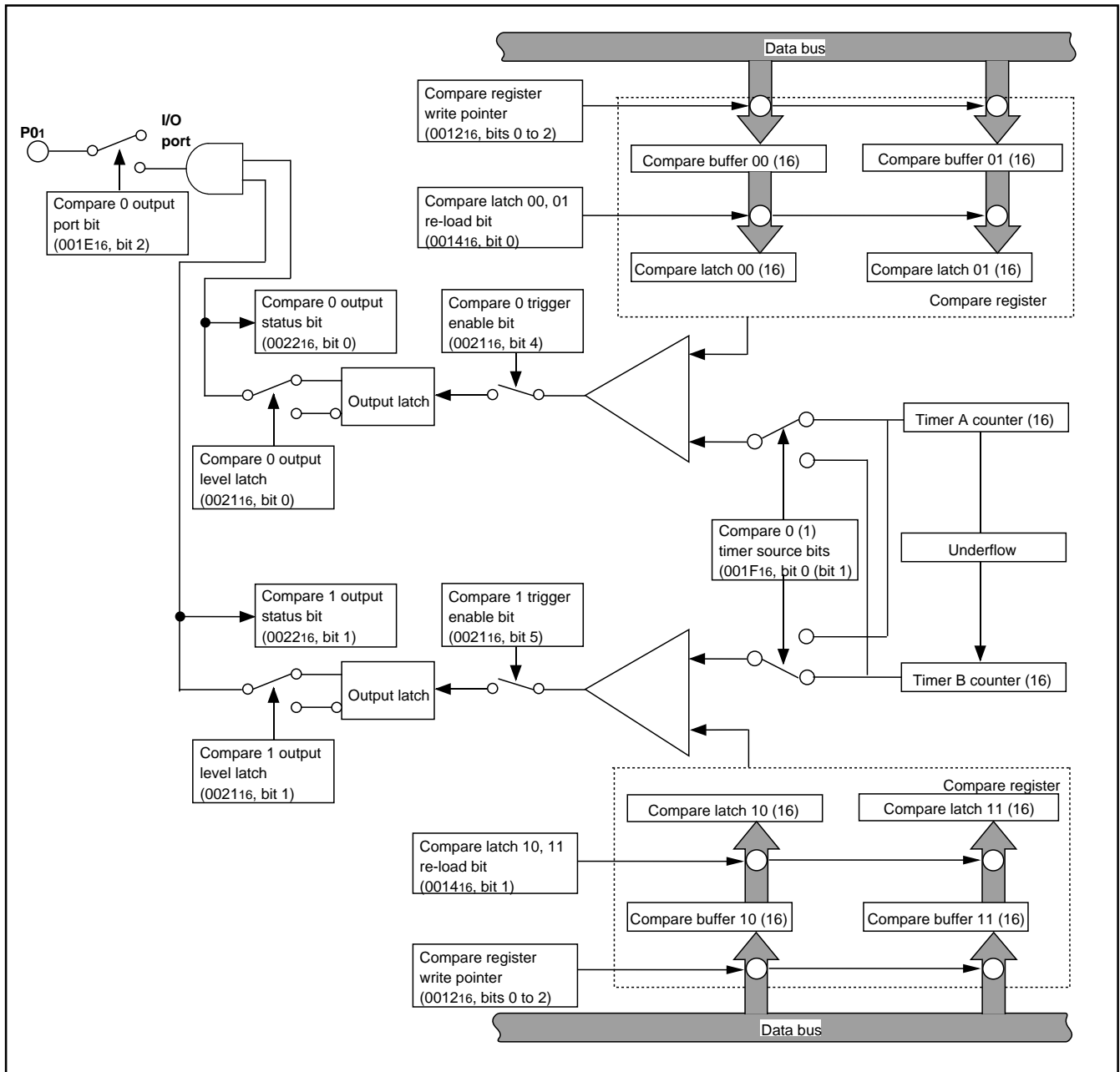


Fig. 39 Block diagram of compare channel 0, 1

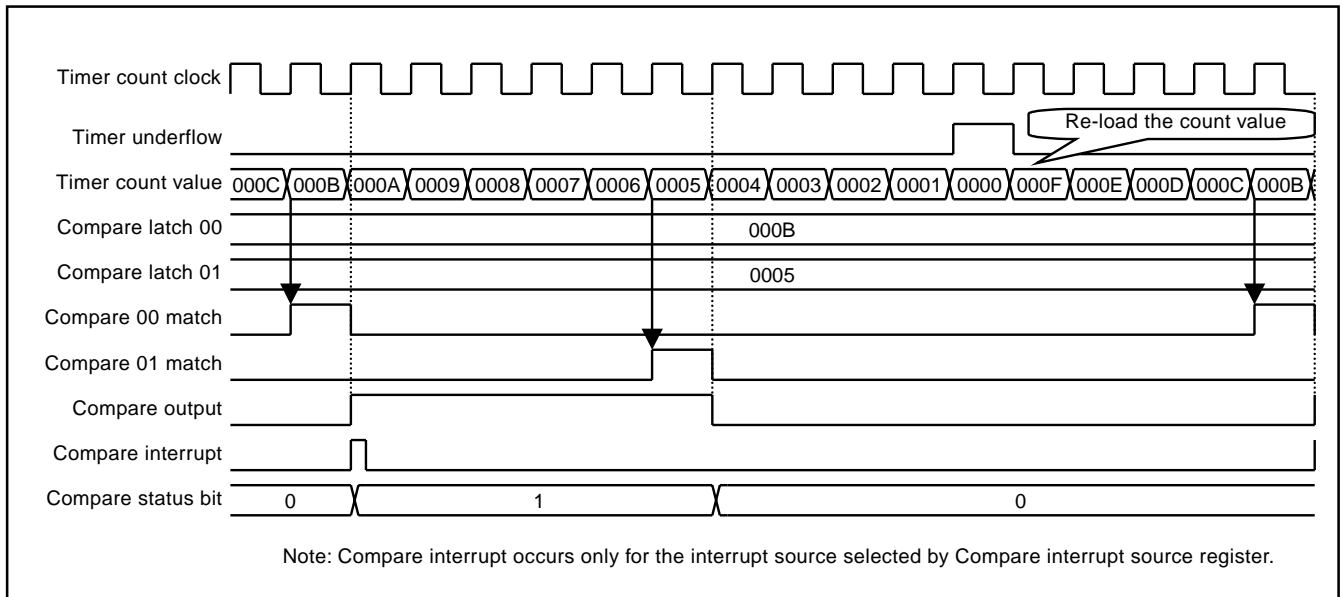


Fig. 40 Output compare mode (general waveform)

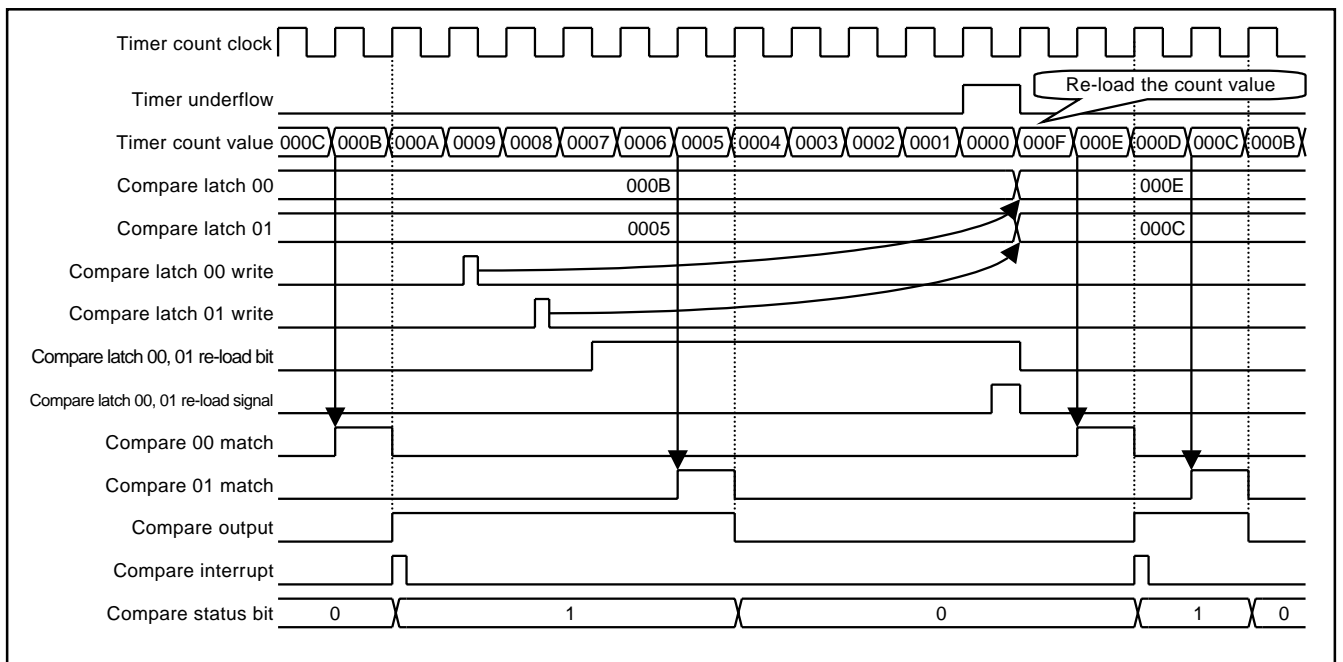
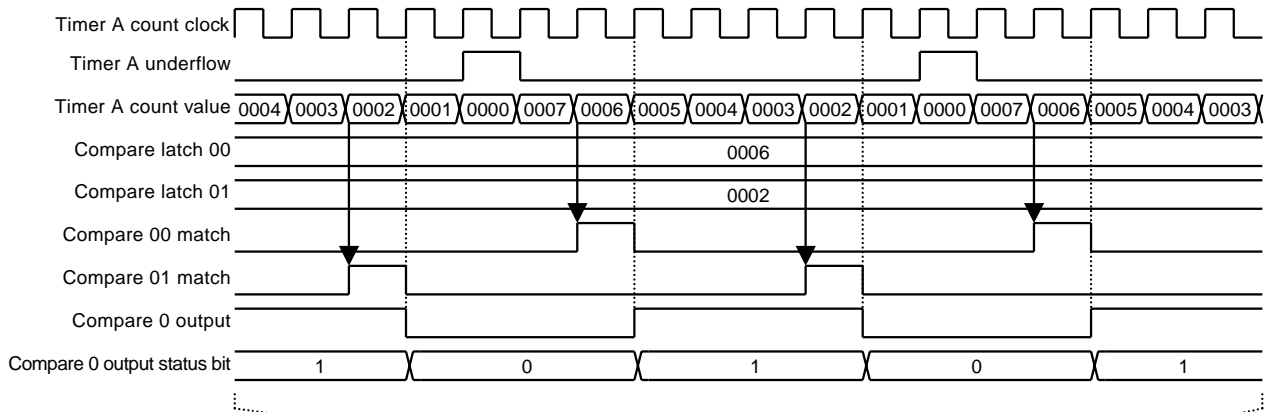
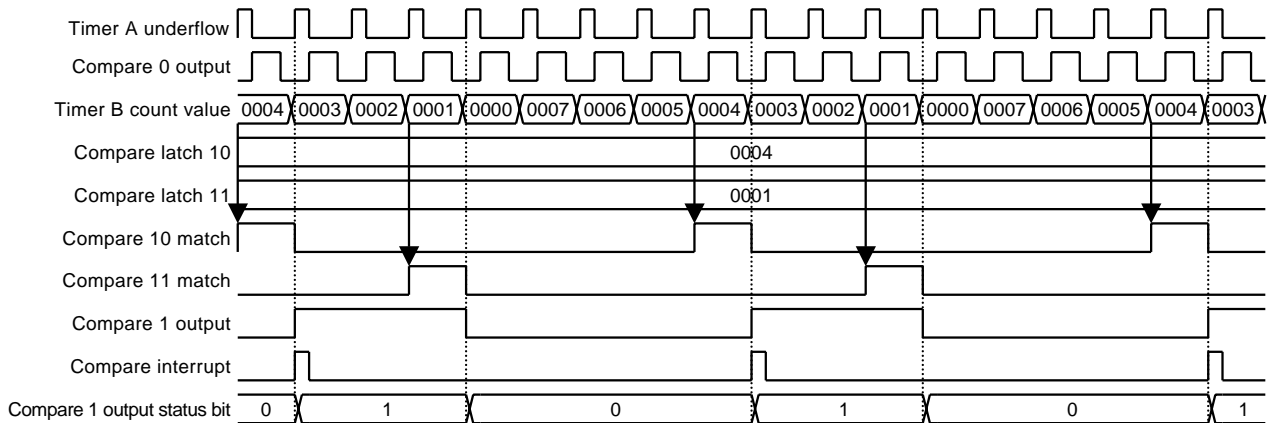
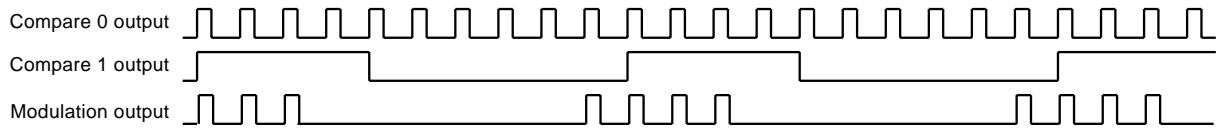
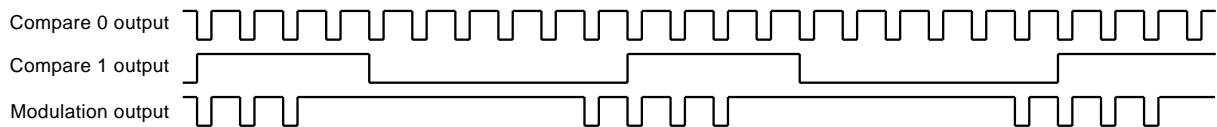
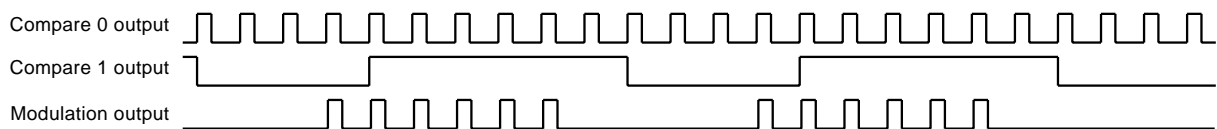
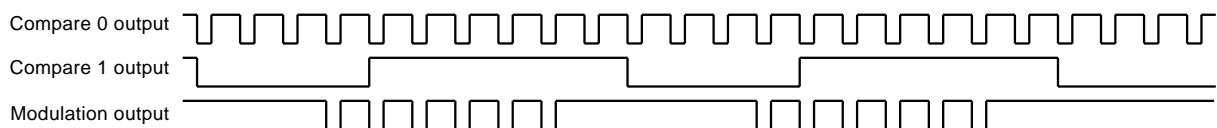


Fig. 41 Output compare mode (compare register write timing)

Carrier wave generated by Compare 0**Modulation of output waveform generated by Compare 1****Port output waveform:**

Note: Compare interrupt occurs only for the interrupt source selected by Compare interrupt source register.

Fig. 42 Output compare mode (compare 0, 1 modulation mode)

1. When Compare 0 output level latch is “Positive”, Compare 1 output level latch is “Positive”.**2. When Compare 0 output level latch is “Negative”, Compare 1 output level latch is “Positive”.****3. When Compare 0 output level latch is “Positive”, Compare 1 output level latch is “Negative”.****4. When Compare 0 output level latch is “Negative”, Compare 1 output level latch is “Negative”.****Fig. 43 Output compare mode (compare 0, 1 modulation mode: effect of output level latch)**

Input capture

7542 group has 2-input capture channels. Each channel (0 and 1) has the same function and can be used to capture count value of either Timer A or Timer B.

The source timer for each channel is selected by setting value of the capture x (x = 0, 1) timer source bit. Timer A and Timer B can be selected for the source timer to each channel, respectively.

To use each capture channel, set the capture x input port bits and set the port direction register corresponding to capture channel to input mode.

The input capture circuit retains the count value of selected timer when external trigger is input. The timer count value is retained to the capture latch x0 when rising edge is input and is retained to the capture latch x1 when falling edge is input.

The count value of timer can be retained by software by capture y (y = 00, 01, 10, 11) software trigger bit too. When "1" is set to this bit, count value of timer is retained to the corresponded capture latch.

When reading from the capture y software trigger bit is executed, "0" is read out.

The latest status of capture latch can be confirmed by reading of the capture x status bit. This bit indicates the capture latch which latest data is in.

The valid trigger edge for capture interrupt is set by the capture x interrupt edge selection bits. (Regardless of the setting value of capture x interrupt edge selection bits, timer count values for both edges are retained to the capture latch.)

Each capture input has the noise filter circuit that judges continuous 4-time same level with sampling clock to be valid. The sampling clock of noise filter is set by the capture x noise filter clock selection bits.

Reading from the register for each channel is controlled by setting value of the capture register read pointer. Reading from each register is in the following order;

1. Set the value of the corresponded input capture channel to the capture register read pointer.
2. Read from the capture register (low-order) and capture register (high-order).

■ Notes on Input Capture

- If the capture trigger is input while the capture register (low-order and high-order) is in read, captured value is changed between high-order reading and low-order reading. Accordingly, some countermeasure by software is recommended, for example comparing the values that twice of read.
- When the ring-oscillator is selected for Timer A count source, Timer A cannot be used for the capture source timer.
Timer B cannot be used for the capture source timer when the system is in the following state;
 - CPU operation clock source: XIN oscillation
 - Timer B count source: Timer A underflow
 - Timer A count source: Ring oscillator output
- When writing "1" to capture latch x0 (x1) software trigger bit of capture latch x0 and x1 at the same time, or external trigger and software trigger occur simultaneously, the set value of capture x status bit is undefined.
- When setting the interrupt active edge selection bit and noise filter clock selection bit of external interrupt CAP0, CAP1, the interrupt request bit may be set to "1".
When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.
 - ① Set the corresponding interrupt enable bit to "0" (disabled).
 - ② Set the interrupt edge selection bit or noise filter clock selection bit.
 - ③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
 - ④ Set the corresponding interrupt enable bit to "1" (enabled).
- When the capture interrupt is used as the interrupt for return from stop mode, set the capture x noise filter clock selection bits to "00 (Filter stop)".

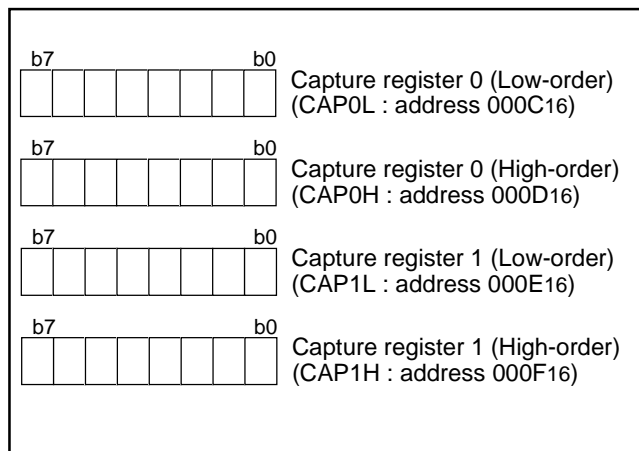


Fig. 44 Structure of capture software trigger register

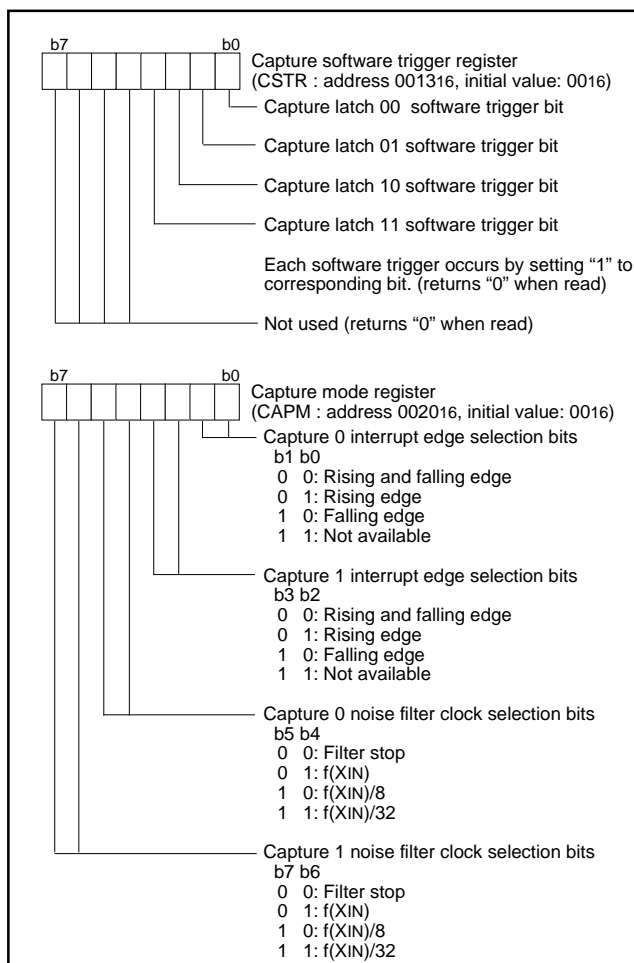


Fig. 45 Structure of capture software trigger register/capture mode register

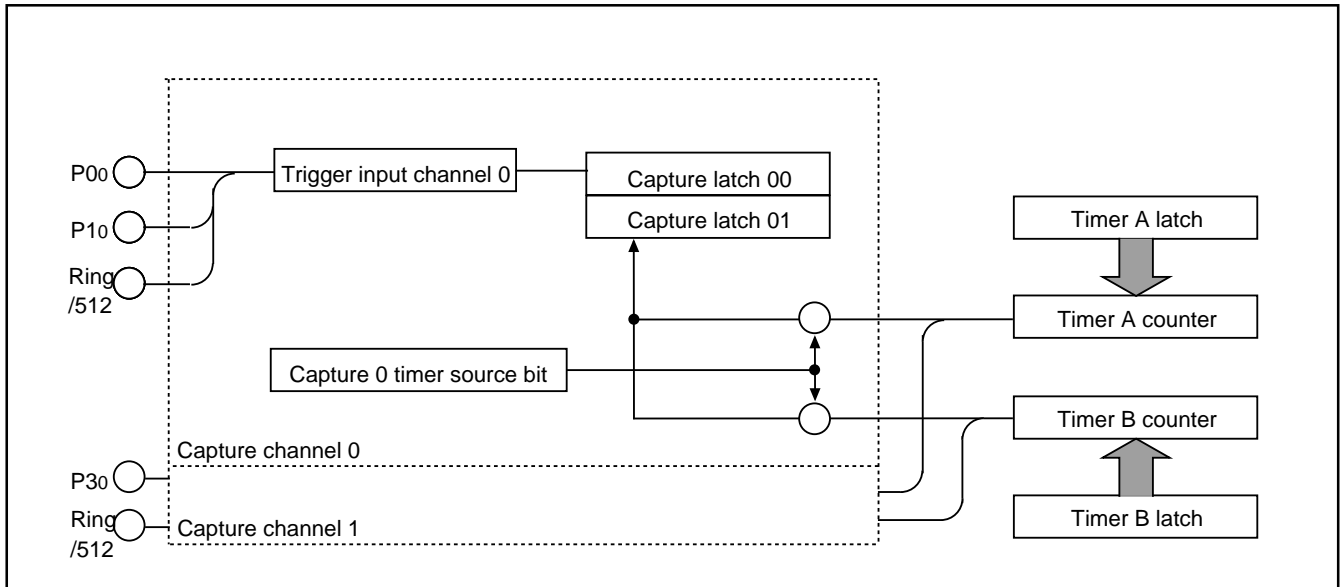


Fig. 46 Block diagram of input capture

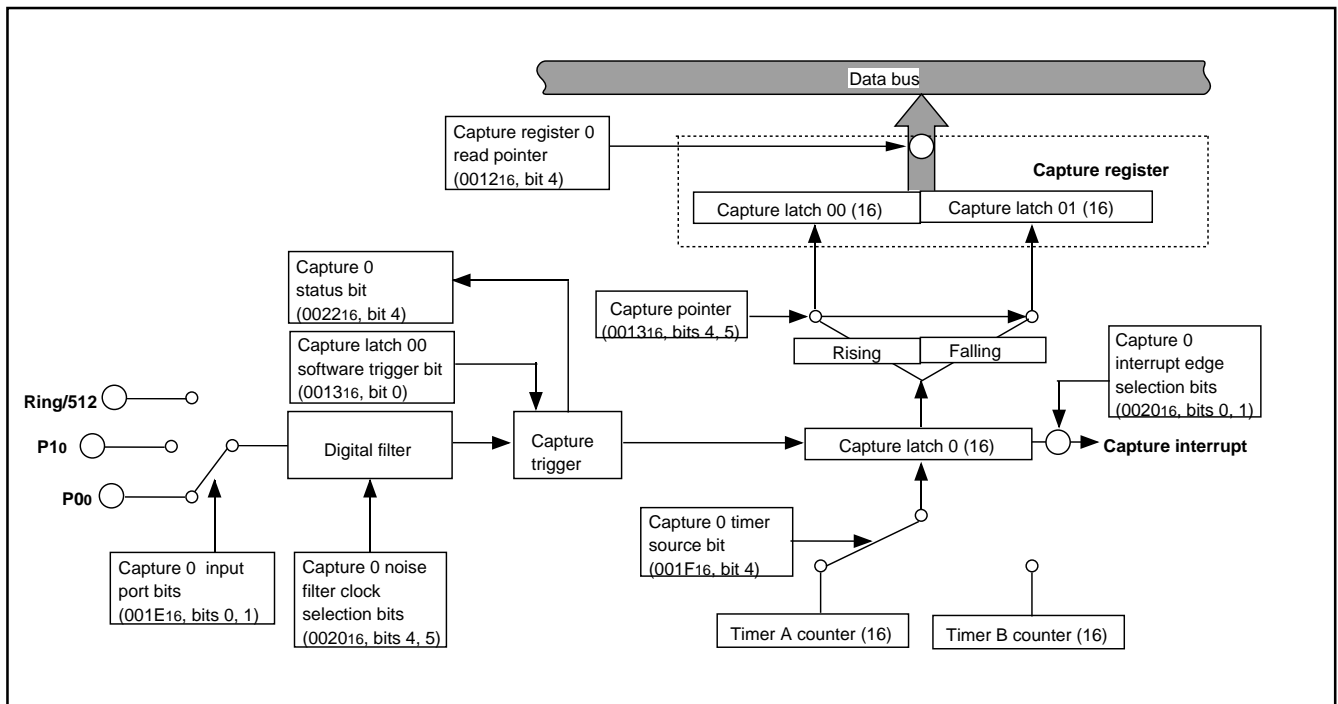


Fig. 47 Block diagram of capture channel 0

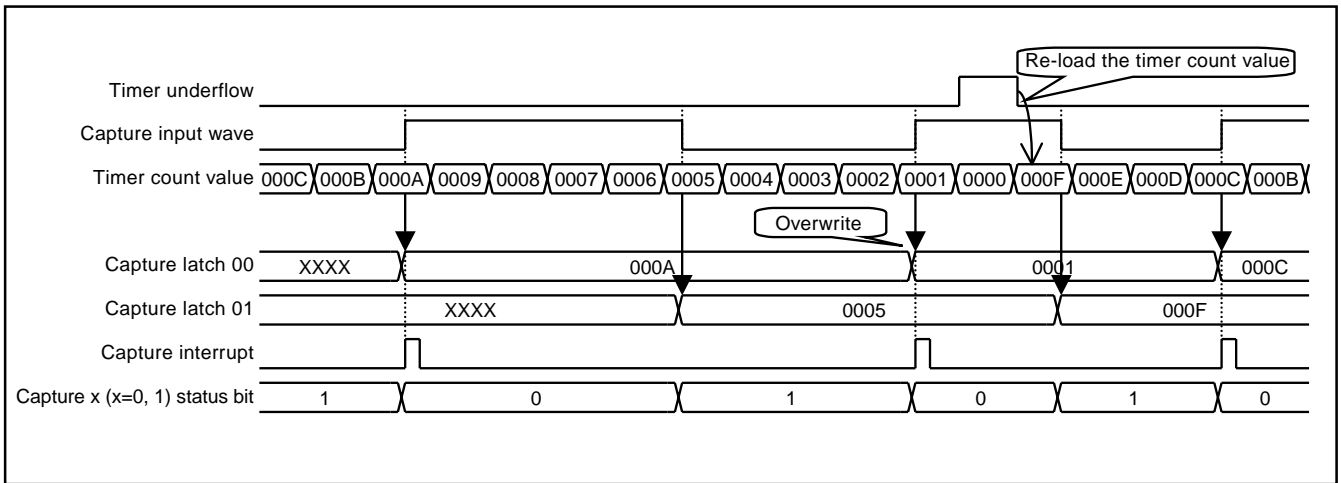


Fig. 48 Capture interrupt edge selection = "rising edge"

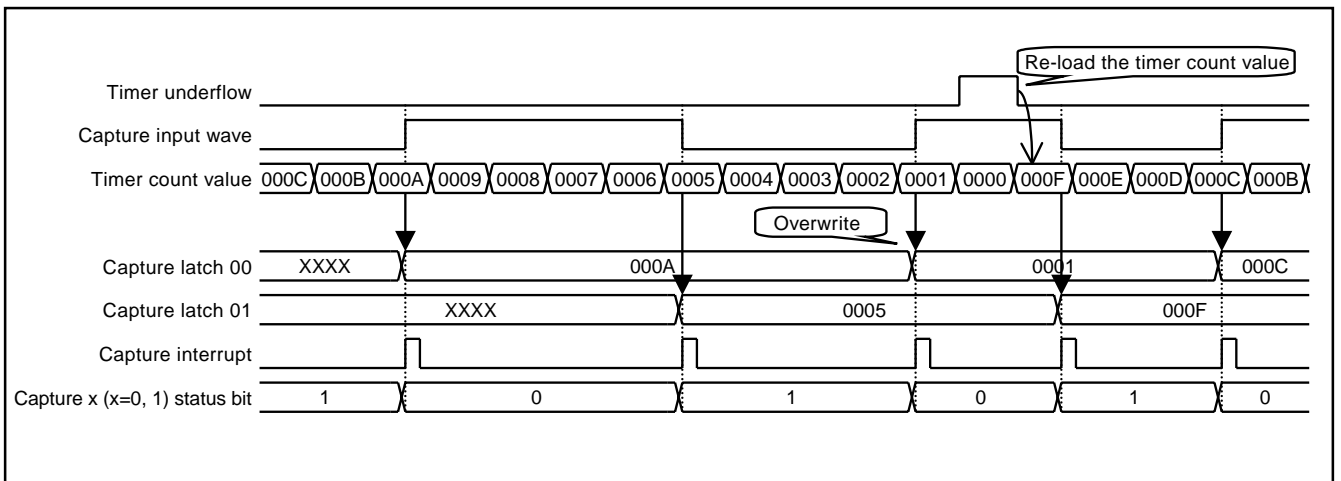


Fig. 49 Capture interrupt edge selection = "rising and falling edge"

Serial I/O

The 7542 Group has Serial I/O1 and Serial I/O2. Except that Serial I/O1 has the bus collision detection function, they have the same function.

Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O1 Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6) to "1".

For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

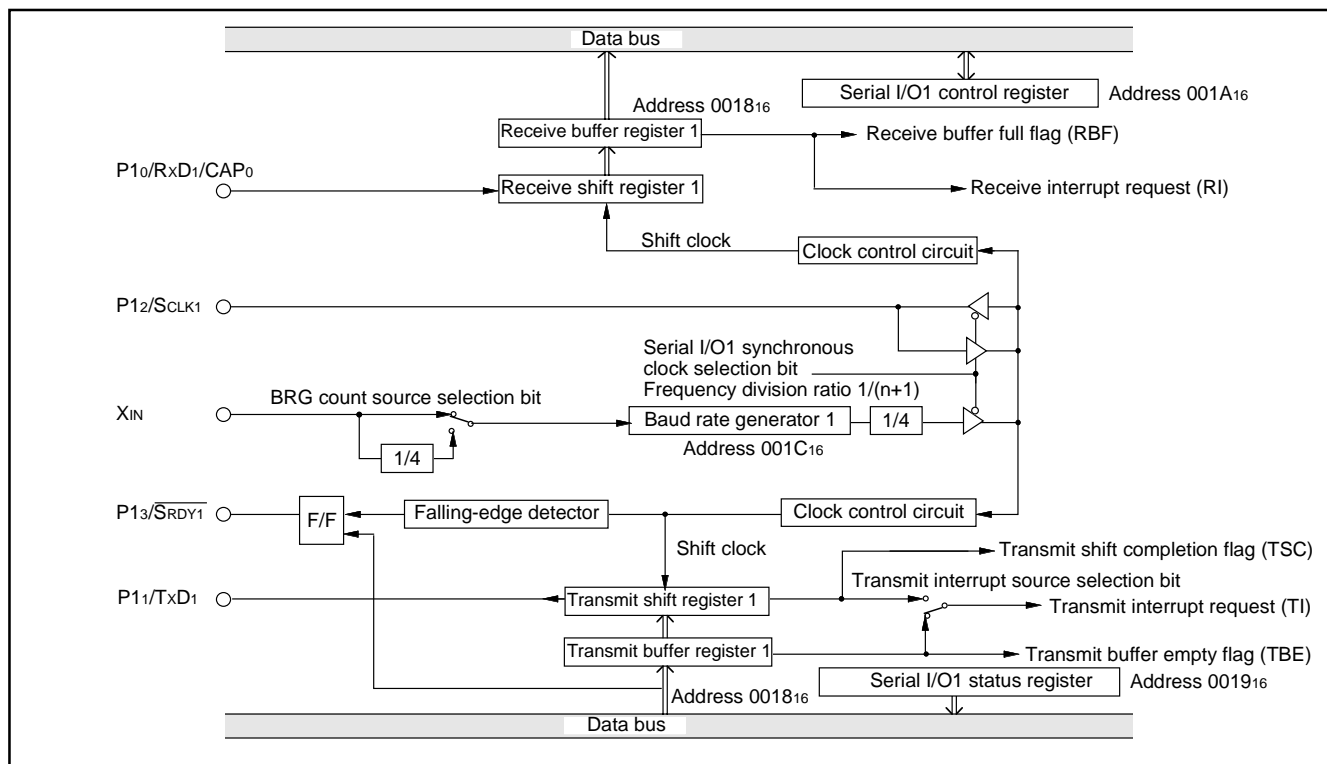


Fig. 50 Block diagram of clock synchronous serial I/O1

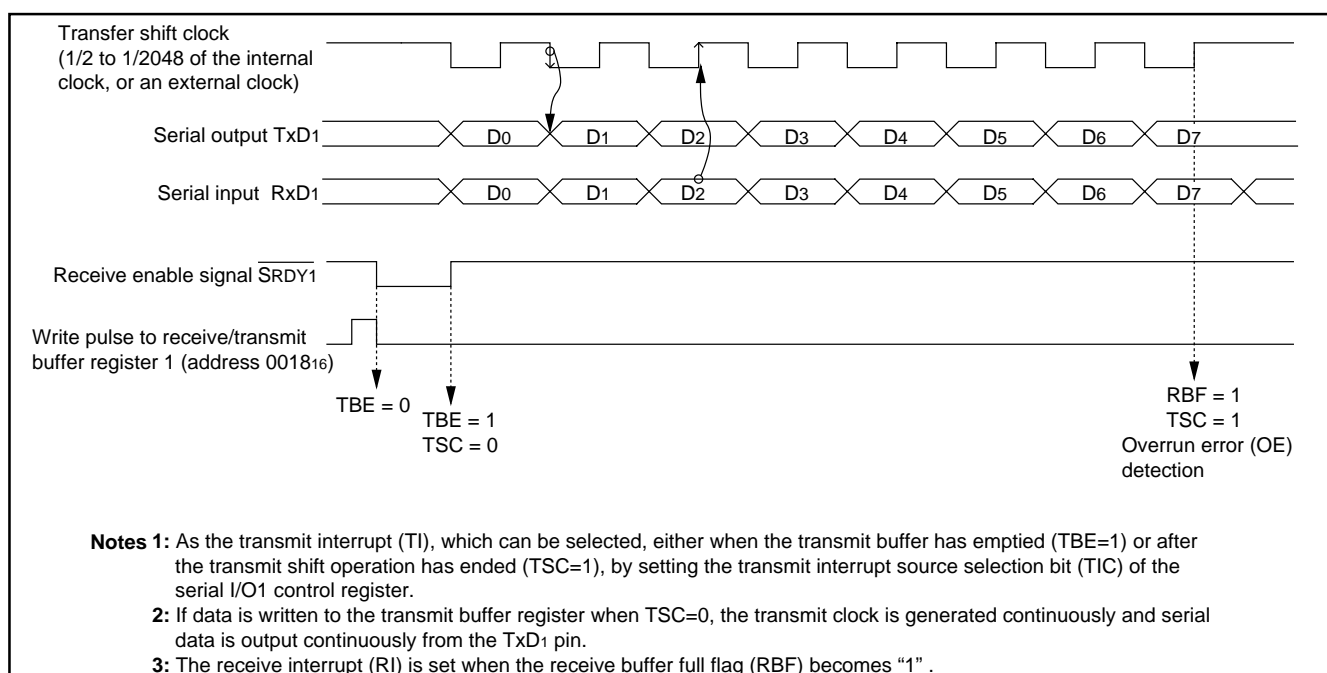


Fig. 51 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O1 (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit of the serial I/O1 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

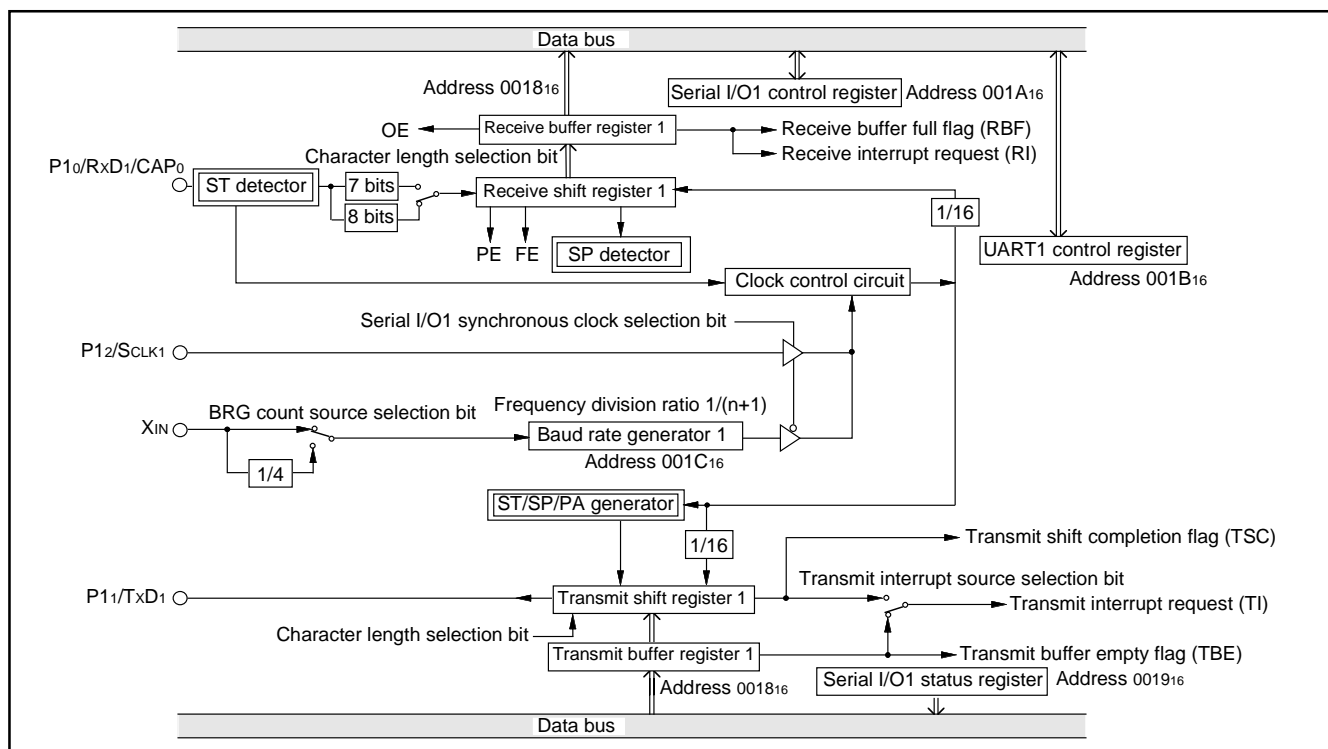


Fig. 52 Block diagram of UART serial I/O1

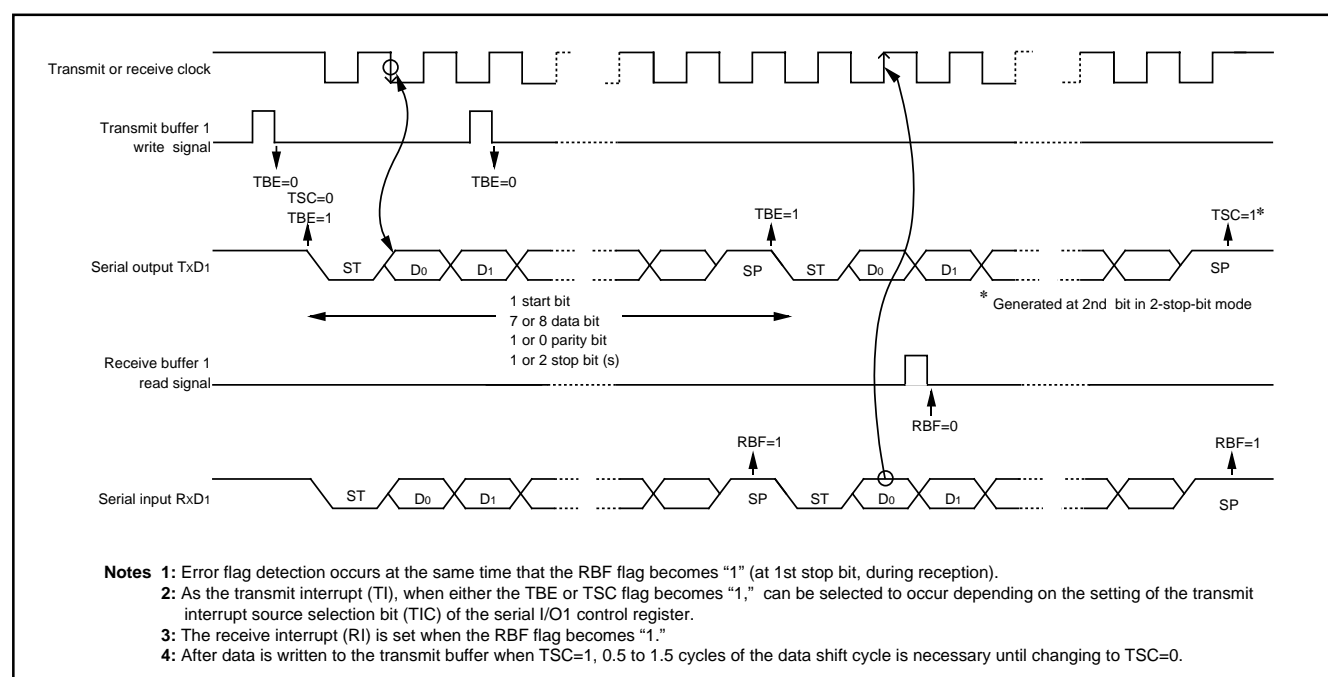


Fig. 53 Operation of UART serial I/O1 function

[Transmit buffer register 1/receive buffer register 1 (TB1/RB1)] 0018₁₆

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O1 status register (SIO1STS)] 0019₁₆

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O1 control register (SIO1CON)] 001A₁₆

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART1 control register (UART1CON)] 001B₁₆

The UART1 control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of a data transfer and one bit (bit 4) which is always valid and sets the output structure of the P11/TxD1 pin.

[Baud rate generator 1 (BRG1)] 001C₁₆

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

■ Notes on Serial I/O1**• Serial I/O interrupt**

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

- ① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
- ② Set the transmit enable bit to "1".
- ③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- ⑤ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O1 is enabled.

The functions of P12 and P13 are switched with the setting values of a serial I/O1 mode selection bit and a serial I/O1 synchronous clock selection bit as follows.

(1) Serial I/O1 mode selection bit → "1" :

Clock synchronous type serial I/O is selected.

Setup of a serial I/O1 synchronous clock selection bit

"0" : P12 pin turns into an output pin of a synchronous clock.

"1" : P12 pin turns into an input pin of a synchronous clock.

Setup of a $\overline{\text{SRDY}}$ output enable bit (SRDY)

"0" : P13 pin can be used as a normal I/O pin.

"1" : P13 pin turns into a $\overline{\text{SRDY}}$ output pin.

(2) Serial I/O1 mode selection bit → "0" :

Clock asynchronous (UART) type serial I/O is selected.

Setup of a serial I/O1 synchronous clock selection bit

"0" : P12 pin can be used as a normal I/O pin.

"1" : P12 pin turns into an input pin of an external clock.

When clock asynchronous (UART) type serial I/O is selected, it is P13 pin. It can be used as a normal I/O pin.

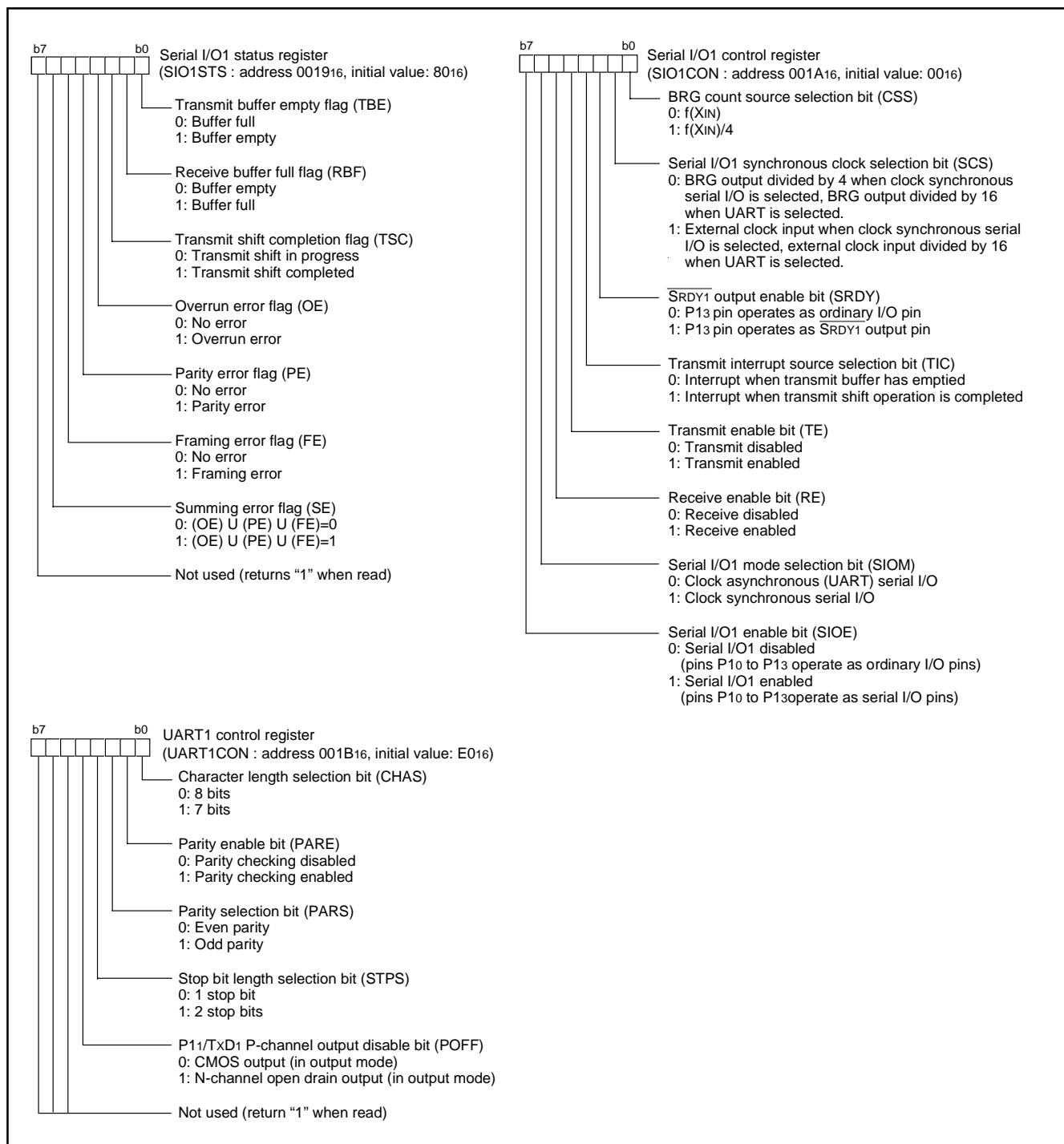


Fig. 54 Structure of serial I/O1-related registers

Bus collision detection (SIO1)

SIO1 can detect a bus collision by setting UART1 bus collision detection interrupt enable bit.

When transmission is started in the clock synchronous or asynchronous (UART) serial I/O mode, the transmit pin TxD1 is compared with the receive pin RxD1 in synchronization with rising edge of transmit shift clock. If they do not coincide with each other, a bus collision detection interrupt request occurs.

When a transmit data collision is detected between LSB and MSB of transmit data in the clock synchronous serial I/O mode or between the start bit and stop bit of transmit data in UART mode, a bus collision detection can be performed by both the internal clock and the external clock.

A block diagram is shown in Fig. 56.

A timing diagram is shown in Fig. 57.

Note: Bus collision detection can be used when SIO1 is operating at full-duplex communication. When SIO1 is operating at half-duplex communication, set bus collision detection interrupt to be disabled.

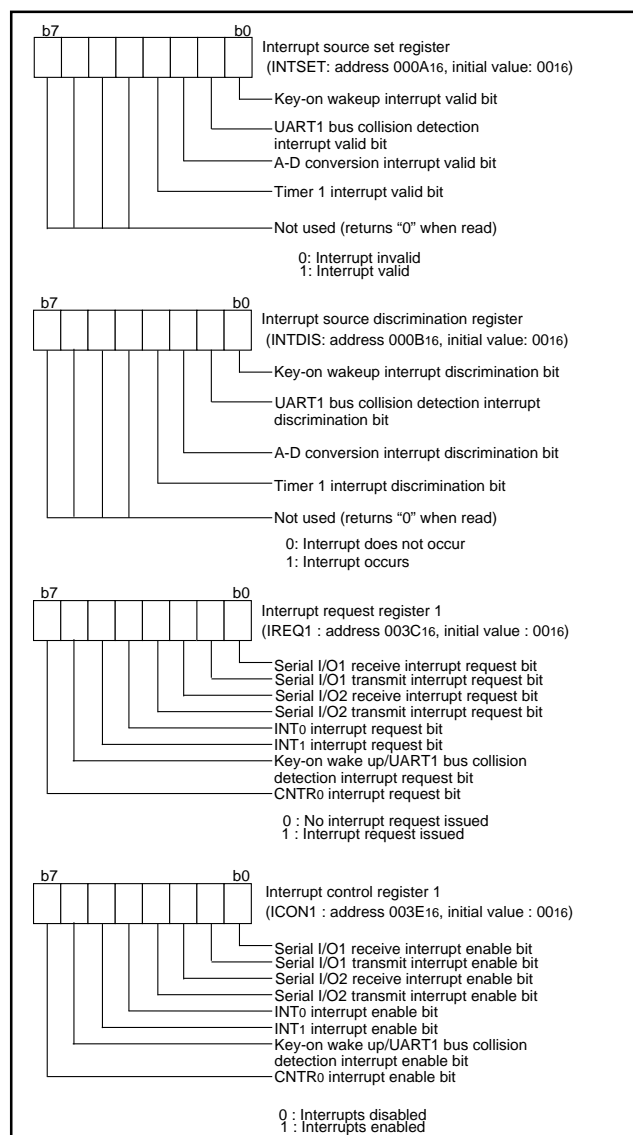


Fig. 55 Bus collision detection circuit related registers

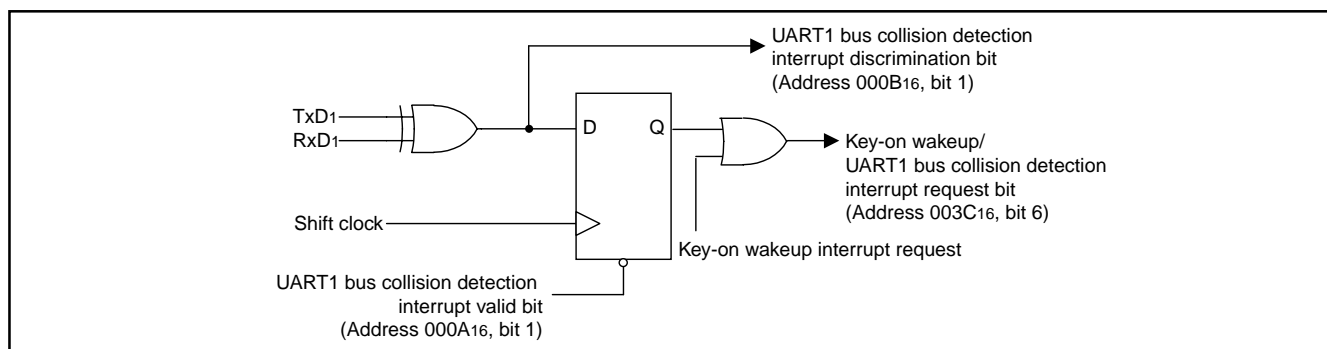


Fig. 56 Block diagram of bus collision detection interrupt circuit

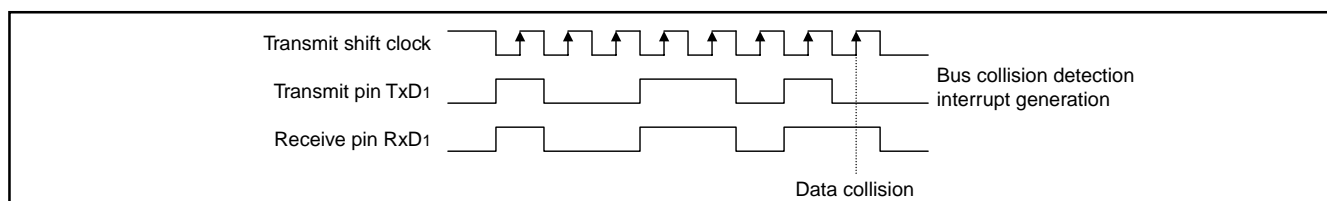


Fig. 57 Timing diagram of bus collision detection interrupt

●Serial I/O2

Serial I/O2 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O2 Mode

Clock synchronous serial I/O2 mode can be selected by setting the serial I/O2 mode selection bit of the serial I/O2 control register (bit 6) to "1".

For clock synchronous serial I/O2, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

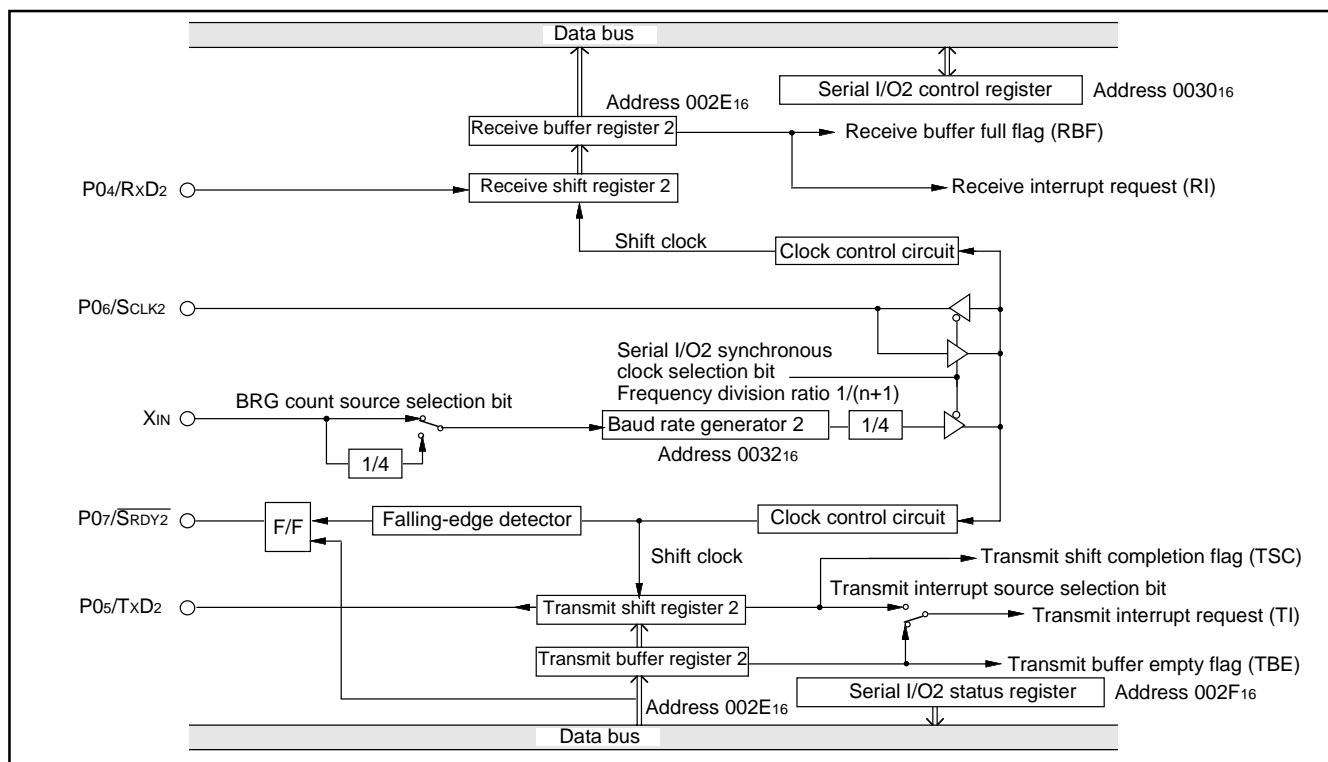


Fig. 58 Block diagram of clock synchronous serial I/O2

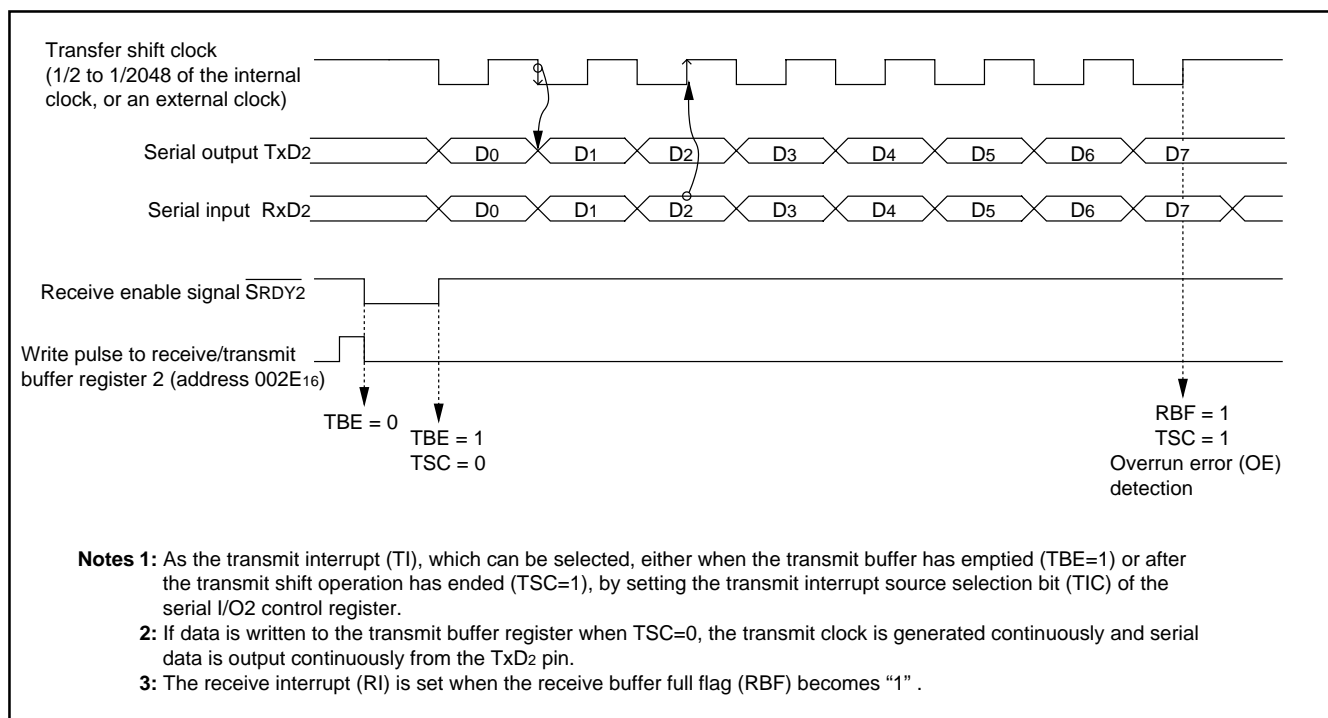


Fig. 59 Operation of clock synchronous serial I/O2 function

(2) Asynchronous Serial I/O2 (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O2 mode selection bit of the serial I/O2 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

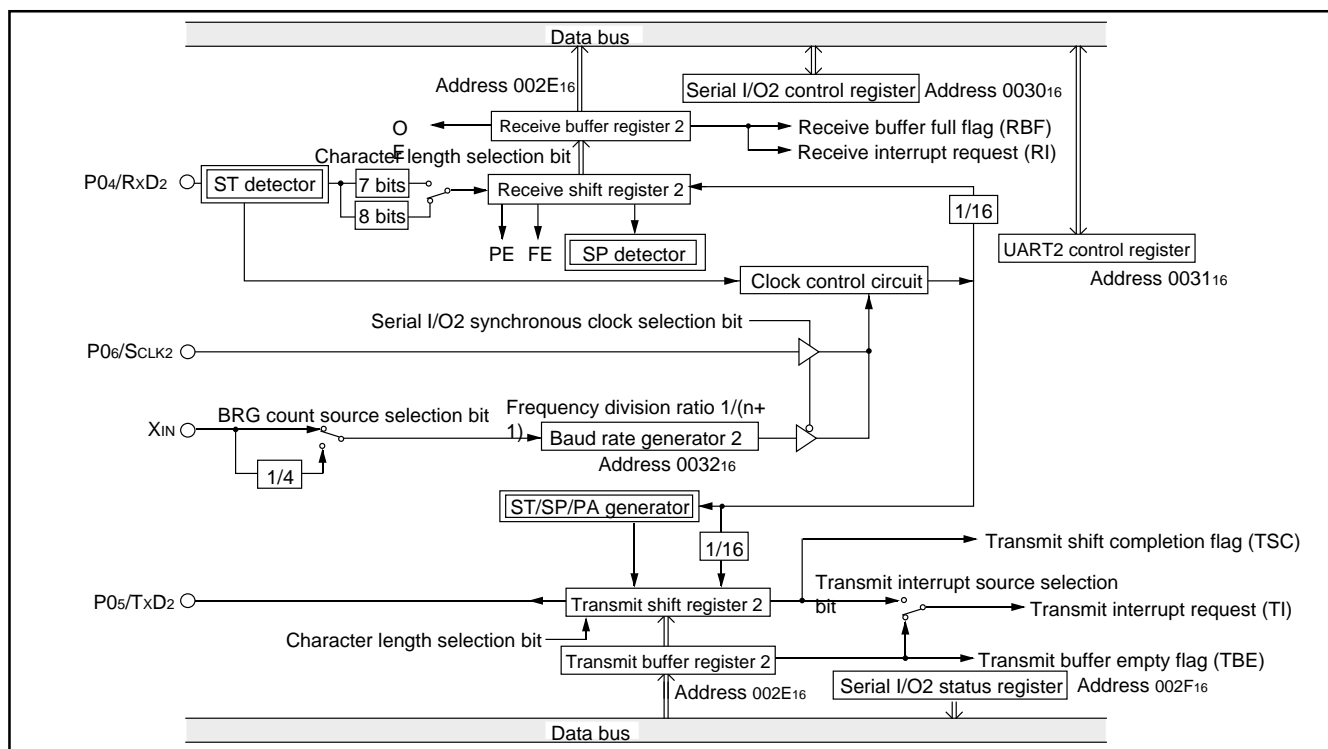


Fig. 60 Block diagram of UART serial I/O2

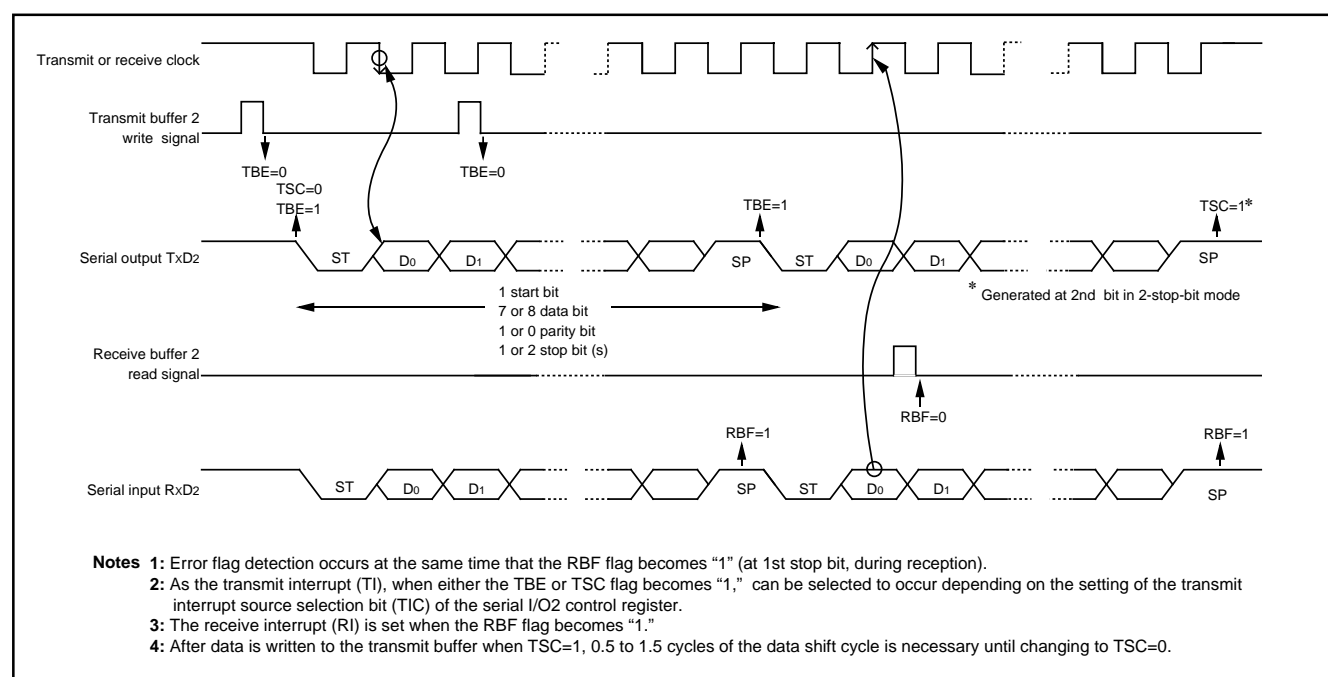


Fig. 61 Operation of UART serial I/O2 function

[Transmit buffer register 2/receive buffer register 2 (TB2/RB2)] 002E16

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O2 status register (SIO2STS)] 002F16

The read-only serial I/O2 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O2 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O2 enable bit SIOE (bit 7 of the serial I/O2 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O2 status register are initialized to "0" at reset, but if the transmit enable bit of the serial I/O2 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O2 control register (SIO2CON)] 003016

The serial I/O2 control register consists of eight control bits for the serial I/O2 function.

[UART2 control register (UART2CON)] 003116

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P05/TxD2 pin.

[Baud rate generator 2 (BRG2)] 003216

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

■ Notes on Serial I/O2**• Serial I/O interrupt**

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

- ① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
- ② Set the transmit enable bit to "1".
- ③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- ⑤ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O2 is enabled.

The functions of P06 and P07 are switched with the setting values of a serial I/O2 mode selection bit and a serial I/O2 synchronous clock selection bit as follows.

(1) Serial I/O2 mode selection bit → "1" :

Clock synchronous type serial I/O is selected.

Setup of a serial I/O2 synchronous clock selection bit

"0" : P06 pin turns into an output pin of a synchronous clock.

"1" : P06 pin turns into an input pin of a synchronous clock.

Setup of a $\overline{\text{SRDY2}}$ output enable bit (SRDY)

"0" : P07 pin can be used as a normal I/O pin.

"1" : P07 pin turns into a $\overline{\text{SRDY2}}$ output pin.

(2) Serial I/O2 mode selection bit → "0" :

Clock asynchronous (UART) type serial I/O is selected.

Setup of a serial I/O2 synchronous clock selection bit

"0" : P06 pin can be used as a normal I/O pin.

"1" : P06 pin turns into an input pin of an external clock.

When clock asynchronous (UART) type serial I/O is selected, it is P07 pin. It can be used as a normal I/O pin.

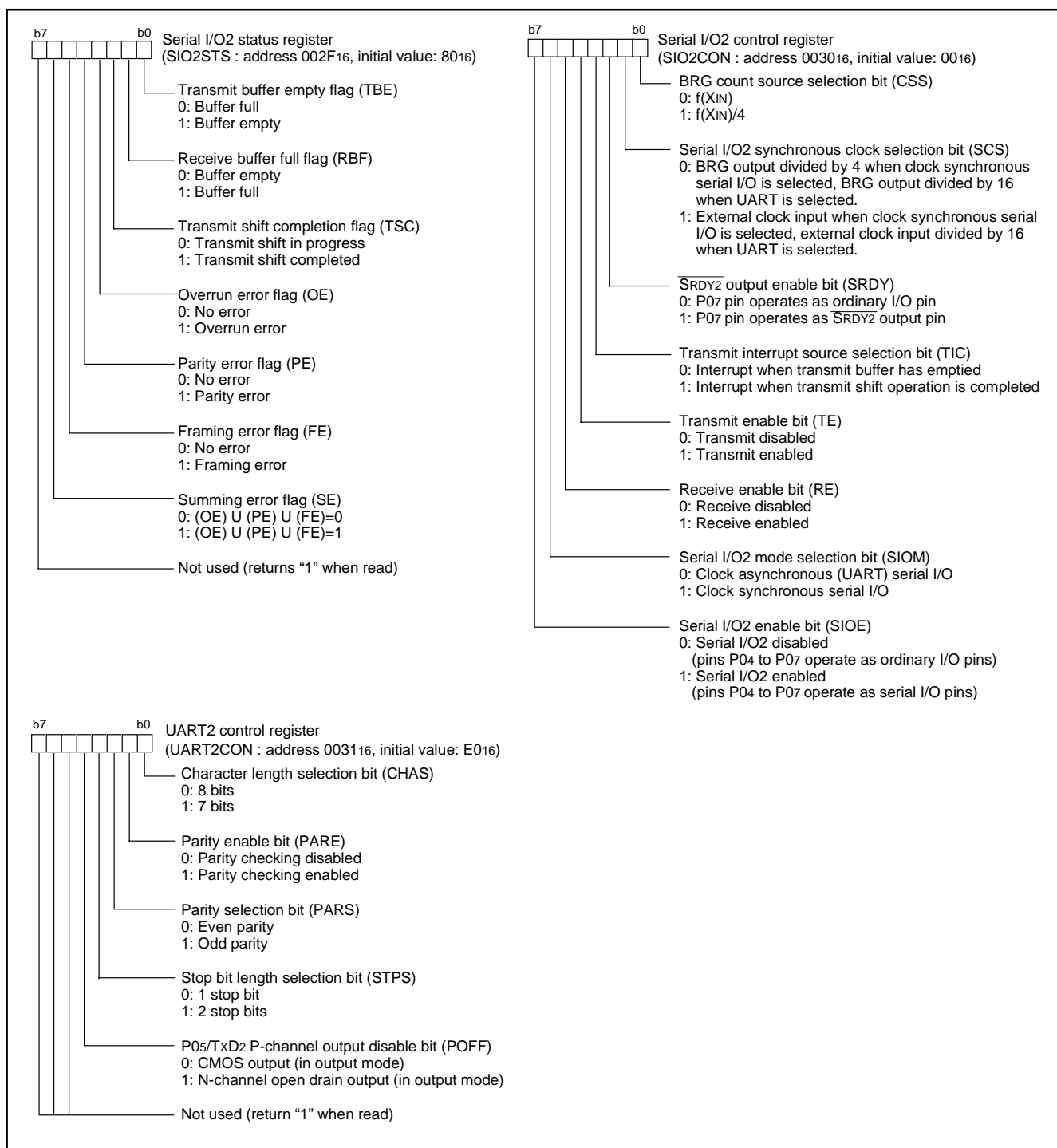


Fig. 62 Structure of serial I/O2-related registers

A-D Converter

The functional blocks of the A-D converter are described below.

[A-D conversion register] AD

The A-D conversion register is a read-only register that stores the result of A-D conversion. Do not read out this register during an A-D conversion.

[A-D control register] ADCON

The A-D control register controls the A-D converter. Bit 2 to 0 are analog input pin selection bits. Bit 4 is the A-D conversion completion bit. The value of this bit remains at "0" during A-D conversion, and changes to "1" at completion of A-D conversion.

A-D conversion is started by setting this bit to "0".

[Comparison voltage generator]

The comparison voltage generator divides the voltage between AVSS and VREF by 1024, and outputs the divided voltages.

[Channel selector]

The channel selector selects one of ports P27/AN7 to P20/AN0, and inputs the voltage to the comparator.

[Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A-D conversion register. When A-D conversion is completed, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to "1". Because the comparator is constructed linked to a capacitor, set $f(XIN)$ to 500 kHz or more during A-D conversion.

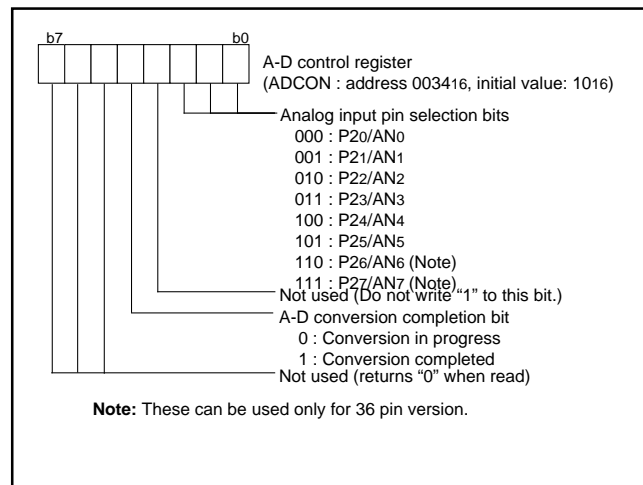


Fig. 63 Structure of A-D control register

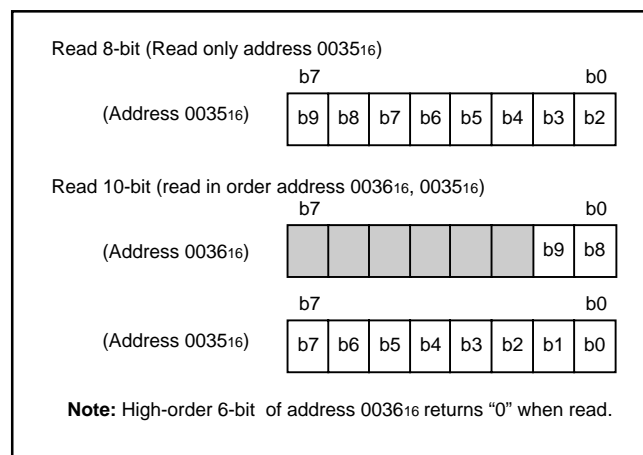


Fig. 64 Structure of A-D conversion register

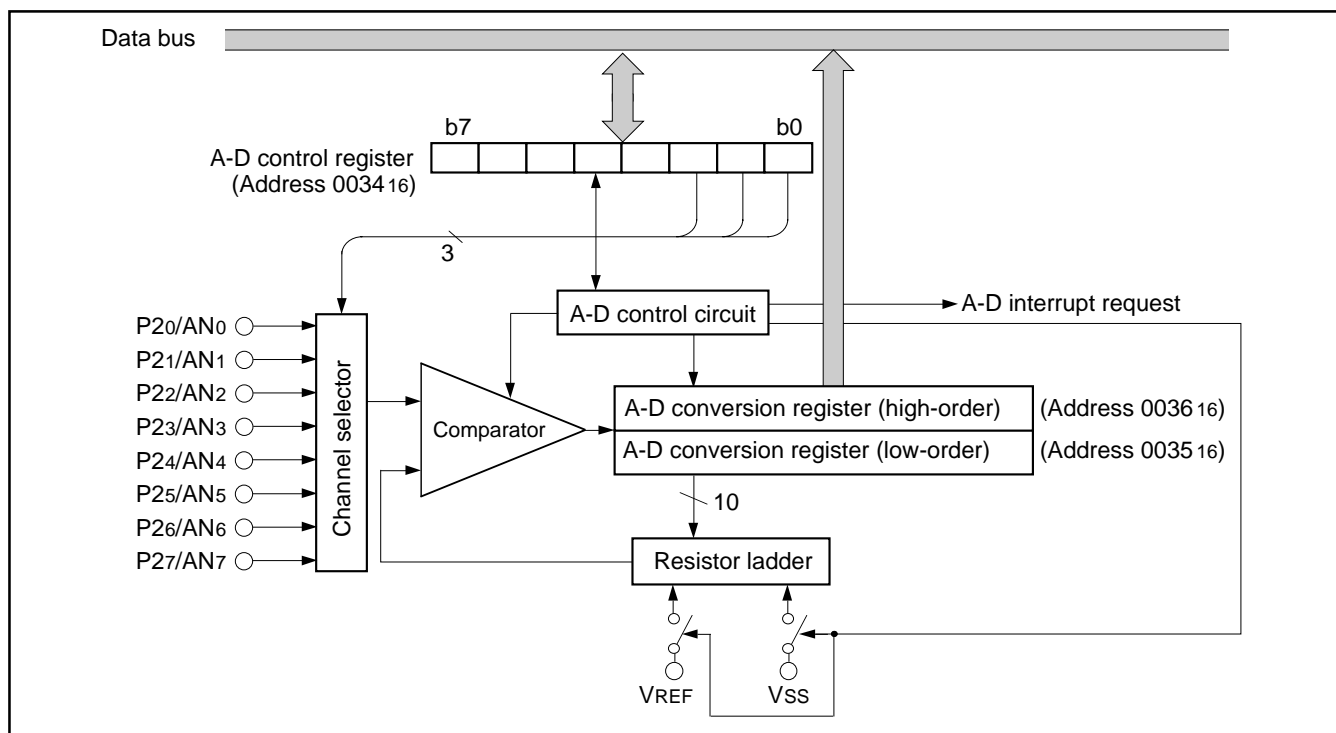


Fig. 65 Block diagram of A-D converter

Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

Standard operation of watchdog timer

The watchdog timer stops when the watchdog timer control register (address 0039₁₆) is not set after reset. Writing an optional value to the watchdog timer control register (address 0039₁₆) causes the watchdog timer to start to count down. When the watchdog timer H underflows, an internal reset occurs. Accordingly, it is programmed that the watchdog timer control register (address 0039₁₆) can be set before an underflow occurs.

When the watchdog timer control register (address 0039₁₆) is read, the values of the high-order 6-bit of the watchdog timer H, STP instruction disable bit and watchdog timer H count source selection bit are read.

Initial value of watchdog timer

By a reset or writing to the watchdog timer control register (address 0039₁₆), the watchdog timer H is set to "FF₁₆" and the watchdog timer L is set to "FF₁₆".

Operation of watchdog timer H count source selection bit

A watchdog timer H count source can be selected by bit 7 of the watchdog timer control register (address 0039₁₆). When this bit is "0", the count source becomes a watchdog timer L underflow signal. The detection time is 131.072 ms at $f(XIN)=8$ MHz. When this bit is "1", the count source becomes $f(XIN)/16$. In this case, the detection time is 512 μ s at $f(XIN)=8$ MHz. This bit is cleared to "0" after reset.

Operation of STP instruction disable bit

When the watchdog timer is in operation, the STP instruction can be disabled by bit 6 of the watchdog timer control register (address 0039₁₆).

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled, and an internal reset occurs if the STP instruction is executed.

Once this bit is set to "1", it cannot be changed to "0" by program. This bit is cleared to "0" after reset.

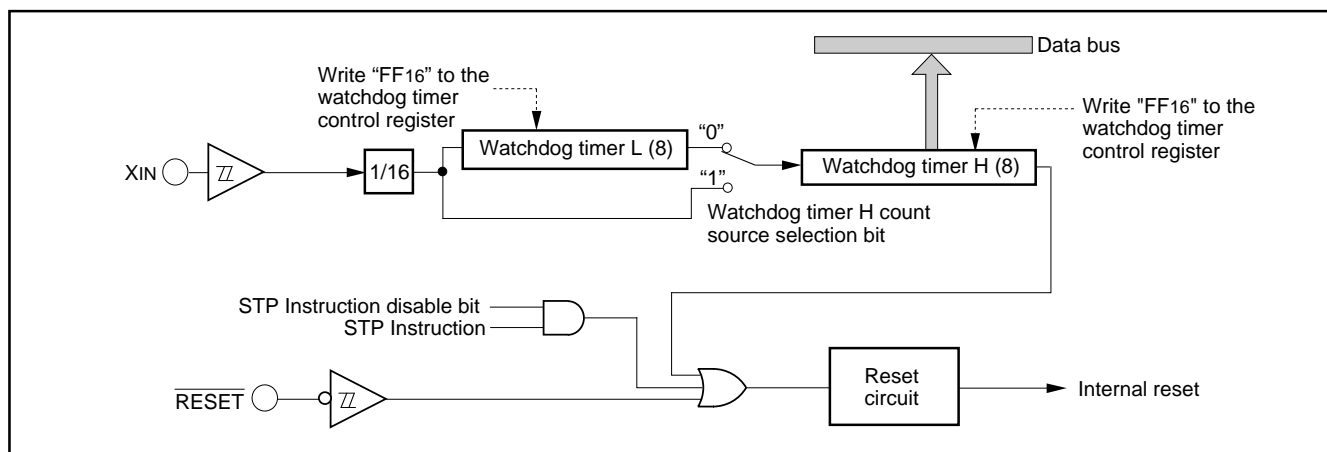


Fig. 66 Block diagram of watchdog timer

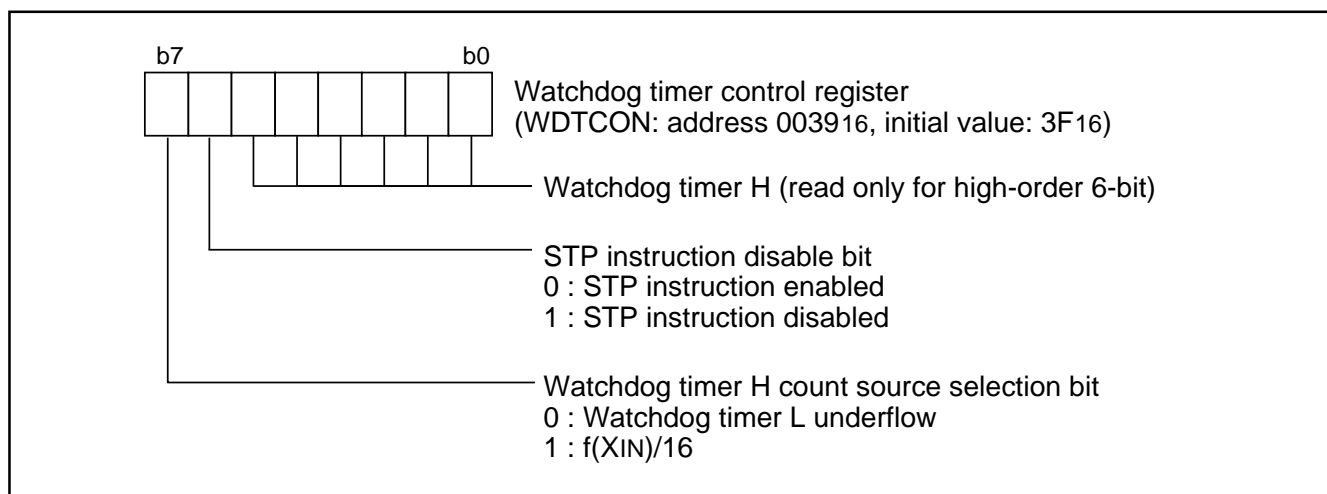


Fig. 67 Structure of watchdog timer control register

Reset Circuit

The 7542 group starts operation by the built-in ring oscillator after system is released from reset.

Accordingly, when the rising of power supply voltage passes 2.2V, set the reset input voltage to become below 0.2V_{CC} (0.44V).

Moreover, switch CPU clock to the external oscillator after the rising of power supply voltage passes the minimum operation voltage and after an oscillation is stabilized.

Note: The minimum operation voltage is decided by the division ratio of an external oscillator's frequency and a CPU clock.
Decide on an external oscillator's oscillation stabilizing time after fully evaluating an oscillator's stabilizing time used.

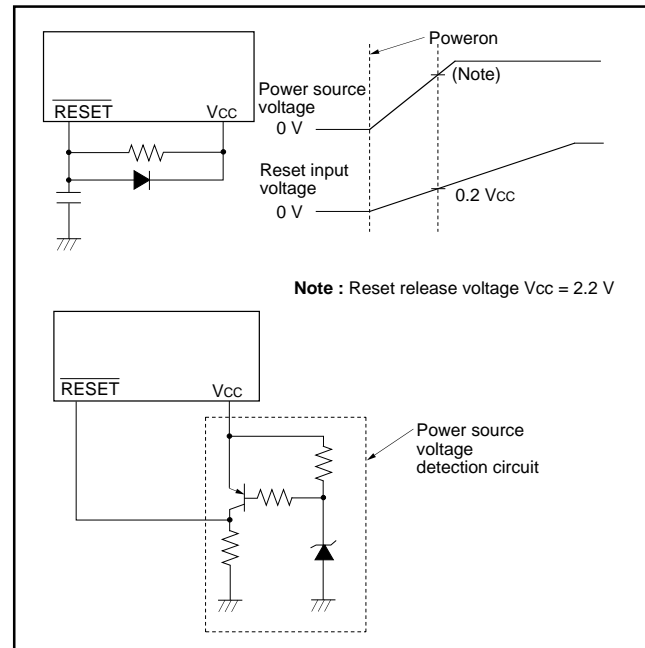


Fig. 68 Example of reset circuit

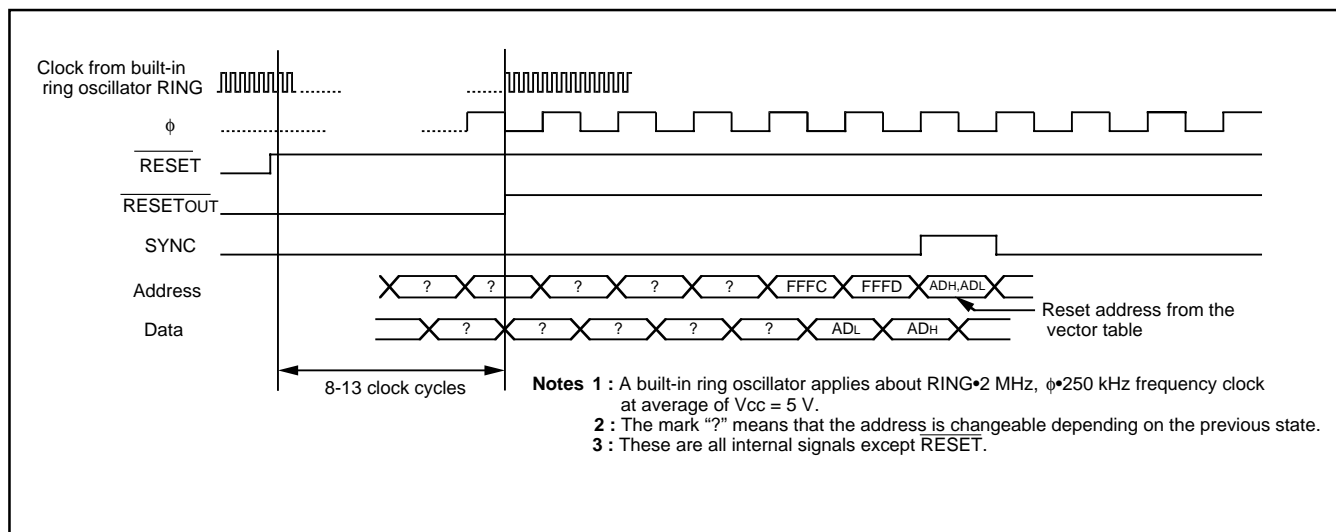


Fig. 69 Timing diagram at reset

	Address	Register contents
(1) Port P0 direction register (P0D)	000116	0016
(2) Port P1 direction register (P1D)	000316	X X X 0 0 0 0 0
(3) Port P2 direction register (P2D)	000516	0016
(4) Port P3 direction register (P3D)	000716	0016
(5) Interrupt source set register (INTSET)	000A16	0016
(6) Interrupt source discrimination register (INTDIS)	000B16	0016
(7) Compare register (low-order) (CMPL)	001016	0016
(8) Compare register (high-order) (CMPH)	001116	0016
(9) Capture/Compare register R/W pointer (CCRP)	001216	0016
(10) Capture software trigger register (CSTR)	001316	0016
(11) Compare register re-load register (CMPR)	001416	0016
(12) Port P0P3 drive capacity control register (DCCR)	001516	0016
(13) Pull-up control register (PULL)	001616	0016
(14) Port P1P3 control register (P1P3C)	001716	0016
(15) Serial I/O1 status register (SIO1STS)	001916	1 0 0 0 0 0 0 0
(16) Serial I/O1 control register (SIO1CON)	001A16	0016
(17) UART1 control register (UART1CON)	001B16	1 1 1 0 0 0 0 0
(18) Timer A, B mode register (TABM)	001D16	0016
(19) Capture/Compare port register (CCPR)	001E16	0016
(20) Timer source selection register (TMSR)	001F16	0016
(21) Capture mode register (CAPM)	002016	0016
(22) Compare output mode register (CMOM)	002116	0016
(23) Capture/Compare status register (CCSR)	002216	0016
(24) Compare interrupt source register (CISR)	002316	0016
(25) Timer A (low-order) (TAL)	002416	FF16
(26) Timer A (high-order) (TAH)	002516	FF16
(27) Timer B (low-order) (TBL)	002616	FF16
(28) Timer B (high-order) (TBH)	002716	FF16
(29) Prescaler 1 (PRE1)	002816	FF16
(30) Timer 1 (T1)	002916	0116
(31) Timer count source set register (TCSS)	002A16	0016
(32) Timer X mode register (TXM)	002B16	0016
(33) Prescaler X (PREX)	002C16	FF16
(34) Timer X (TX)	002D16	FF16
(35) Serial I/O2 control register (SIO2STS)	002F16	1 0 0 0 0 0 0 0
(36) Serial I/O2 register (SIO2CON)	003016	0016
(37) UART2 control register (UART2CON)	003116	1 1 1 0 0 0 0 0
(38) A-D control register (ADCON)	003416	0 0 0 1 0 0 0 0
(39) Ring oscillation division ratio selection register (RODR)	003716	0 0 0 0 0 0 0 1
(40) MISRG	003816	0016
(41) Watchdog timer control register (WDTCON)	003916	0 0 1 1 1 1 1 1
(42) Interrupt edge selection register (INTEDGE)	003A16	0016
(43) CPU mode register (CPUM)	003B16	1 0 0 0 0 0 0 0
(44) Interrupt request register 1 (IREQ1)	003C16	0016
(45) Interrupt request register 2 (IREQ2)	003D16	0016
(46) Interrupt control register 1 (ICON1)	003E16	0016
(47) Interrupt control register 2 (ICON2)	003F16	0016
(48) Flash memory control register 0 (FMCR0) (Note 3)	0FE016	0 0 0 0 0 0 0 1
(49) Flash memory control register 1 (FMCR1) (Note 3)	0FE116	0 1 0 0 0 0 0 0
(50) Processor status register	(PS)	X X X X X 1 X X
(51) Program counter	(PCH)	Contents of address FFFD16
	(PCL)	Contents of address FFFC16

Notes 1: X : Undefined

2:The content of other registers is undefined when the microcomputer is reset.

The initial values must be surely set before you use it.

3:Only flash memory version has this register.

Fig. 70 Internal status of microcomputer at reset

Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT, and an RC oscillation circuit can be formed by connecting a resistor and a capacitor.

Use the circuit constants in accordance with the resonator manufacturer's recommended values.

(1) Ring oscillator operation

When the MCU operates by the ring oscillator for the main clock, connect XIN pin to VCC through a resistor and leave XOUT pin open.

The clock frequency of the ring oscillator depends on the supply voltage and the operation temperature range.

Be careful that variable frequencies when designing application products.

(2) Ceramic resonator

When the ceramic resonator is used for the main clock, connect the ceramic resonator and the external circuit to pins XIN and XOUT at the shortest distance. A feedback resistor is built in between pins XIN and XOUT.

(3) RC oscillation

When the RC oscillation is used for the main clock, connect the XIN pin and XOUT pin to the external circuit of resistor R and the capacitor C at the shortest distance.

The frequency is affected by a capacitor, a resistor and a micro-computer.

So, set the constants within the range of the frequency limits.

(4) External clock

When the external signal clock is used for the main clock, connect the XIN pin to the clock source and leave XOUT pin open.

Select "0" (ceramic oscillation) to oscillation mode selection bit of CPU mode register (003B16).

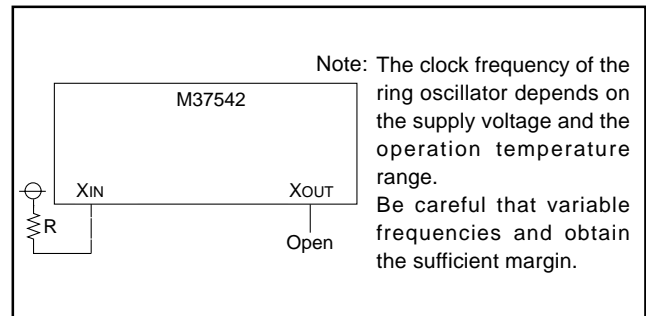


Fig. 71 Processing of XIN and XOUT pins at ring oscillator operation

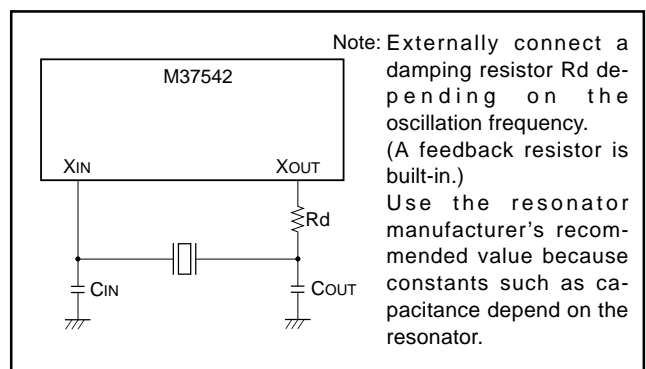


Fig. 72 External circuit of ceramic resonator

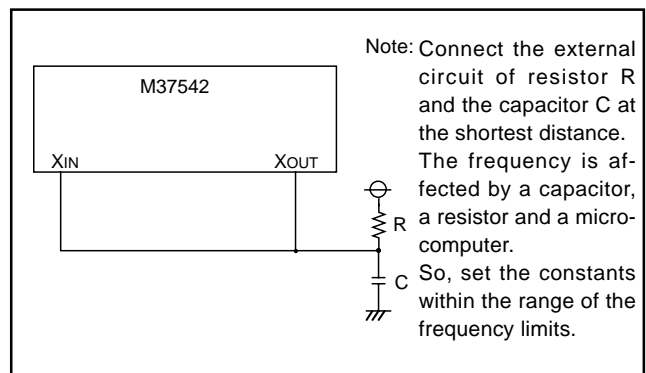


Fig. 73 External circuit of RC oscillation

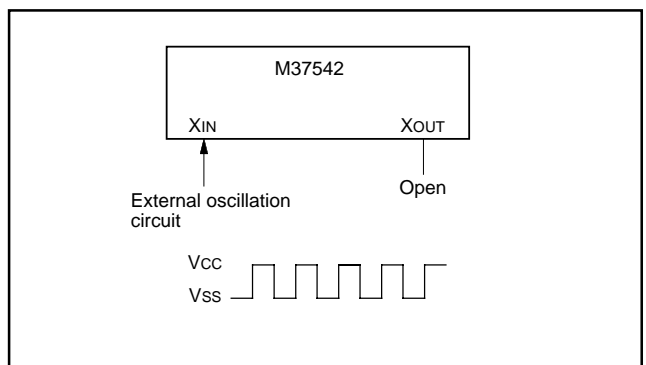


Fig. 74 External clock input circuit

(1) Oscillation control**• Stop mode**

When the STP instruction is executed, the internal clock ϕ stops at an "H" level and the XIN oscillator stops. At this time, timer 1 is set to "0116" and prescaler 1 is set to "FF16" when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 1 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. $f(XIN)/16$ is forcibly connected to the input of prescaler 1. When an external interrupt is accepted, oscillation is restarted but the internal clock ϕ remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock ϕ is supplied. This is because when a ceramic oscillator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an "L" level to the RESET pin while oscillation becomes stable, or set the wait time by ring oscillator operation after system is released from reset until the oscillation is stabilized.

With the FLASH version, the internal power supply circuit is changed to low power consumption mode for consumption current reduction at the time of STP instruction execution.

Although an internal power supply circuit is usually changed to the normal operation mode at the time of the return from an STP instruction, since a certain time is required to start the power supply to FLASH and operation of FLASH to be enabled, set wait time 100 μ s or more with the FLASH version by the oscillation stabilization time set function after release of the STP instruction which used the timer 1.

• Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

■ Notes on Clock Generating Circuit

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 1 after fully appreciating the oscillation stabilization time of the oscillator to be used.

• Switch of ceramic and RC oscillations

After releasing reset the operation starts by starting a built-in ring oscillator. Then, a ceramic oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.

• Double-speed mode

When a ceramic oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

• CPU mode register

Bits 5, 1 and 0 of CPU mode register are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by error-writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. (The emulator MCU "M37542RSS" is excluded.)

Also, when the read-modify-write instructions (SEB, CLB) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

• Clock division ratio, XIN oscillation control, ring oscillator control

The state transition shown in Fig. 79 can be performed by setting the clock division ratio selection bits (bits 7 and 6), XIN oscillation control bit (bit 4), ring oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 79.

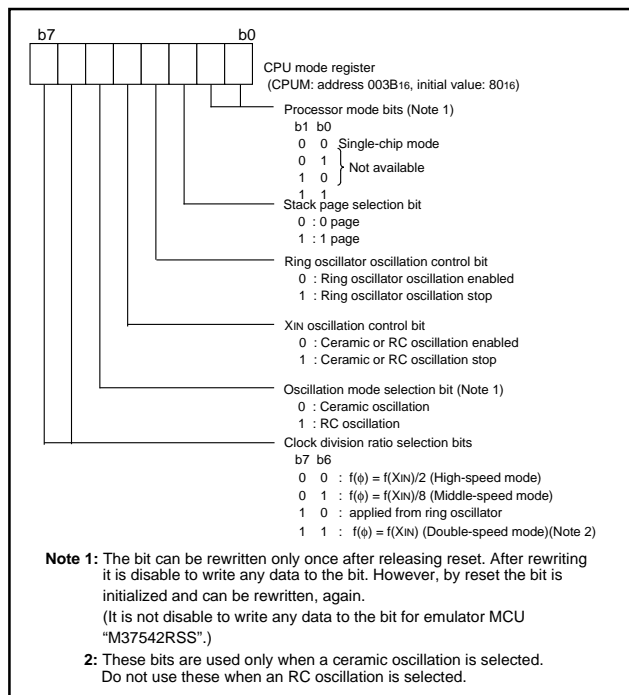


Fig. 75 Structure of CPU mode register

● Ring oscillation division ratio

At ring oscillator mode, division ratio of ring oscillator for CPU clock is selected by setting value of ring oscillation division ratio selection register. The division ratio of ring oscillation for CPU clock is selected from among 1/1, 1/2, 1/8, 1/128. The operation clock for the peripheral function block is not changed by setting value of this register.

■ Notes on Ring Oscillation Division Ratio

- When system is released from reset, ROSC/8 (ring middle-speed mode) is selected for CPU clock.
- When state transition from the ceramic or RC oscillation to ring oscillator, ROSC/8 (ring middle-speed mode) is selected for CPU clock.
- When the MCU operates by ring-oscillator for the main clock without external oscillation circuit, connect XIN pin to VCC through a resistor and leave XOUT pin open.
Set "10010x002" (x = 0 or 1) to CPUM.

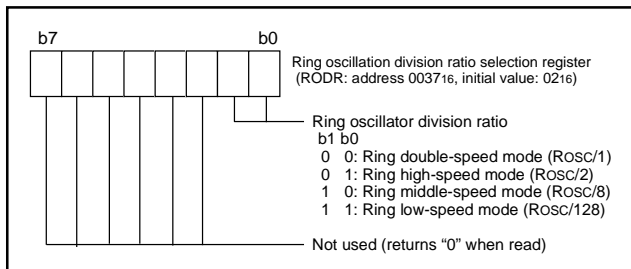
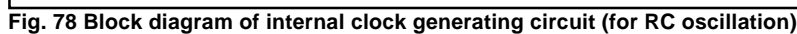


Fig. 76 Structure of ring oscillation division ratio selection register



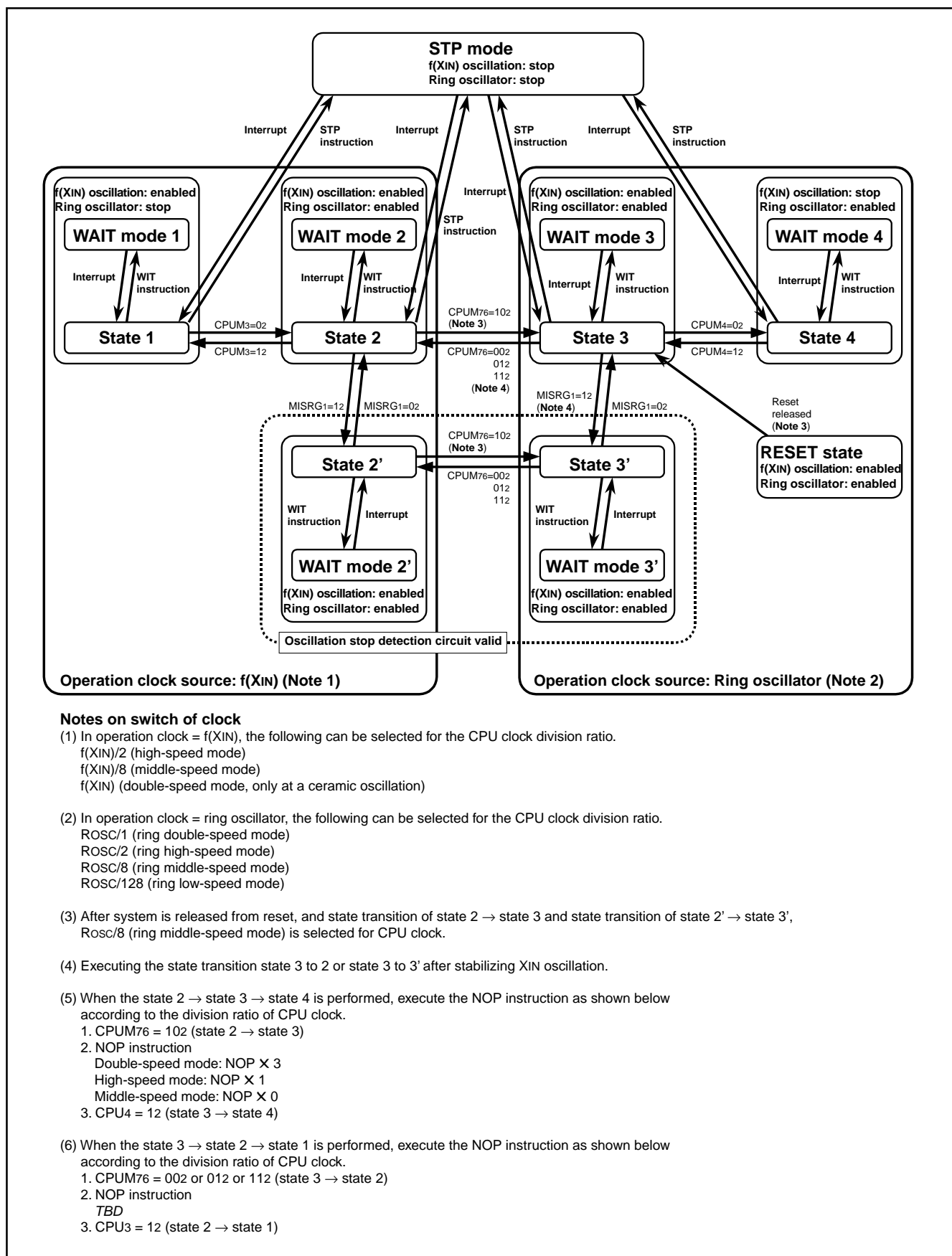


Fig. 79 State transition

● Oscillation stop detection circuit

The oscillation stop detection circuit is used for reset occurrence when a ceramic resonator or RC oscillation circuit stops by disconnection. To use this circuit, set a built-in ring oscillator to be in active.

The oscillation stop detection circuit is in active to set "1" to the ceramic or RC oscillation stop detection function active bit. When the oscillation stop detection circuit is in active, ceramic or RC oscillation is watched by the built-in ring oscillator. When stop of ceramic or RC oscillation is detected, the oscillation stop detection status bit is set to "1". While "1" is set to the oscillation stop reset bit, internal reset occurs when oscillation stop is detected.

The external reset and the oscillation stop reset can be discriminated by reading the oscillation stop detection status bit.

The oscillation stop detection status bit retains "1", not initialized, when the oscillation stop reset occurs. The oscillation stop detection status bit is initialized to "0" when the external reset occurs. Accordingly, reset by oscillation stop can be confirmed by using this bit.

■ Notes on Oscillation Stop Detection Circuit

- Do not execute the transition to "state 2'a" shown in Figure 81 because in this "state 2'a", MCU is stopped without reset even when XIN oscillation is stopped.
- Ceramic or RC oscillation stop detection function active bit is not cleared by the oscillation stop internal reset. Accordingly, the oscillation stop detection circuit is in active when system is released from internal reset cause of oscillation stop detection.
- Oscillation stop detection status bit is initialized by the following operation.
 - External reset
 - Write "0" data to the ceramic or RC oscillation stop detection function active bit.
- The oscillation stop detection circuit is not included in the emulator MCU "M37542RSS".

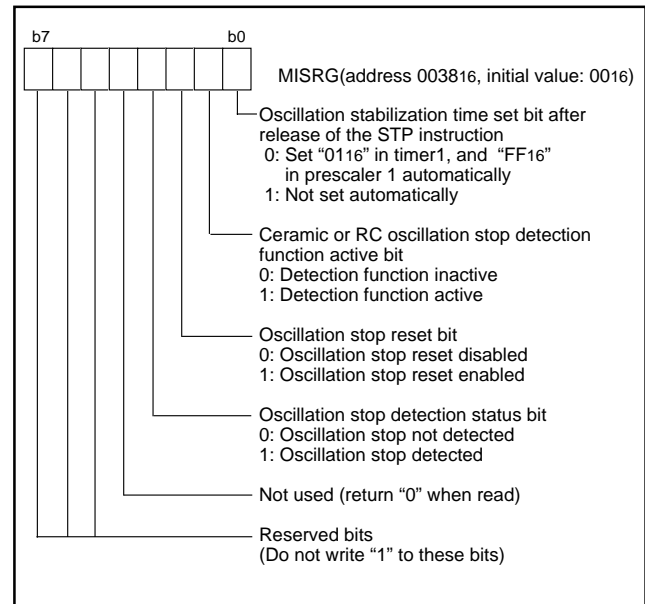


Fig. 80 Structure of MISRG

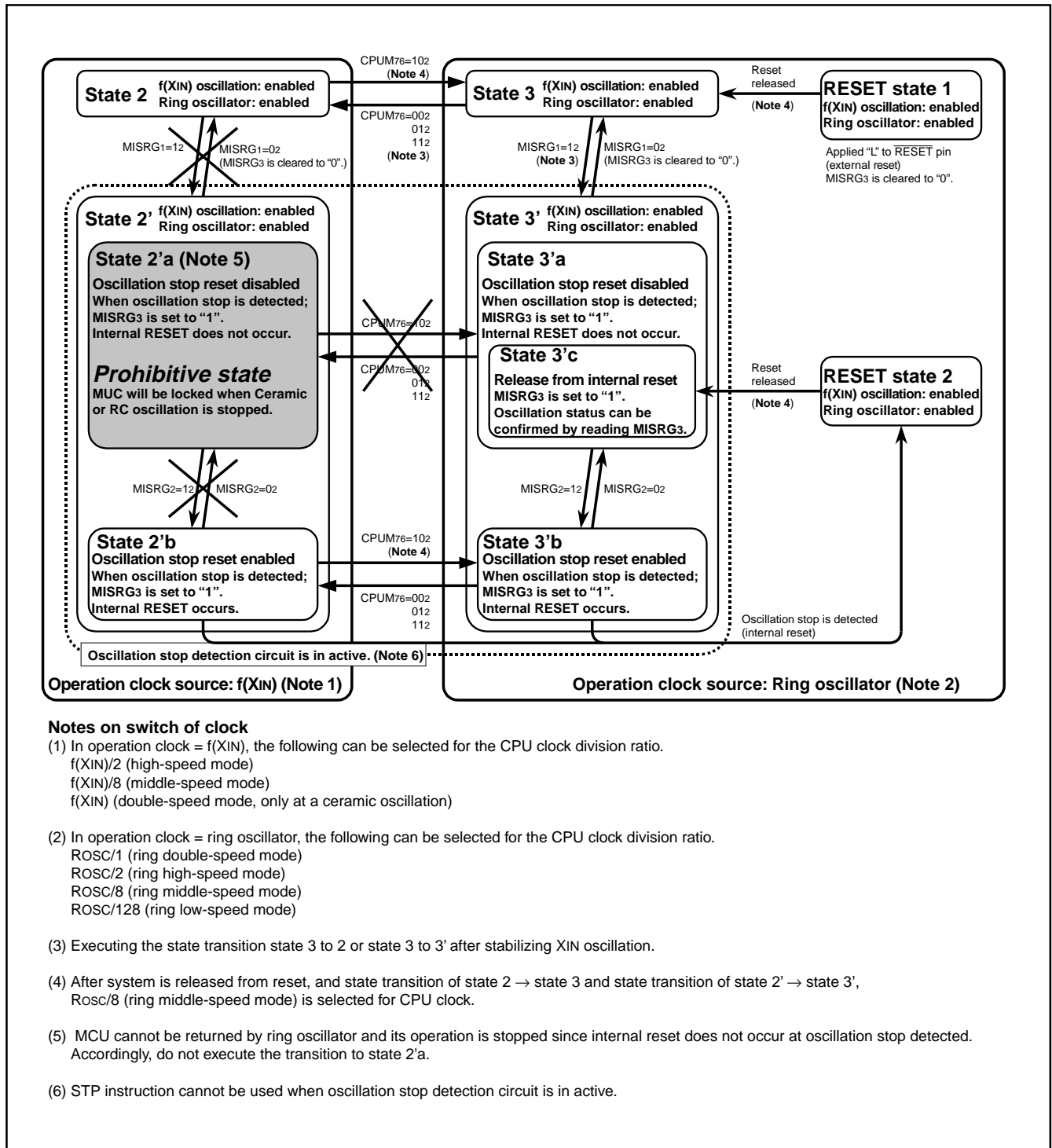


Fig. 81 State transition 2

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is "1". After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

- For calculations in decimal notation, set the decimal mode flag D to "1", then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.
- In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Ports

- The values of the port direction registers cannot be read. That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
- It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.
- For setting direction registers, use the LDM instruction, STA instruction, etc.

A-D Conversion

Do not execute the STP instruction during A-D conversion.

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.

The frequency of the internal clock ϕ is the same as that of the XIN in double-speed mode, twice the XIN cycle in high-speed mode and 8 times the XIN cycle in middle-speed mode.

CPU Mode Register

The oscillation mode selection bit and processor mode bits can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit. (Emulator MCU is excluded.)

When a ceramic oscillation is selected, a double-speed mode of the clock division ratio selection bits can be used. Do not use it when an RC oscillation is selected.

State transition

Do not stop the clock selected as the operation clock because of setting of CM3, 4.

NOTES ON HARDWARE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μ F to 0.1 μ F is recommended.

NOTES ON PERIPHERAL FUNCTIONS

■ Interrupt

(1) When setting the followings, the interrupt request bit may be set to "1".

- When setting external interrupt active edge

Related register:

Interrupt edge selection register (address 003A16)

Timer X mode register (address 002B16)

Capture mode register (address 002016)

When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

- ① Set the corresponding interrupt enable bit to "0" (disabled).
- ② Set the interrupt edge select bit (active edge switch bit, trigger mode bit).
- ③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- ④ Set the corresponding interrupt enable bit to "1" (enabled).

(2) Use a LDM instruction to clear an interrupt discrimination bit.

LDM #0n, \$0Bn

Set the following values to "n"

"0": an interrupt discrimination bit to clear

"1": other interrupt discrimination bits

Ex.) When a key-on wakeup interrupt discrimination bit is cleared;

LDM #00001110B and \$0B.

■ Timers

- When n (0 to 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.
- When a count source of timer X, timer Y or timer Z is switched, stop a count of timer X.

■ Timer X

(1) CNTR0 interrupt active edge selection-1

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

When this bit is "0", the CNTR0 interrupt request bit is set to "1" at the falling edge of CNTR0 pin input signal. When this bit is "1", the CNTR0 interrupt request bit is set to "1" at the rising edge of CNTR0 pin input signal.

(2) CNTR0 interrupt active edge selection-2

According to the setting value of CNTR0 active edge switch bit, the interrupt request bit may be set to "1".

When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

- ① Set the corresponding interrupt enable bit to "0" (disabled).
- ② Set the active edge switch bit.
- ③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- ④ Set the corresponding interrupt enable bit to "1" (enabled).

■ Notes on Timer A, B

(1) Setting of timer value

When "1: Write to only latch" is set to the timer A (B) write control bit, written data to timer register is set to only latch even if timer is stopped. Accordingly, in order to set the initial value for timer when it is stopped, set "0: Write to latch and timer simultaneously" to timer A (B) write control bit.

(2) Read/write of timer A

Stop timer A to read/write its data when the system is in the following state;

- CPU operation clock source: XIN oscillation
- Timer A count source: Ring oscillator output

(3) Read/write of timer B

Stop timer B to read/write its data when the system is in the following state;

- CPU operation clock source: XIN oscillation
- Timer B count source: Timer A underflow
- Timer A count source: Ring oscillator output

■ Notes on Output Compare

- When the selected source timer of each compare channel is stopped, written data to compare register is loaded to the compare latch simultaneously.
- Do not write the same data to both of compare latch x0 and x1.
- When setting value of the compare latch is larger than timer setting value, compare match signal is not generated. Accordingly, the output waveform is fixed to "L" or "H" level.
However, when setting value of another compare latch is smaller than timer setting value, this compare match signal is generated. Accordingly, compare match interrupt occurs.
- When the compare x trigger enable bit is cleared to "0" (disabled), the match trigger to the waveform output circuit is disabled, and the output waveform can be fixed to "L" or "H" level.
However, in this case, the compare match signal is generated. Accordingly, compare match interrupt occurs.

■ Notes on Input Capture

- If the capture trigger is input while the capture register (low-order and high-order) is in read, captured value is changed between high-order reading and low-order reading. Accordingly, some countermeasure by software is recommended, for example comparing the values that twice of read.
- When the ring-oscillator is selected for Timer A count source, Timer A cannot be used for the capture source timer.
Timer B cannot be used for the capture source timer when the system is in the following state;
 - CPU operation clock source: XIN oscillation
 - Timer B count source: Timer A underflow
 - Timer A count source: Ring oscillator output
- When writing "1" to capture latch x0 (x1) software trigger bit of capture latch x0 and x1 at the same time, or external trigger and software trigger occur simultaneously, the set value of capture x status bit is undefined.
- When setting the interrupt active edge selection bit and noise filter clock selection bit of external interrupt CAP0, CAP1, the interrupt request bit may be set to "1".
When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.
 - ① Set the corresponding interrupt enable bit to "0" (disabled).
 - ② Set the interrupt edge selection bit or noise filter clock selection bit.
 - ③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
 - ④ Set the corresponding interrupt enable bit to "1" (enabled).
- The capture interrupt cannot be used as the interrupt for return from stop mode. Even when the valid edge of the capture interrupt is input at stop mode, system retains the stop mode. Then, system returns from stop mode by other external interrupts, the capture interrupt is accepted.
In this case, after system returns from stop mode, the interrupt request bit of the corresponding capture interrupt is set to "1".

■ Notes on Serial I/O1

• Serial I/O interrupt

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

- ① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
- ② Set the transmit enable bit to "1".
- ③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- ⑤ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O1 is enabled.

The functions of P12 and P13 are switched with the setting values of a serial I/O1 mode selection bit and a serial I/O1 synchronous clock selection bit as follows.

(1) Serial I/O1 mode selection bit → "1" :

Clock synchronous type serial I/O is selected.

Setup of a serial I/O1 synchronous clock selection bit

"0" : P12 pin turns into an output pin of a synchronous clock.

"1" : P12 pin turns into an input pin of a synchronous clock.

Setup of a $\overline{\text{SRDY}}_1$ output enable bit (SRDY)

"0" : P13 pin can be used as a normal I/O pin.

"1" : P13 pin turns into a $\overline{\text{SRDY}}_1$ output pin.

(2) Serial I/O1 mode selection bit → "0" :

Clock asynchronous (UART) type serial I/O is selected.

Setup of a serial I/O1 synchronous clock selection bit

"0" : P12 pin can be used as a normal I/O pin.

"1" : P12 pin turns into an input pin of an external clock.

When clock asynchronous (UART) type serial I/O is selected, it is P13 pin. It can be used as a normal I/O pin.

• Bus collision detection

Bus collision detection can be used when SIO1 is operating at full-duplex communication. When SIO1 is operating at half-duplex communication, set bus collision detection interrupt to be disabled.

■ Notes on Serial I/O2

• Serial I/O interrupt

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

- ① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
- ② Set the transmit enable bit to "1".
- ③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- ⑤ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O2 is enabled.

The functions of P06 and P07 are switched with the setting values of a serial I/O2 mode selection bit and a serial I/O2 synchronous clock selection bit as follows.

(1) Serial I/O2 mode selection bit → "1" :

Clock synchronous type serial I/O is selected.

Setup of a serial I/O2 synchronous clock selection bit

"0" : P06 pin turns into an output pin of a synchronous clock.

"1" : P06 pin turns into an input pin of a synchronous clock.

Setup of a $\overline{\text{SRDY}}_2$ output enable bit (SRDY)

"0" : P07 pin can be used as a normal I/O pin.

"1" : P07 pin turns into a $\overline{\text{SRDY}}_2$ output pin.

(2) Serial I/O2 mode selection bit → "0" :

Clock asynchronous (UART) type serial I/O is selected.

Setup of a serial I/O2 synchronous clock selection bit

"0" : P06 pin can be used as a normal I/O pin.

"1" : P06 pin turns into an input pin of an external clock.

When clock asynchronous (UART) type serial I/O is selected, it is P07 pin. It can be used as a normal I/O pin.

■ A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that $f(\text{XIN})$ is 500kHz or more during A-D conversion.

■ Notes on Clock Generating Circuit

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 1 after fully appreciating the oscillation stabilization time of the oscillator to be used.

- Switch of ceramic and RC oscillations

After releasing reset the operation starts by starting a built-in ring oscillator. Then, a ceramic oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.

- Double-speed mode

When a ceramic oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

- CPU mode register

Bits 5, 1 and 0 of CPU mode register are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by error-writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. (The emulator MCU "M37542RSS" is excluded.)

Also, when the read-modify-write instructions (SEB, CLB) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

- Clock division ratio, XIN oscillation control, ring oscillator control

The state transition shown in Fig. 79 can be performed by setting the clock division ratio selection bits (bits 7 and 6), XIN oscillation control bit (bit 4), ring oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 79.

■ Notes on Ring Oscillation Division Ratio

- When system is released from reset, ROSC/8 (ring middle-speed mode) is selected for CPU clock.
- When state transition from the ceramic or RC oscillation to ring oscillator, ROSC/8 (ring middle-speed mode) is selected for CPU clock.
- When the MCU operates by ring-oscillator for the main clock without external oscillation circuit, connect XIN pin to VCC through a resistor and leave XOUT pin open.
Set "10010x002" (x = 0 or 1) to CPUM.

■ Notes on Oscillation Stop Detection Circuit

- When the oscillation stop reset bit is set to "0", internal reset does not occur. If the ceramic or RC oscillation is selected for the CPU clock, MCU will be locked when the ceramic or RC oscillation is stopped. So when the ceramic or RC oscillation is selected for the main clock, set the oscillation stop reset bit to "1". (State 2'a of Fig. 81)
- Ceramic or RC oscillation stop detection function active bit is not cleared by the oscillation stop internal reset. Accordingly, the oscillation stop detection circuit is in active when system is released from internal reset cause of oscillation stop detection.
- Oscillation stop detection status bit is initialized by the following operation.
 - (1) External reset
 - (2) Write "0" data to the ceramic or RC oscillation stop detection function active bit.
- The oscillation stop detection circuit is not included in the emulator MCU "M37542RSS".

■ Notes on CPU Rewrite Mode

Take the notes described below when rewriting the flash memory in CPU rewrite mode.

●Operation speed

During CPU rewrite mode, set the system clock ϕ to 4.0 MHz or less using the clock division ratio selection bits (bits 6 and 7 of address 003B16).

●Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during CPU rewrite mode.

●Interrupts inhibited against use

The interrupts cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory.

●Watchdog timer

If the watchdog timer has been already activated, internal reset due to an underflow will not occur because the watchdog timer is surely cleared during program or erase.

●Reset

Reset is always valid. The MCU is activated using the boot mode at release of reset in the condition of CNVss = "H", so that the program will begin at the address which is stored in addresses FFFC16 and FFFD16 of the boot ROM area.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- 1.Mask ROM Order Confirmation Form *
- 2.Mark Specification Form *
- 3.Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

For the mask ROM confirmation and the mark specifications, refer to the "Renesas Technology Corp." Homepage (<http://www.renesas.com/en/rom>).

FLASH MEMORY MODE

The 7542 group's flash memory version has the flash memory that can be rewritten with a single power source.

For this flash memory, three flash memory modes are available in which to read, program, and erase: the parallel I/O and standard serial I/O modes in which the flash memory can be manipulated using a programmer and the CPU rewrite mode in which the flash memory can be manipulated by the Central Processing Unit (CPU).

● Summary

Table 7 lists the summary of the 7542 Group (flash memory version).

This flash memory version has some blocks on the flash memory as shown in Figure 82 and each block can be erased.

In addition to the ordinary User ROM area to store the MCU operation control program, the flash memory has a Boot ROM area that is used to store a program to control rewriting in CPU rewrite and standard serial I/O modes. This Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. However, the user can write a rewrite control program in this area that suits the user's application system. This Boot ROM area can be rewritten in only parallel I/O mode.

Table 7 Summary of 7542 group's flash memory version

Item		Specifications
Power source voltage (Vcc)		VCC = 2.7 to 5.5 V
Program/Erase VPP voltage (VPP)		VCC = 2.7 to 5.5 V
Flash memory mode		3 modes; Parallel I/O mode, Standard serial I/O mode, CPU rewrite mode
Erase block division	User ROM area/Data ROM area	Refer to Fig. 82.
	Boot ROM area (Note)	Not divided (4K bytes)
Program method		In units of bytes
Erase method		Block erase
Program/Erase control method		Program/Erase control by software command
Number of commands		5 commands
Number of program/Erase times		TBD
ROM code protection		Available in parallel I/O mode and standard serial I/O mode

Note: The Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory.
This Boot ROM area can be erased and written in only parallel I/O mode.

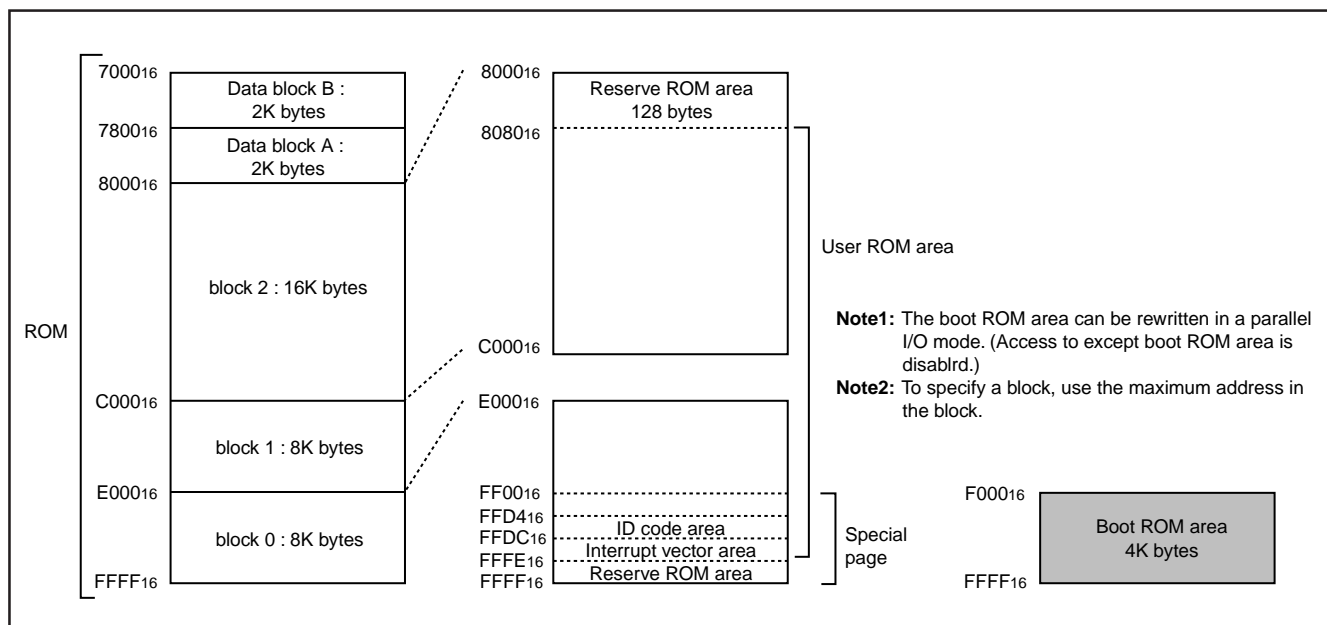


Fig. 82 Block diagram of built-in flash memory

● Boot Mode

The control program for CPU rewrite mode must be written into the User ROM or Boot ROM area in parallel I/O mode beforehand. (If the control program is written into the Boot ROM area, the standard serial I/O mode becomes unusable.)

See Figure 82 for details about the Boot ROM area.

Normal microcomputer mode is entered when the microcomputer is reset with pulling CNVss pin low. In this case, the CPU starts operating using the control program in the User ROM area.

When the microcomputer is reset and the CNVss pin high after pulling the P37(RP) pin low, P32(CE) pin high, P06/SCLK pin low and P05/TxD2 pin high, the CPU starts operating (start address of program is stored into addresses FFFC₁₆ and FFFD₁₆) using the control program in the Boot ROM area. This mode is called the "Boot mode". Also, User ROM area can be rewritten using the control program in the Boot ROM area.

● Block Address

Block addresses refer to the maximum address of each block. These addresses are used in the block erase command.

● CPU Rewrite Mode

In CPU rewrite mode, the internal flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU).

In CPU rewrite mode, only the User ROM area shown in Figure 82 can be rewritten; the Boot ROM area cannot be rewritten. Make sure the program and block erase commands are issued for only the User ROM area and each block area.

The control program for CPU rewrite mode can be stored in either User ROM or Boot ROM area. In the CPU rewrite mode, because the flash memory cannot be read from the CPU, the rewrite control program must be transferred to internal RAM area before it can be executed.

• Outline Performance

CPU rewrite mode is usable in the single-chip or Boot mode. The only User ROM area can be rewritten.

In CPU rewrite mode, the CPU erases, programs and reads the internal flash memory as instructed by software commands. This rewrite control program must be transferred to internal RAM area before it can be executed.

The MCU enters CPU rewrite mode by setting "1" to the CPU rewrite mode select bit (bit 1 of address 0FE016). Then, software commands can be accepted.

Use software commands to control program and erase operations. Whether a program or erase operation has terminated normally or in error can be verified by reading the status register.

Figure 83 shows the flash memory control register 0.

Bit 0 of the flash memory control register 0 is the RY/BY status flag used exclusively to read the operating status of the flash memory. During programming and erase operations, it is "0" (busy). Otherwise, it is "1" (ready).

Bit 1 of the flash memory control register 0 is the CPU rewrite mode select bit. When this bit is set to "1", the MCU enters CPU rewrite mode. And then, software commands can be accepted. In CPU rewrite mode, the CPU becomes unable to access the internal flash memory directly. Therefore, use the control program in the internal RAM for write to bit 1. To set this bit 1 to "1", it is necessary to write "0" and then write "1" in succession to bit 1. The bit can be set to "0" by only writing "0".

Bit 2 of the flash memory control register 0 is the 8KB user block E/W mode disable bit. When this bit is set to "0", CPU rewriting to block 0 and block 1 of FLASH is disabled.

Bit 3 of the flash memory control register 0 is the flash memory reset bit used to reset the control circuit of internal flash memory. This bit is used when exiting CPU rewrite mode and when flash memory access has failed. When the CPU rewrite mode select bit is "1", setting "1" for this bit resets the control circuit. To release the reset, it is necessary to set this bit to "0".

Bit 5 of the flash memory control register 0 is the User ROM area select bit and is valid only in the boot mode. Setting this bit to "1" in the boot mode switches an accessible area from the boot ROM area to the user ROM area. To use the CPU rewrite mode in the boot mode, set this bit to "1". Note that when the microcomputer is booted up in the user ROM area, only the user ROM area is accessible and bit 5 is invalid; on the other hand, when the microcomputer is in the boot mode, bit 5 is valid independent of the CPU rewrite mode. To rewrite bit 5, execute the user-original reprogramming control software transferred to the internal RAM in advance.

Bit 6 of the flash memory control register 0 is the program status flag. This bit is set to "1" when writing to flash memory is failed. When program error occurs, the block cannot be used.

Bit 7 of the flash memory control register 0 is the erase status flag. This bit is set to "1" when erasing flash memory is failed. When erase error occurs, the block cannot be used.

Figure 84 shows the flash memory control register 1.

Bit 0 of the flash memory control register 1 is the Erase suspend enable bit. By setting this bit to "1", the erase suspend mode to suspend erase processing temporarily when block erase command is executed can be used. In order to set this bit to "1", writing "0" and "1" in succession to bit 0. In order to set this bit to "0", write "0" only to bit 0.

Bit 1 of the flash memory control register 1 is the erase suspend request bit. By setting this bit to "1" when erase suspend enable bit is "1", the erase processing is suspended.

Bit 6 of the flash memory control register 1 is the erase suspend flag. This bit is cleared to "0" at the flash erasing.

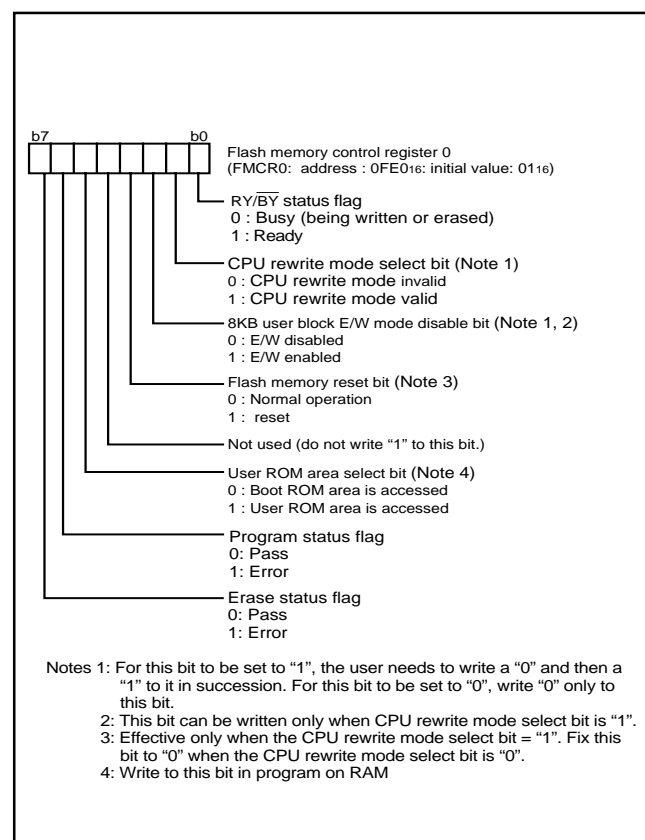


Fig. 83 Structure of flash memory control register 0

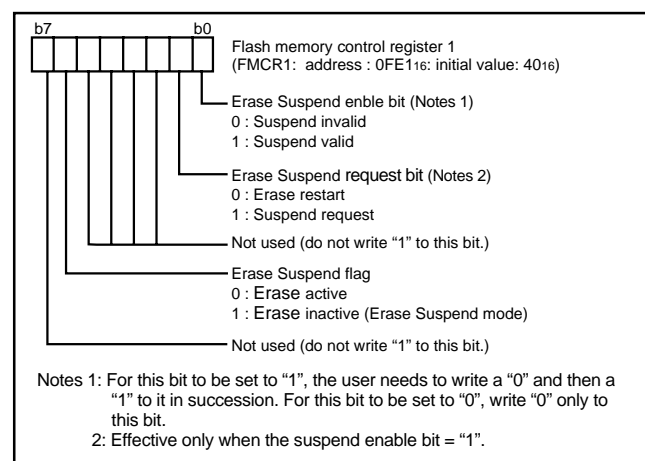


Fig. 84 Structure of flash memory control register 1

Figure 85 shows a flowchart for setting/releasing CPU rewrite mode.

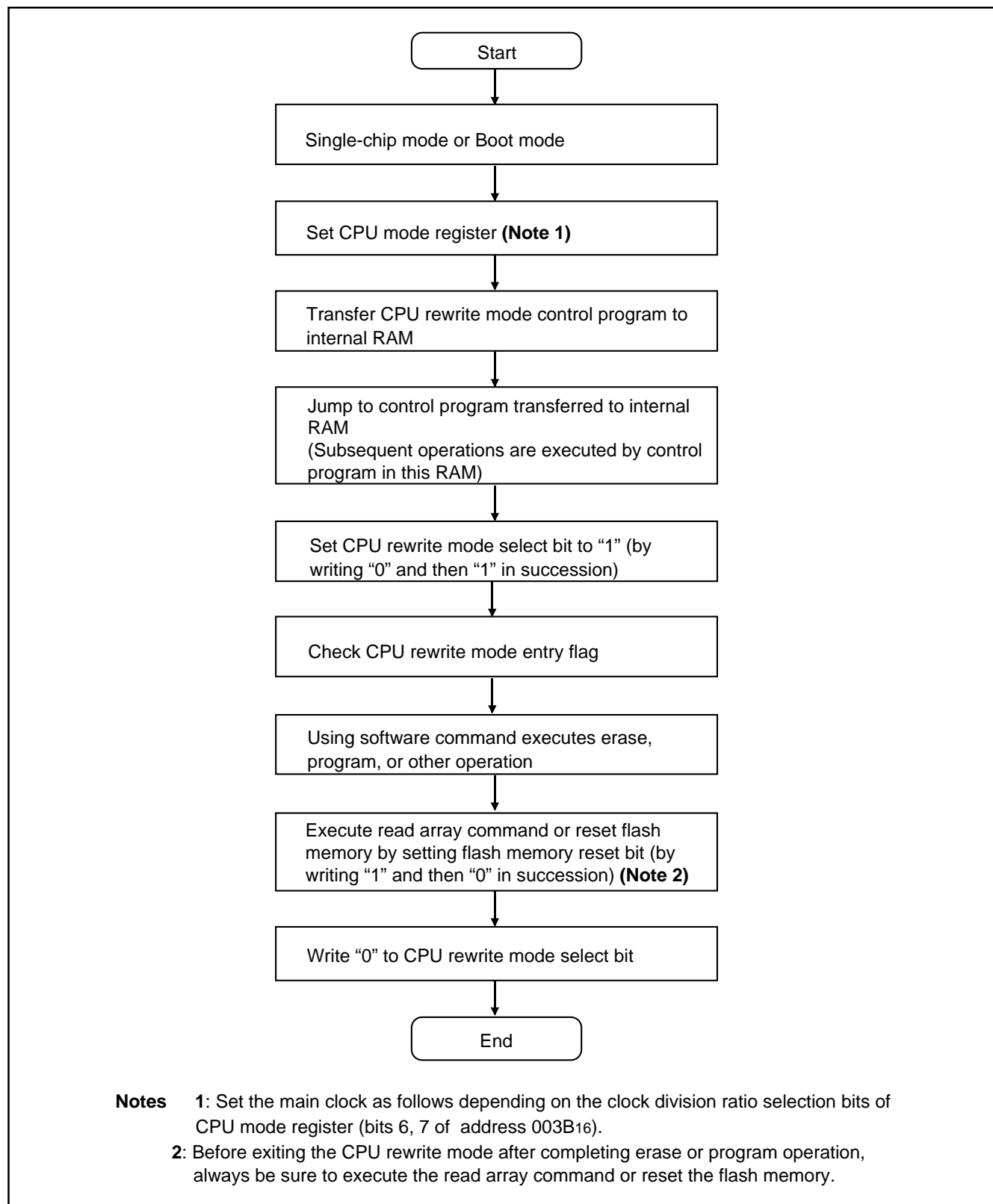


Fig. 85 CPU rewrite mode set/release flowchart

■ Notes on CPU Rewrite Mode

Take the notes described below when rewriting the flash memory in CPU rewrite mode.

●Operation speed

During CPU rewrite mode, set the system clock ϕ to 4.0 MHz or less using the clock division ratio selection bits (bits 6 and 7 of address 003B16).

●Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during CPU rewrite mode.

●Interrupts inhibited against use

The interrupts cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory.

●Watchdog timer

If the watchdog timer has been already activated, internal reset due to an underflow will not occur because the watchdog timer is surely cleared during program or erase.

●Reset

Reset is always valid. The MCU is activated using the boot mode at release of reset in the condition of CNVss = "H", so that the program will begin at the address which is stored in addresses FFFC16 and FFFD16 of the boot ROM area.

● Software Commands

Table 8 lists the software commands.

After setting the CPU rewrite mode select bit to "1", execute a software command to specify an erase or program operation.

Each software command is explained below.

• Read Array Command (FF₁₆)

The read array mode is entered by writing the command code "FF₁₆" in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the contents of the specified address are read out at the data bus (D₀ to D₇).

The read array mode is retained until another command is written.

• Read Status Register Command (70₁₆)

When the command code "70₁₆" is written in the first bus cycle, the contents of the status register are read out at the data bus (D₀ to D₇) by a read in the second bus cycle.

The status register is explained in the next section.

• Clear Status Register Command (50₁₆)

This command is used to clear the bits SR4 and SR5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code "50₁₆" in the first bus cycle.

• Program Command (40₁₆)

Program operation starts when the command code "40₁₆" is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, program operation (data programming and verification) will start.

Whether the write operation is completed can be confirmed by read status register or the RY/BY status flag. When the program starts, the read status register mode is entered automatically and the contents of the status register is read at the data bus (D₀ to D₇). The status register bit 7 (SR7) is set to "0" at the same time the write operation starts and is returned to "1" upon completion of the write operation. In this case, the read status register mode remains active until the read array command (FF₁₆) is written.

The RY/BY status flag of the flash memory control register is "0" during write operation and "1" when the write operation is completed as is the status register bit 7.

At program end, program results can be checked by reading the status register.

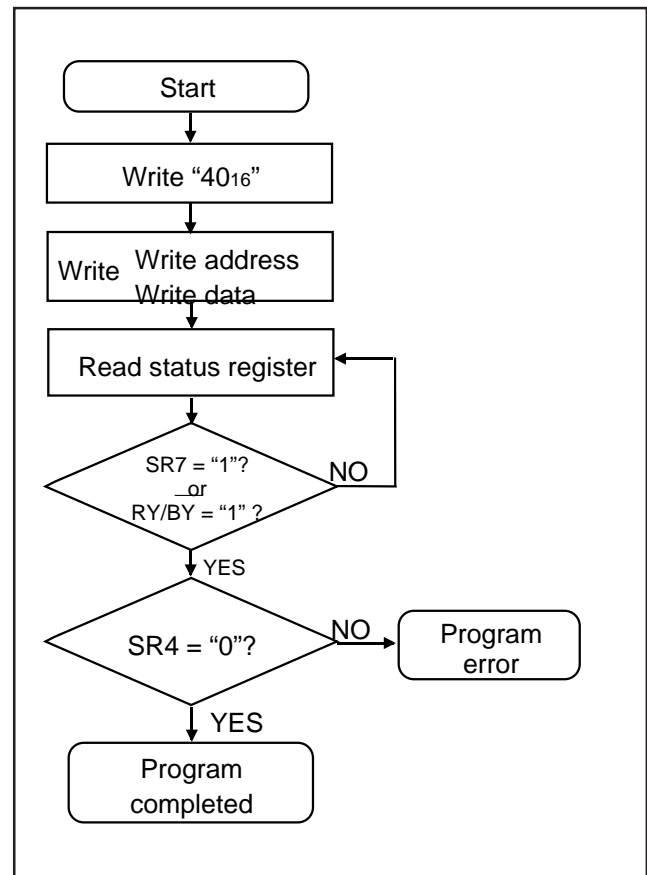


Fig. 86 Program flowchart

Table 8 List of software commands (CPU rewrite mode)

Command	Cycle number	First bus cycle			Second bus cycle		
		Mode	Address	Data (D ₀ to D ₇)	Mode	Address	Data (D ₀ to D ₇)
Read array	1	Write	X (Note 4)	FF ₁₆			
Read status register	2	Write	X	70 ₁₆	Read	X	SRD (Note 1)
Clear status register	1	Write	X	50 ₁₆			
Program	2	Write	X	40 ₁₆	Write	WA (Note 2)	WD (Note 2)
Block erase	2	Write	X	20 ₁₆	Write	BA (Note 3)	D0 ₁₆

Notes 1: SRD = Status Register Data

2: WA = Write Address, WD = Write Data

3: BA = Block Address to be erased (Input the maximum address of each block.)

4: X denotes a given address in the User ROM area.

• Block Erase Command (20₁₆/D0₁₆)

By writing the command code "20₁₆" in the first bus cycle and the confirmation command code "D0₁₆" and the block address in the second bus cycle that follows, the block erase (erase and erase verify) operation starts for the block address of the flash memory to be specified.

Whether the block erase operation is completed can be confirmed by read status register or the RY/ $\overline{\text{BY}}$ status flag of flash memory control register. At the same time the block erase operation starts, the read status register mode is automatically entered, so that the contents of the status register can be read out. The status register bit 7 (SR7) is set to "0" at the same time the block erase operation starts and is returned to "1" upon completion of the block erase operation. In this case, the read status register mode remains active until the read array command (FF₁₆) is written.

The RY/ $\overline{\text{BY}}$ status flag is "0" during block erase operation and "1" when the block erase operation is completed as is the status register bit 7.

After the block erase ends, erase results can be checked by reading the status register. For details, refer to the section where the status register is detailed.

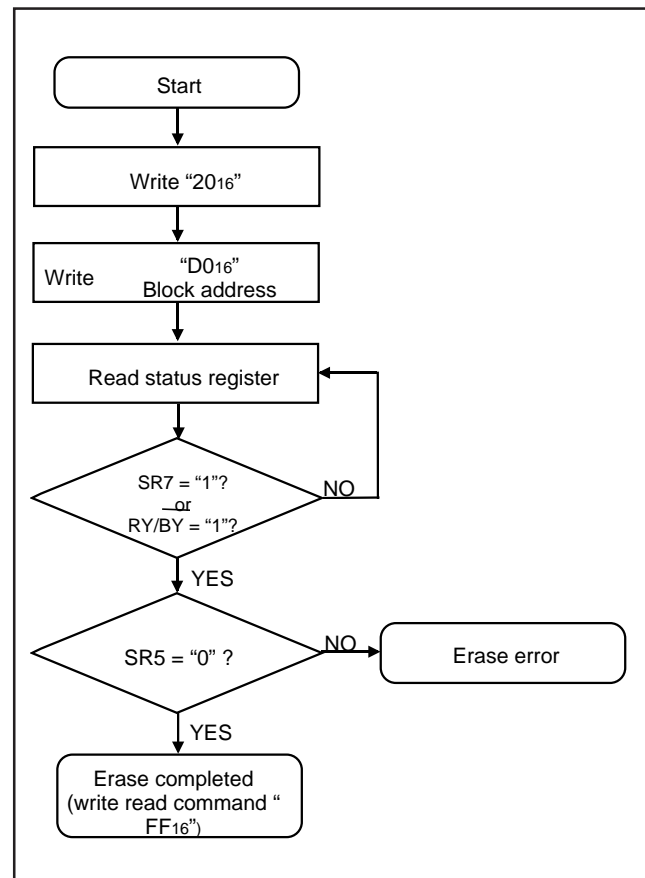


Fig. 87 Erase flowchart

● Status Register

The status register shows the operating status of the flash memory and whether erase operations and programs ended successfully or in error. It can be read in the following ways:

- (1) By reading an arbitrary address from the User ROM area after writing the read status register command (70₁₆)
- (2) By reading an arbitrary address from the User ROM area in the period from when the program starts or erase operation starts to when the read array command (FF₁₆) is input.

Also, the status register can be cleared by writing the clear status register command (50₁₆).

After reset, the status register is set to "80₁₆".

Table 9 shows the status register. Each bit in this register is explained below.

•Sequencer status (SR7)

The sequencer status indicates the operating status of the flash memory. This bit is set to "0" (busy) during write or erase operation and is set to "1" when these operations ends.

After power-on, the sequencer status is set to "1" (ready).

•Erase status (SR5)

The erase status indicates the operating status of erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is reset to "0".

•Program status (SR4)

The program status indicates the operating status of write operation. When a write error occurs, it is set to "1".

The program status is reset to "0" when it is cleared.

If "1" is written for any of the SR5 and SR4 bits, the read array, program, and block erase commands are not accepted. Before executing these commands, execute the clear status register command (50₁₆) and clear the status register.

Also, if any commands are not correct, both SR5 and SR4 are set to "1".

Table 9 Definition of each bit in status register

Each bit of SRD bits	Status name	Definition	
		"1"	"0"
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved	-	-
SR5 (bit5)	Erase status	Terminated in error	Terminated normally
SR4 (bit4)	Program status	Terminated in error	Terminated normally
SR3 (bit3)	Reserved	-	-
SR2 (bit2)	Reserved	-	-
SR1 (bit1)	Reserved	-	-
SR0 (bit0)	Reserved	-	-

● Full Status Check

By performing full status check, it is possible to know the execution results of erase and program operations. Figure 88 shows a full status check flowchart and the action to be taken when each error occurs.

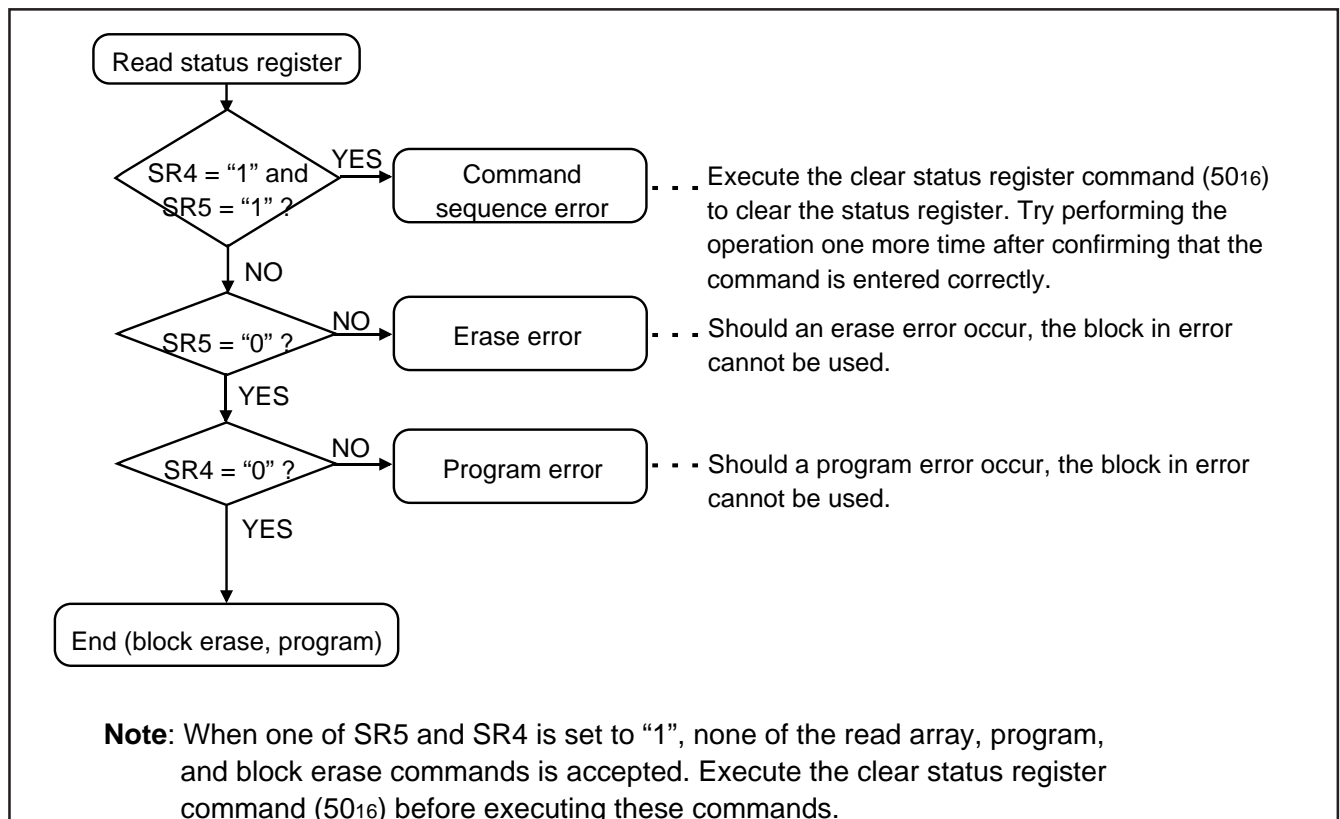


Fig. 88 Full status check flowchart and remedial procedure for errors

● Functions To Inhibit Rewriting Flash Memory Version

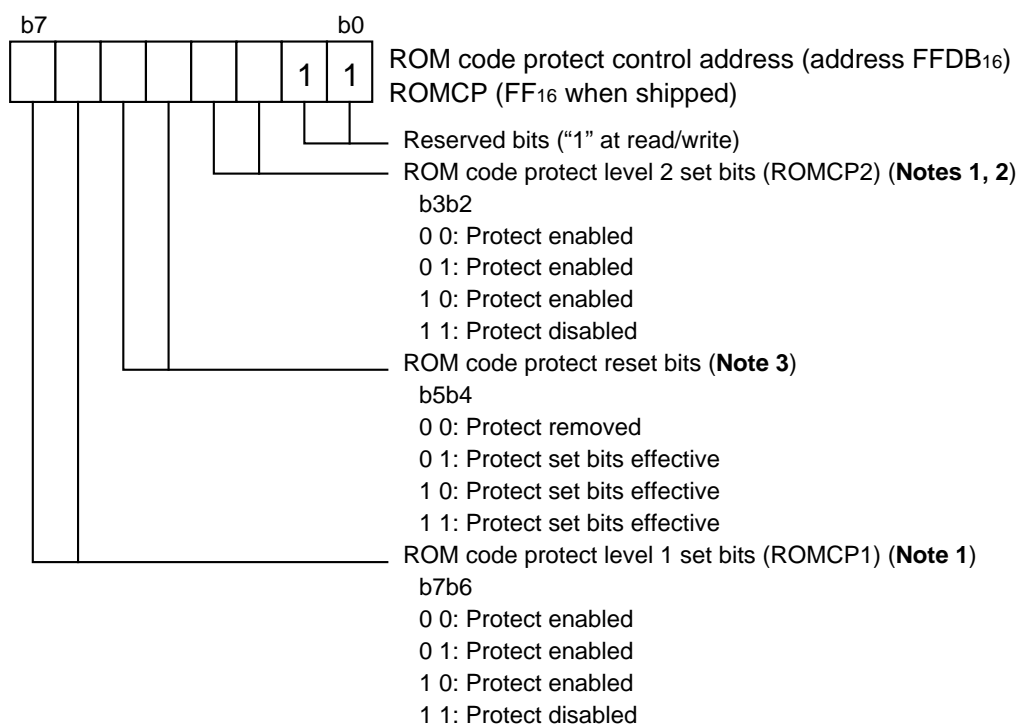
To prevent the contents of internal flash memory from being read out or rewritten easily, this MCU incorporates a ROM code protect function for use in parallel I/O mode and an ID code check function for use in standard serial I/O mode.

(1) ROM Code Protect Function

The ROM code protect function is the function to inhibit reading out or modifying the contents of internal flash memory by using the ROM code protect control address (address FFDB₁₆) in parallel I/O mode. Figure 89 shows the ROM code protect control address (address FFDB₁₆). (This address exists in the User ROM area.)

If one or both of the pair of ROM code protect bits is set to "0", the ROM code protect is turned on, so that the contents of internal flash memory are protected against readout and modification. The ROM code protect is implemented in two levels. If level 2 is selected, the flash memory is protected even against readout by a shipment inspection LSI tester, etc. When an attempt is made to select both level 1 and level 2, level 2 is selected by default.

If both of the two ROM code protect reset bits are set to "00", the ROM code protect is turned off, so that the contents of internal flash memory can be readout or modified. Once the ROM code protect is turned on, the contents of the ROM code protect reset bits cannot be modified in parallel I/O mode. Use the serial I/O or CPU rewrite mode to rewrite the contents of the ROM code protect reset bits.



- Notes**
- 1: When ROM code protect is turned on, the internal flash memory is protected against readout or modification in parallel I/O mode.
 - 2: When ROM code protect level 2 is turned on, ROM code readout by a shipment inspection LSI tester, etc. also is inhibited.
 - 3: The ROM code protect reset bits can be used to turn off ROM code protect level 1 and ROM code protect level 2. However, since these bits cannot be modified in parallel I/O mode, they need to be rewritten in serial I/O mode or CPU rewrite mode.

Fig. 89 Structure of ROM code protect control address

(2) ID Code Check Function

Use this function in standard serial I/O mode. When the contents of the flash memory are not blank, the ID code sent from the programmer is compared with the ID code written in the flash memory to see if they match. If the ID codes do not match, the commands sent from the programmer are not accepted. The ID code consists of 8-bit data, and its areas are FFD4₁₆ to FFDA₁₆. Write a program which has had the ID code preset at these addresses to the flash memory.

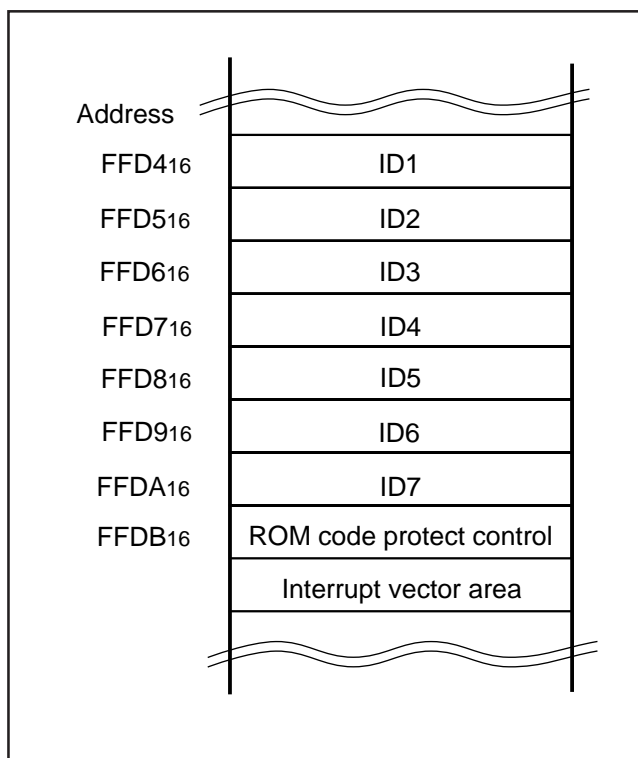


Fig. 90 ID code store addresses

● Parallel I/O Mode

The parallel I/O mode is used to input/output software commands, address and data in parallel for operation (read, program and erase) to internal flash memory.

Use the external device (writer) only for 7542 Group (flash memory version). For details, refer to the user's manual of each writer manufacturer.

• User ROM and Boot ROM Areas

In parallel I/O mode, the User ROM and Boot ROM areas shown in Figure 82 can be rewritten. Both areas of flash memory can be operated on in the same way.

The Boot ROM area is 4 Kbytes in size and located at addresses F000₁₆ through FFFF₁₆. Make sure program and block erase operations are always performed within this address range. (Access to any location outside this address range is prohibited.)

In the Boot ROM area, an erase block operation is applied to only one 4 Kbyte block. The boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. Therefore, using the MCU in standard serial I/O mode, do not rewrite to the Boot ROM area.

● Standard serial I/O Mode

The standard serial I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is clock synchronized serial. This mode requires a purpose-specific peripheral unit.

The standard serial I/O mode is different from the parallel I/O mode in that the CPU controls flash memory rewrite (uses the CPU rewrite mode), rewrite data input and so forth. The standard serial I/O mode is started when the microcomputer is reset and the CNVss pin high after pulling the P37(RP) pin low, P32(CE) pin high, P06/SCLK2 pin low and P05/TxD2 pin high. (In the ordinary microcomputer mode, set CNVss pin to "L" level.)

This control program is written in the Boot ROM area when the product is shipped from Renesas. Accordingly, make note of the fact that the standard serial I/O mode cannot be used if the Boot ROM area is rewritten in parallel I/O mode. Figures 91 to 96 show the pin connections for the standard serial I/O mode.

In standard serial I/O mode, serial data I/O uses the four UART2 pins SCLK2, RxD2, TxD2 and $\overline{\text{SRDY2}}$ (BUSY). The SCLK2 pin is the transfer clock input pin through which an external transfer clock is input. The TxD2 pin is for CMOS output. The $\overline{\text{SRDY2}}$ (BUSY) pin outputs "L" level when ready for reception and "H" level when reception starts.

Serial data I/O is transferred serially in 8-bit units.

In standard serial I/O mode, only the User ROM area shown in Figure 82 can be rewritten. The Boot ROM area cannot be written. In standard serial I/O mode, a 7-byte ID code is used. When there is data in the flash memory, commands sent from the peripheral unit (programmer) are not accepted unless the ID code matches.

Outline Performance (Standard Serial I/O Mode)

In standard serial I/O mode, software commands, addresses and data are input and output between the MCU and peripheral units (serial programmer, etc.) using 4-wire clock-synchronized serial I/O2 (UART2).

In reception, software commands, addresses and program data are synchronized with the rise of the transfer clock that is input to the SCLK2 pin, and are then input to the MCU via the RxD2 pin. In transmission, the read data and status are synchronized with the fall of the transfer clock, and output from the TxD2 pin.

The TxD2 pin is for CMOS output. Transfer is in 8-bit units with LSB first.

When busy, such as during transmission, reception, erasing or program execution, the $\overline{\text{SRDY2}}$ (BUSY) pin is "H" level. Accordingly, always start the next transfer after the $\overline{\text{SRDY2}}$ (BUSY) pin is "L" level.

Also, data and status registers in a memory can be read after inputting software commands. Status, such as the operating state of the flash memory or whether a program or erase operation ended successfully or not, can be checked by reading the status register.

Table 10 Description of pin function (Flash Memory Serial I/O Mode 1)

Pin name	Signal name	I/O	Function
VCC,VSS	Power supply	I	Apply 2.7 to 5.5 V to the Vcc pin and 0 V to the Vss pin.
CNVSS	CNVss	I	After input of port is set, input "H" level.
RESET	Reset input	I	Reset input pin. System operates when RESET pin is set to "H" level after CNVss pin is set to "H" level.
XIN	Clock input	I	Connect an oscillation circuit between the XIN and XOUT pins. As for the connection method, refer to the "clock generating circuit".
XOUT	Clock output	O	(When system operates only by the ring oscillator, an external circuit is not required.)
VREF	Reference voltage input	I	Apply reference voltage of A-D to this pin.
P00–P03	I/O port P0	I/O	Input "L" or "H" level, or keep open.
P04	RxD input	I	Serial data input pin.
P05	TxD output	O	Serial data output pin.
P06	SCLK input	I	Serial clock input pin.
P07	BUSY output	O	BUSY signal output pin.
P10–P14	I/O port P1	I/O	Input "L" or "H" level, or keep open.
P20–P27	I/O port P2	I/O	Input "L" or "H" level, or keep open.
P30, P31, P33–P36	I/O port P3	I/O	Input "L" or "H" level, or keep open.
P32	CE input	I	Input "H" level.
P37	RP input	I	Input "L" level.

Table 11 Description of pin function (Flash Memory Serial I/O Mode 2)

Pin name	Signal name	I/O	Function
VCC,VSS	Power supply	I	Apply 2.7 to 5.5 V to the Vcc pin and 0 V to the Vss pin.
CNVSS	CNVss	I	After input of port is set, input "H" level.
RESET	Reset input	I	Reset input pin. System operates when RESET pin is set to "H" level after CNVss pin is set to "H" level.
XIN	Clock input	I	Connect an oscillation circuit between the XIN and XOUT pins. As for the connection method, refer to the "clock generating circuit".
XOUT	Clock output	O	(When system operates only by the ring oscillator, an external circuit is not required.)
VREF	Reference voltage input	I	Apply reference voltage of A-D to this pin.
P00–P03, P07	I/O port P0	I/O	Input "L" or "H" level, or keep open.
P04	RxD input	I	Serial data input pin.
P05	TxD output	O	Serial data output pin.
P06	SCLK input	I	Input "L" level.
P10–P14	I/O port P1	I/O	Input "L" or "H" level, or keep open.
P20–P27	I/O port P2	I/O	Input "L" or "H" level, or keep open.
P30, P31, P33–P36	I/O port P3	I/O	Input "L" or "H" level, or keep open.
P32	CE input	I	Input "H" level.
P37	RP input	I	Input "L" level.

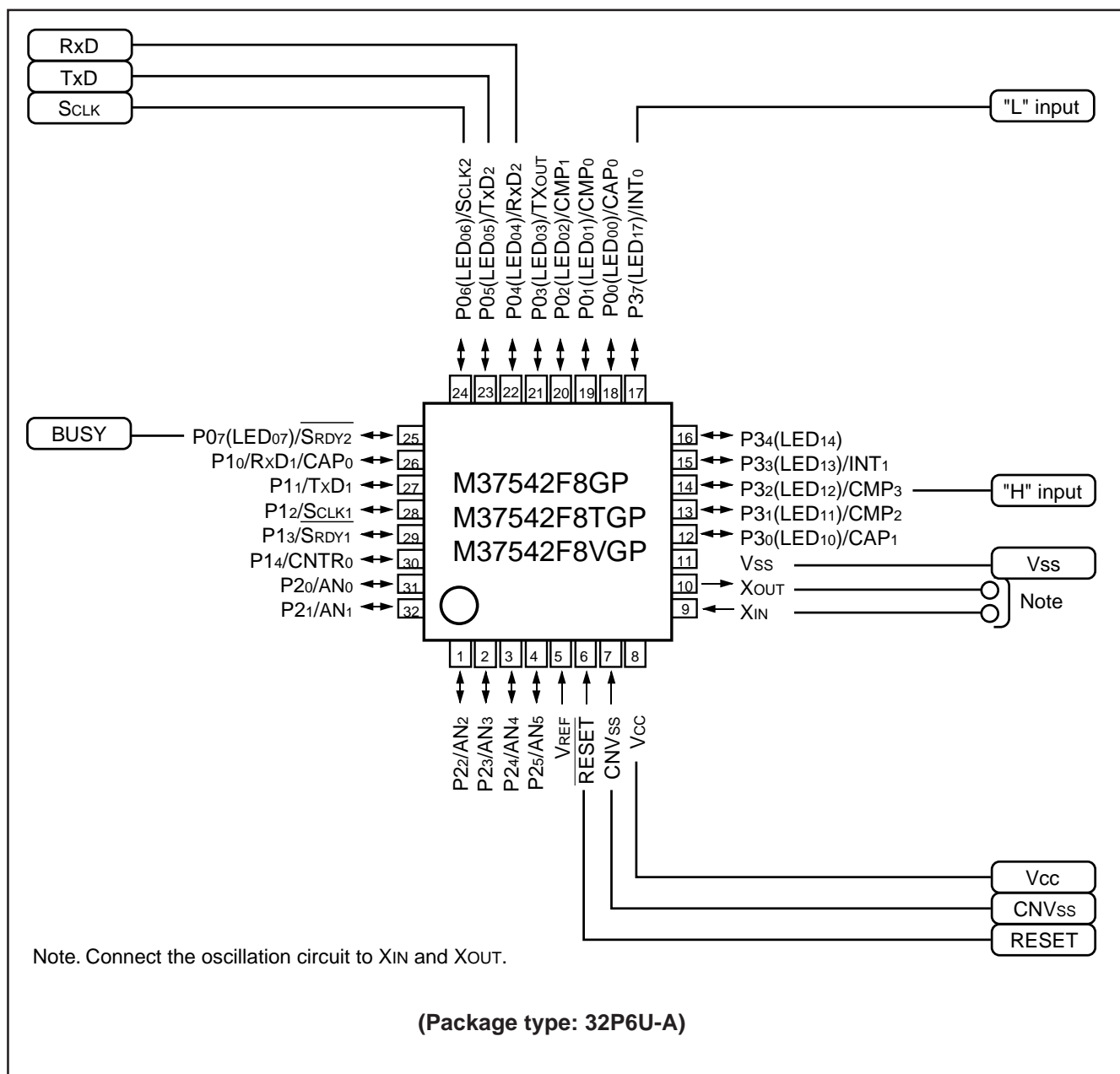


Fig. 91 Pin connection diagram in standard serial I/O mode 1 (32P6U-A package)

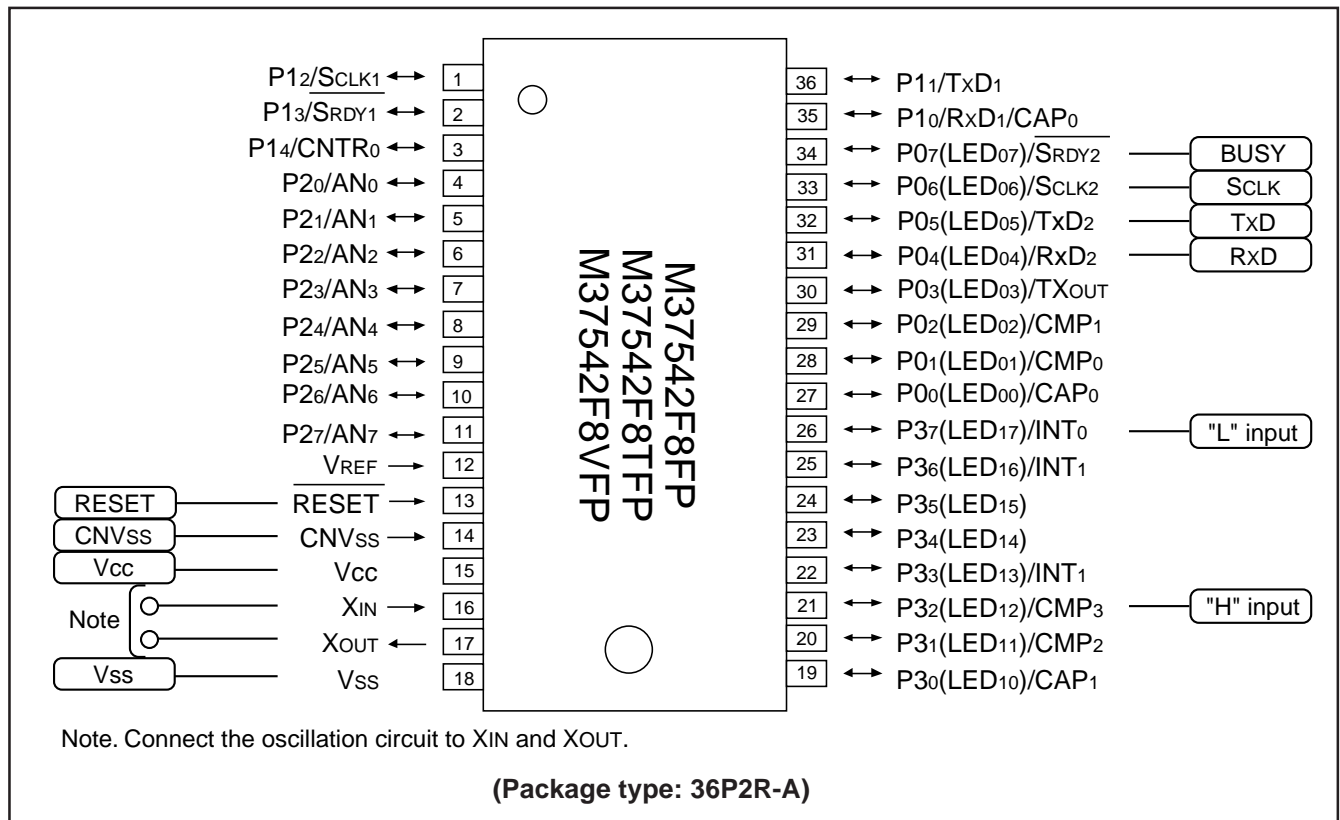


Fig. 92 Pin connection diagram in standard serial I/O mode 1 (36P2R-A package)

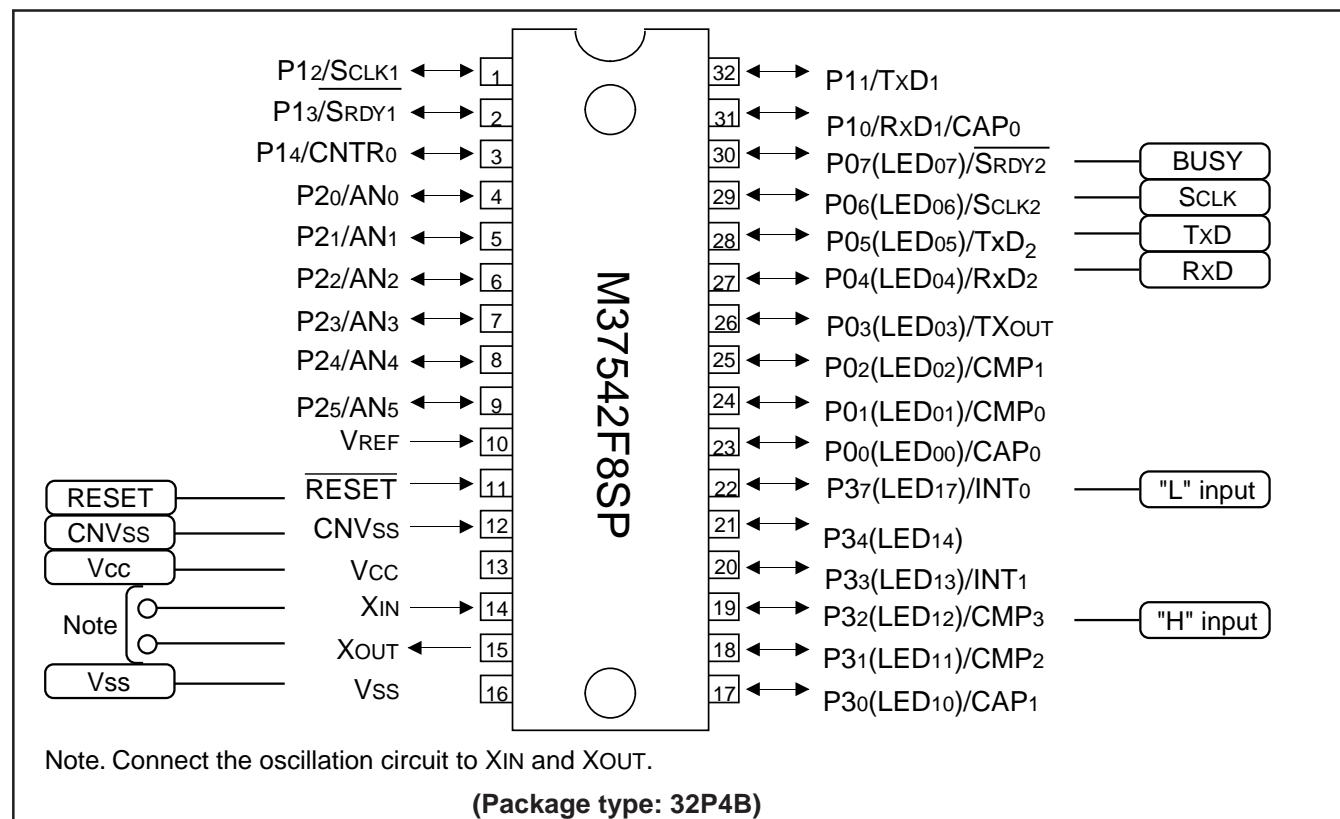


Fig. 93 Pin connection diagram in standard serial I/O mode 1 (32P4B package)

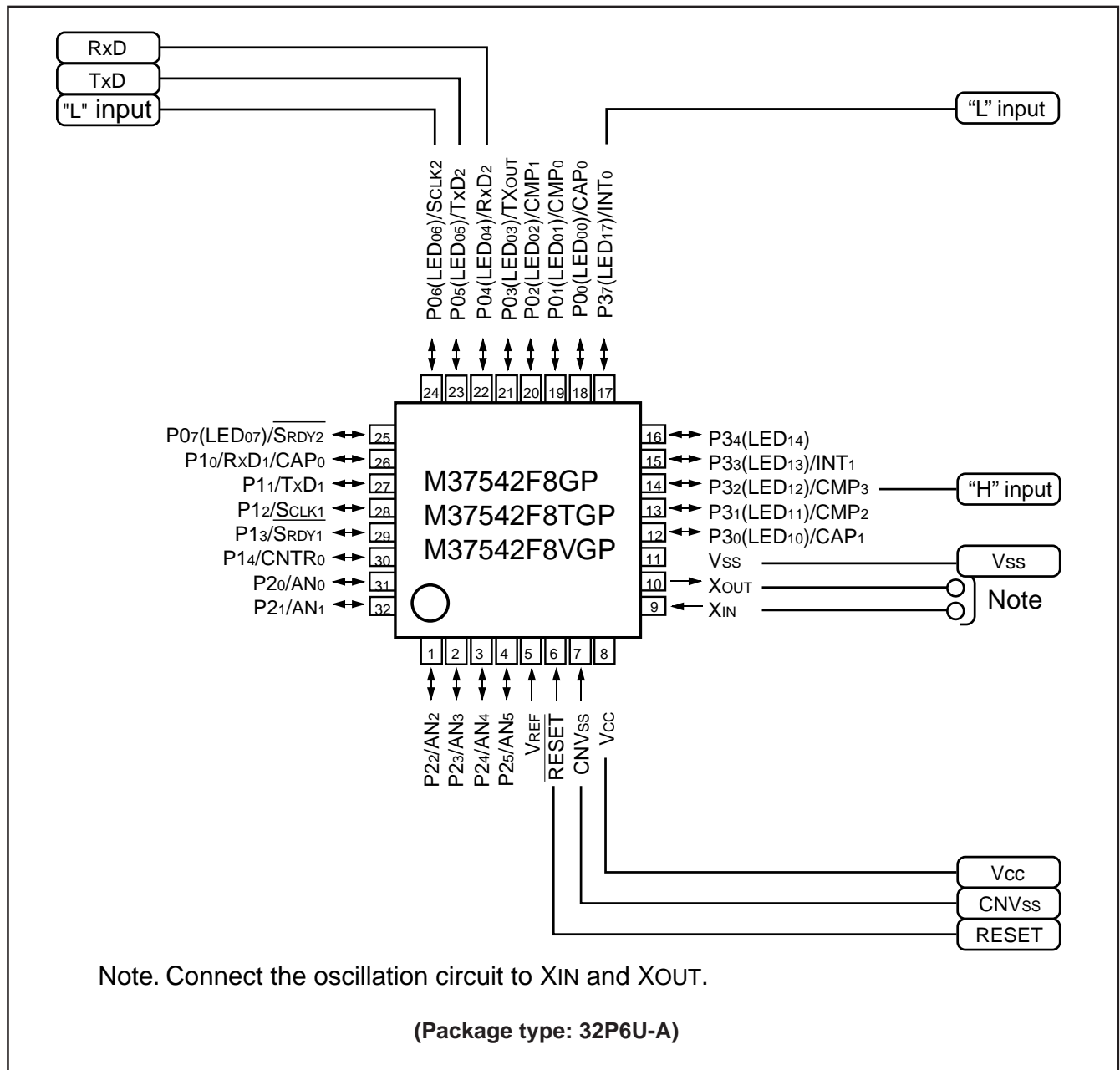


Fig. 94 Pin connection diagram in standard serial I/O mode 2 (32P6U-A package)

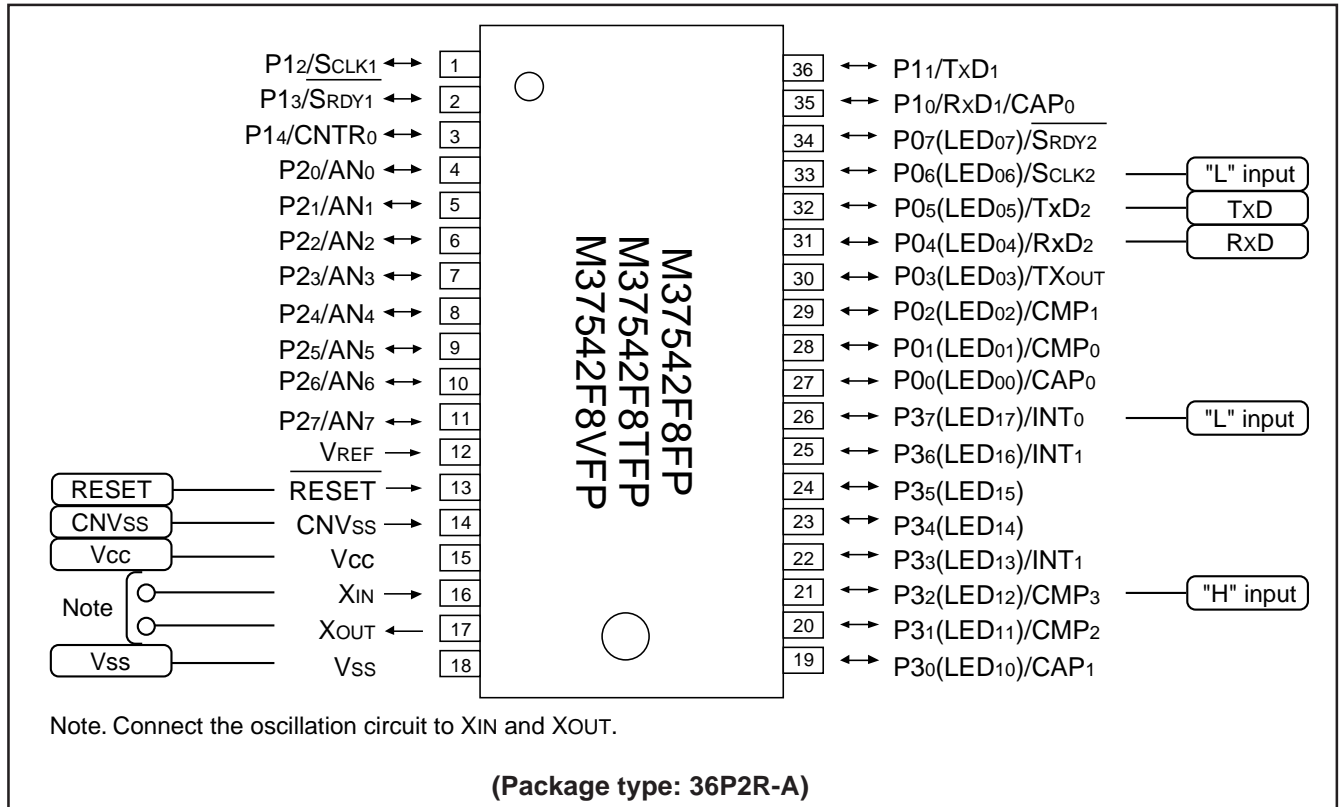


Fig. 95 Pin connection diagram in standard serial I/O mode 2 (36P2R-A package)

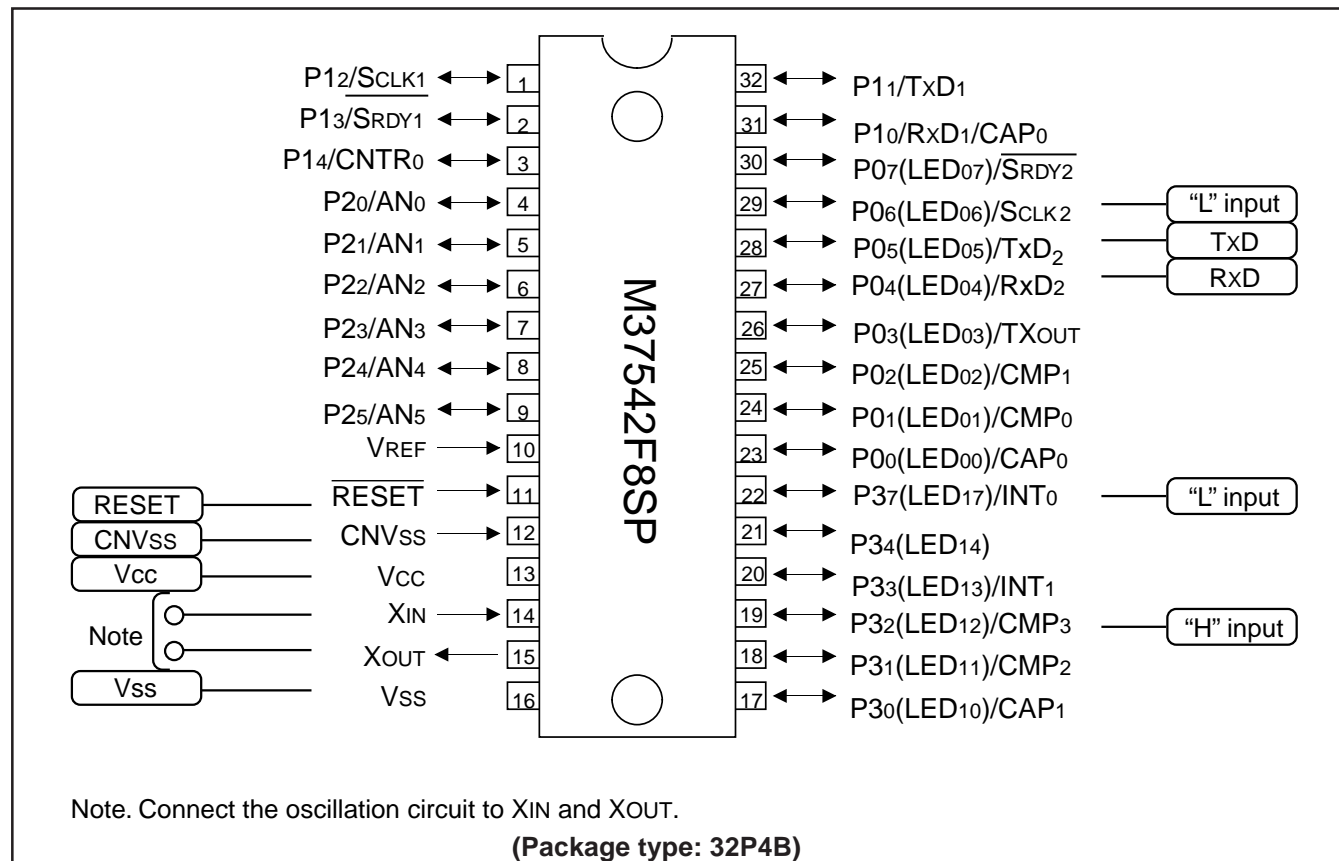


Fig. 96 Pin connection diagram in standard serial I/O mode 2 (32P4B package)

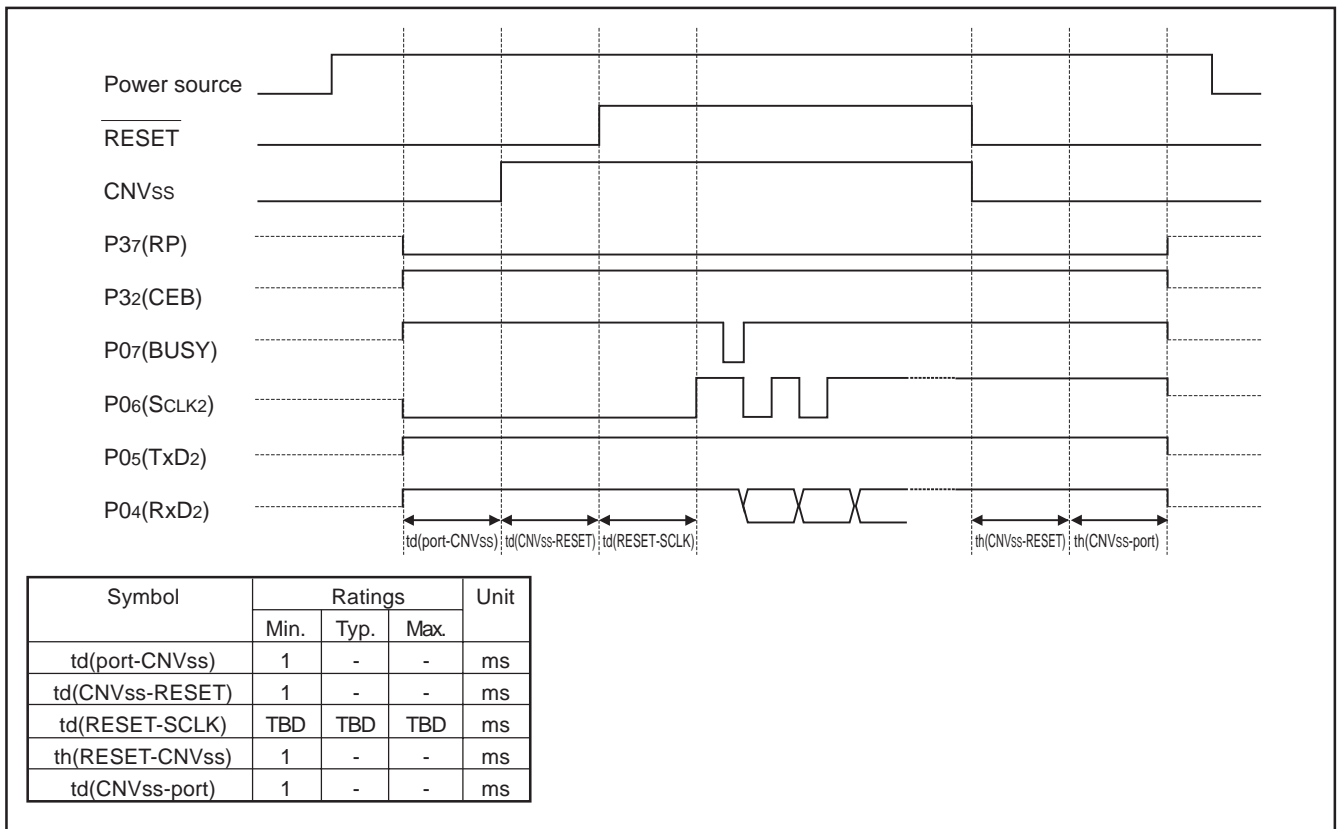


Fig. 95 Pin connection diagram in standard serial I/O mode 1

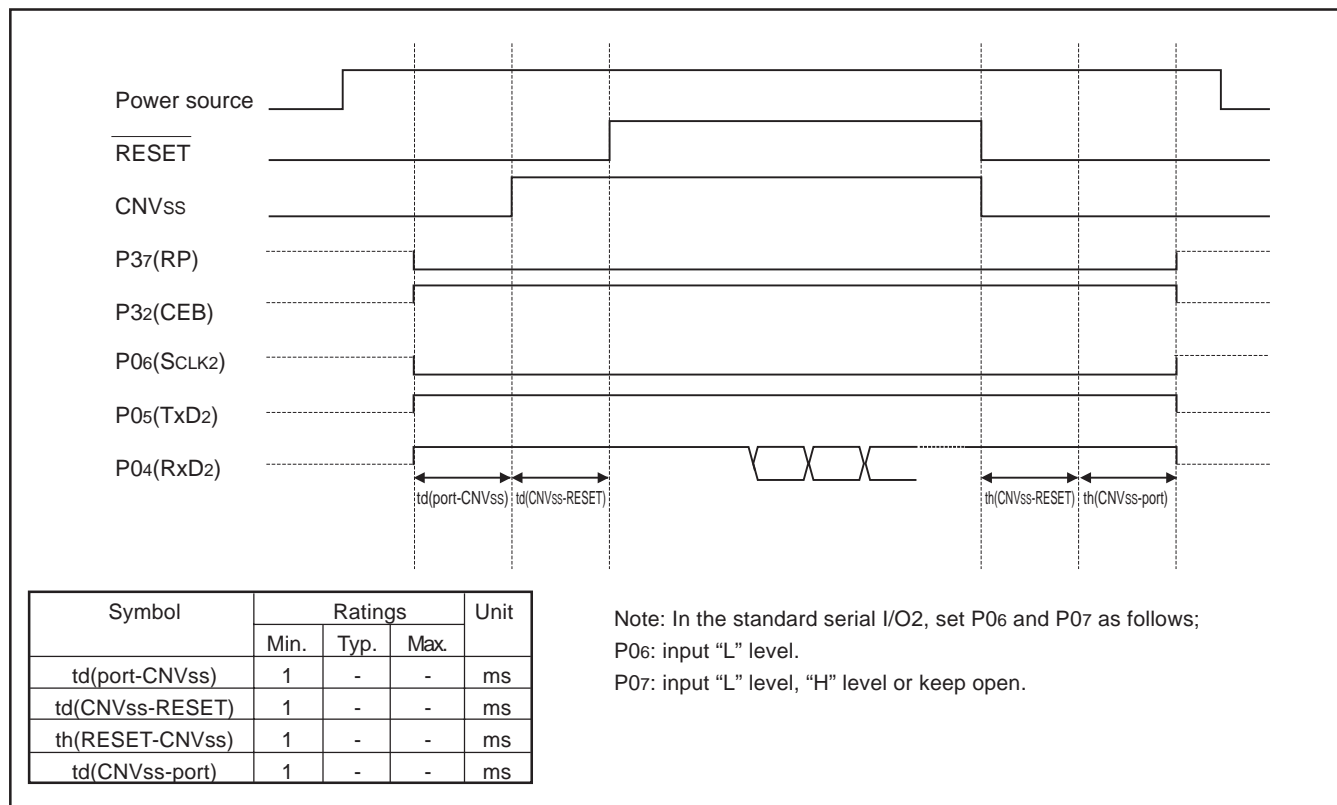


Fig. 96 Pin connection diagram in standard serial I/O mode 2

ELECTRICAL CHARACTERISTICS**1.7542Group (General purpose)**

Applied to: M37542M4/M2-XXXFP/SP/GP

Absolute Maximum Ratings (General purpose)**Table 12 Absolute maximum ratings**

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Power source voltage	All voltages are based on V _{SS} . Output transistors are cut off.	−0.3 to 6.5	V
V _I	Input voltage P00–P07, P10–P14, P20–P27, P30–P37, V _{REF}		−0.3 to V _{CC} + 0.3	V
V _I	Input voltage $\overline{\text{RESET}}$, X _{IN}		−0.3 to V _{CC} + 0.3	V
V _I	Input voltage CNV _{SS}		−0.3 to V _{CC} + 0.3	V
V _O	Output voltage P00–P07, P10–P14, P20–P27, P30–P37, X _{OUT}		−0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	T _a = 25°C	300 (Note)	mW
T _{opr}	Operating temperature		−20 to 85	°C
T _{stg}	Storage temperature		−40 to 125	°C

Note: 200 mW for the 32P6U-A package product.

Recommended Operating Conditions (General purpose)

Table 13 Recommended operating conditions (1) (V_{CC} = 2.2 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage (ceramic)	f(XIN) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(XIN) = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(XIN) = 2 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
		f(XIN) = 6 MHz (Double-speed mode)	4.5	5.0	5.5	V
		f(XIN) = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		f(XIN) = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
		f(XIN) = 1 MHz (Double-speed mode)	2.2	5.0	5.5	V
	Power source voltage (RC)	f(XIN) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(XIN) = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(XIN) = 1 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
VSS	Power source voltage			0		V
VREF	Analog reference voltage		2.0		Vcc	V
VIH	“H” input voltage P00–P07, P10–P14, P20–P27, P30–P37		0.8Vcc		Vcc	V
VIH	“H” input voltage (TTL input level selected) P10, P12, P13, P36, P37 (Note 1)		2.0		Vcc	V
VIH	“H” input voltage RESET, XIN		0.8Vcc		Vcc	V
VIL	“L” input voltage P00–P07, P10–P14, P20–P27, P30–P37		0		0.3Vcc	V
VIL	“L” input voltage (TTL input level selected) P10, P12, P13, P36, P37 (Note 1)		0		0.8	V
VIL	“L” input voltage RESET, CNVss		0		0.2Vcc	V
VIL	“L” input voltage XIN		0		0.16Vcc	V
ΣIOH(peak)	“H” total peak output current (Note 2) P00–P07, P10–P14, P20–P27, P30–P37				–80	mA
ΣIOL(peak)	“L” total peak output current (Note 2) P10–P14, P20–P27				80	mA
ΣIOL(peak)	“L” total peak output current (Note 2) P00–P07, P30–P37				80	mA
ΣIOH(avg)	“H” total average output current (Note 2) P00–P07, P10–P14, P20–P27, P30–P37				–40	mA
ΣIOL(avg)	“L” total average output current (Note 2) P10–P14, P20–P27				40	mA
ΣIOL(avg)	“L” total average output current (Note 2) P00–P07, P30–P37				30	mA

Note 1: V_{CC} = 4.0 to 5.5V

2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Recommended Operating Conditions (General purpose)(continued)**Table 14 Recommended operating conditions (2) (V_{CC} = 2.2 to 5.5 V, T_a = -20 to 85 °C, unless otherwise noted)**

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
I _{OH} (peak)	"H" peak output current (Note 1)	P00–P07, P10–P14, P20–P27, P30–P37			–10	mA
I _{OL} (peak)	"L" peak output current (Note 1)	P00–P07, P30–P37 (Drive capacity = "L") P10–P14, P20–P27			10	mA
I _{OL} (peak)	"L" peak output current (Note 1)	P00–P07, P30–P37 (Drive capacity = "H")			30	mA
I _{OH} (avg)	"H" average output current (Note 2)	P00–P07, P10–P14, P20–P27, P30–P37			–5	mA
I _{OL} (avg)	"L" average output current (Note 2)	P00–P07, P30–P37 (Drive capacity = "L") P10–P14, P20–P27			5	mA
I _{OL} (avg)	"L" average output current (Note 2)	P00–P07, P30–P37 (Drive capacity = "H")			15	mA
f(XIN)	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V _{CC} = 4.5 to 5.5 V Double-speed mode			6	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V _{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V _{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V _{CC} = 2.2 to 5.5 V Double-speed mode			1	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V _{CC} = 4.0 to 5.0 V High-, Middle-speed mode			8	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V _{CC} = 2.4 to 5.0 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V _{CC} = 2.2 to 5.0 V High-, Middle-speed mode			2	MHz
	Oscillation frequency (Note 3) at RC oscillation	V _{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at RC oscillation	V _{CC} = 2.4 to 5.0 V High-, Middle-speed mode			2	MHz
	Oscillation frequency (Note 3) at RC oscillation	V _{CC} = 2.2 to 5.0 V High-, Middle-speed mode			1	MHz

Notes 1: The peak output current is the peak current flowing in each port.**2:** The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.**3:** When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics (General purpose)

Table 15 Electrical characteristics (1) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	“H” output voltage P00–P07, P10–P14, P20–P27, P30–P37 (Note 1)	IOH = –5 mA VCC = 4.0 to 5.5 V	VCC–1.5			V
		IOH = –1.0 mA VCC = 2.2 to 5.5 V	VCC–1.0			V
VOL	“L” output voltage P00–P07, P30–P37 (Drive capacity = “L”) P10–P14, P20–P27	IOL = 5 mA VCC = 4.0 to 5.5 V			1.5	V
		IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
		IOL = 1.0 mA VCC = 2.2 to 5.5 V			1.0	V
VOL	“L” output voltage P00–P07, P30–P37 (Drive capacity = “H”)	IOL = 15 mA VCC = 4.0 to 5.5 V			2.0	V
		IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
		IOL = 10 mA VCC = 2.2 to 5.5 V			1.0	V
VT+–VT–	Hysteresis CNTR0, INT0, INT1, CAP0, CAP1 (Note 2) P00–P07 (Note 3)			0.4		V
VT+–VT–	Hysteresis RXD1, SCLK1, RXD2, SCLK2			0.5		V
VT+–VT–	Hysteresis RESET			0.5		V
IiH	“H” input current P00–P07, P10–P14, P20–P27, P30–P37	VI = VCC (Pin floating. Pull up transistors “off”)			5.0	μA
IiH	“H” input current RESET	VI = VCC			5.0	μA
IiH	“H” input current XIN	VI = VCC		4.0		μA
IiL	“L” input current P00–P07, P10–P14, P20–P27, P30–P37	VI = VSS (Pin floating. Pull up transistors “off”)			–5.0	μA
IiL	“L” input current RESET	VI = VSS			–5.0	μA
IiL	“L” input current XIN	VI = VSS		–4.0		μA
IiL	“L” input current P00–P07, P30–P37	VI = VSS (Pull up transistors “on”)		–0.2	–0.5	mA
VRAM	RAM hold voltage	When clock stopped	2.0		5.5	V
ROSC	Ring oscillator oscillation frequency	VCC = 5.0 V, Ta = 25 °C	1000	2000	3000	kHz
DOSC	Oscillation stop detection circuit detection frequency	VCC = 5.0 V, Ta = 25 °C	62.5	125	187.5	kHz

Notes 1: P11 is measured when the P11/TxD1 P-channel output disable bit of the UART1 control register (bit 4 of address 001B16) is “0”.

P05 is measured when the P05/TxD2 P-channel output disable bit of the UART2 control register (bit 4 of address 003116) is “0”.

2: RXD1, SCLK1, INT0, and INT1 (P36 selected) have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to “0” (CMOS level).

3: It is available only when operating key-on wake up.

Electrical Characteristics (General purpose)(continued)**Table 16 Electrical characteristics (2) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)**

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
I _{CC}	Power source current	Mask ROM version	f(X _{IN}) = 8 MHz	High-speed mode		TBD	TBD	mA
			Output transistors "off"	Middle-speed mode		TBD	TBD	mA
			f(X _{IN}) = 6 MHz	Double-speed mode		TBD	TBD	mA
			Output transistors "off"					
			f(X _{IN}) = 2 MHz, V _{CC} = 2.2 V	High-speed mode		TBD	TBD	mA
			Output transistors "off"					
			Ring oscillator operation mode, Output transistors "off"	Frequency/1		TBD	TBD	mA
				Frequency/2		TBD	TBD	mA
				Frequency/8		TBD	TBD	mA
				Frequency/128		TBD	TBD	mA
			f(X _{IN}) = 8 MHz (in WIT state), functions except timer 1 disabled, Output transistors "off"			TBD	TBD	mA
			f(X _{IN}) = 2 MHz, V _{CC} = 2.2 V (in WIT state), functions except timer 1 disabled, Output transistors "off"			TBD	TBD	mA
			Ring oscillator operation mode, (in WIT state), functions except timer 1 disabled, Output transistors "off"			TBD	TBD	mA
			Increment when A-D conversion is executed f(X _{IN}) = 8 MHz, V _{CC} = 5 V			TBD	TBD	mA
			All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C		0.1	1.0	μA
				Ta = 85 °C			0.1	μA

A-D Converter Characteristics (General purpose)**Table 17 A-D Converter characteristics****(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy	T _a = 25 °C, V _{CC} = 2.7 to 5.5 V			TBD	LSB
t _{CONV}	Conversion time				122	t _c (X _{IN})
R _{LADDER}	Ladder resistor			35		kΩ
I _{VREF}	Reference power source input current	V _{REF} = 5.0 V	50	150	200	μA
		V _{REF} = 3.0 V	30	90	120	
I _{I(AD)}	A-D port input current				5.0	μA

Timing Requirements (General purpose)

Table 18 Timing requirements (1) (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input "L" pulse width	2			μs
t _c (XIN)	External clock input cycle time	125			ns
t _{WH} (XIN)	External clock input "H" pulse width	50			ns
t _{WL} (XIN)	External clock input "L" pulse width	50			ns
t _c (CNTR0)	CNTR0, INT0, INT1, CAP0, CAP1 input cycle time (Note 1)	200			ns
t _{WH} (CNTR0)	CNTR0, INT0, INT1, CAP0, CAP1 input "H" pulse width (Note 1)	80			ns
t _{WL} (CNTR0)	CNTR0, INT0, INT1, CAP0, CAP1 input "L" pulse width (Note 1)	80			ns
t _c (SCLK1)	Serial I/O1, serial I/O2 clock input cycle time (Note 2)	800			ns
t _{WH} (SCLK1)	Serial I/O1, serial I/O2 clock input "H" pulse width (Note 2)	370			ns
t _{WL} (SCLK1)	Serial I/O1, serial I/O2 clock input "L" pulse width (Note 2)	370			ns
t _{su} (RxD1–SCLK1)	Serial I/O1, serial I/O2 input set up time	220			ns
t _h (SCLK1–RxD1)	Serial I/O1, serial I/O2 input hold time	100			ns

Notes 1: As for CAP0, CAP1, it is the value when noise filter is not used.

2: In this time, bit 6 of the serial I/O1 control register (address 001A16) is set to "1" (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O1 control register is "0" (clock asynchronous serial I/O is selected), the rating values are divided by 4.
In this time, bit 6 of the serial I/O2 control register (address 003016) is set to "1" (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O2 control register is "0" (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Table 19 Timing requirements (2) (V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input "L" pulse width	2			μs
t _c (XIN)	External clock input cycle time	250			ns
t _{WH} (XIN)	External clock input "H" pulse width	100			ns
t _{WL} (XIN)	External clock input "L" pulse width	100			ns
t _c (CNTR0)	CNTR0, INT0, INT1, CAP0, CAP1 input cycle time (Note 1)	500			ns
t _{WH} (CNTR0)	CNTR0, INT0, INT1, CAP0, CAP1 input "H" pulse width (Note 1)	230			ns
t _{WL} (CNTR0)	CNTR0, INT0, INT1, CAP0, CAP1 input "L" pulse width (Note 1)	230			ns
t _c (SCLK1)	Serial I/O1, serial I/O2 clock input cycle time (Note 2)	2000			ns
t _{WH} (SCLK1)	Serial I/O1, serial I/O2 clock input "H" pulse width (Note 2)	950			ns
t _{WL} (SCLK1)	Serial I/O1, serial I/O2 clock input "L" pulse width (Note 2)	950			ns
t _{su} (RxD1–SCLK1)	Serial I/O1, serial I/O2 input set up time	400			ns
t _h (SCLK1–RxD1)	Serial I/O1, serial I/O2 input hold time	200			ns

Notes 1: As for CAP0, CAP1, it is the value when noise filter is not used.

2: In this time, bit 6 of the serial I/O1 control register (address 001A16) is set to "1" (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O1 control register is "0" (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.
In this time, bit 6 of the serial I/O2 control register (address 003016) is set to "1" (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O2 control register is "0" (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Table 20 Timing requirements (3) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input "L" pulse width	2			μs
t _c (X _{IN})	External clock input cycle time	500			ns
t _{WH} (X _{IN})	External clock input "H" pulse width	200			ns
t _{WL} (X _{IN})	External clock input "L" pulse width	200			ns
t _c (CNTR ₀)	CNTR ₀ , INT ₀ , INT ₁ , CAP ₀ , CAP ₁ input cycle time (Note 1)	1000			ns
t _{WH} (CNTR ₀)	CNTR ₀ , INT ₀ , INT ₁ , CAP ₀ , CAP ₁ input "H" pulse width (Note 1)	460			ns
t _{WL} (CNTR ₀)	CNTR ₀ , INT ₀ , INT ₁ , CAP ₀ , CAP ₁ input "L" pulse width (Note 1)	460			ns
t _c (SCLK ₁)	Serial I/O1, serial I/O2 clock input cycle time (Note 2)	4000			ns
t _{WH} (SCLK ₁)	Serial I/O1, serial I/O2 clock input "H" pulse width (Note 2)	1900			ns
t _{WL} (SCLK ₁)	Serial I/O1, serial I/O2 clock input "L" pulse width (Note 2)	1900			ns
t _{su} (RxD ₁ –SCLK ₁)	Serial I/O1, serial I/O2 input set up time	800			ns
t _h (SCLK ₁ –RxD ₁)	Serial I/O1, serial I/O2 input hold time	400			ns

Notes 1: As for CAP₀, CAP₁, it is the value when noise filter is not used.

- 2:** In this time, bit 6 of the serial I/O1 control register (address 001A16) is set to "1" (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O1 control register is "0" (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.
In this time, bit 6 of the serial I/O2 control register (address 003016) is set to "1" (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O2 control register is "0" (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Switching Characteristics (General purpose)

Table 21 Switching characteristics (1) ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(SCLK1)$	Serial I/O1, serial I/O2 clock output "H" pulse width	$t_c(SCLK1)/2-30$			ns
$t_{WL}(SCLK1)$	Serial I/O1, serial I/O2 clock output "L" pulse width	$t_c(SCLK1)/2-30$			ns
$t_d(SCLK1-TxD1)$	Serial I/O1, serial I/O2 output delay time			140	ns
$t_v(SCLK1-TxD1)$	Serial I/O1, serial I/O2 output valid time	-30			ns
$t_r(SCLK1)$	Serial I/O1, serial I/O2 clock output rising time			30	ns
$t_f(SCLK1)$	Serial I/O1, serial I/O2 clock output falling time			30	ns
$t_r(CMOS)$	CMOS output rising time (Note 1)		10	30	ns
$t_f(CMOS)$	CMOS output falling time (Note 1)		10	30	ns

Note 1: Pin XOUT is excluded.

Table 22 Switching characteristics (2) ($V_{CC} = 2.4$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

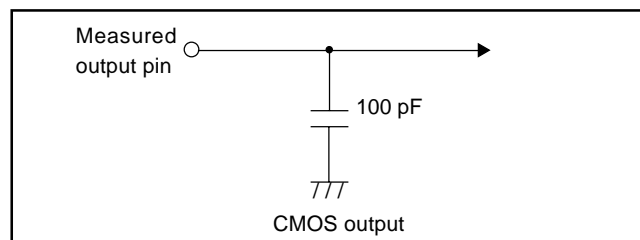
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(SCLK1)$	Serial I/O1, serial I/O2 clock output "H" pulse width	$t_c(SCLK1)/2-50$			ns
$t_{WL}(SCLK1)$	Serial I/O1, serial I/O2 clock output "L" pulse width	$t_c(SCLK1)/2-50$			ns
$t_d(SCLK1-TxD1)$	Serial I/O1, serial I/O2 output delay time			350	ns
$t_v(SCLK1-TxD1)$	Serial I/O1, serial I/O2 output valid time	-30			ns
$t_r(SCLK1)$	Serial I/O1, serial I/O2 clock output rising time			50	ns
$t_f(SCLK1)$	Serial I/O1, serial I/O2 clock output falling time			50	ns
$t_r(CMOS)$	CMOS output rising time (Note 1)		20	50	ns
$t_f(CMOS)$	CMOS output falling time (Note 1)		20	50	ns

Note 1: Pin XOUT is excluded.

Table 23 Switching characteristics (3) ($V_{CC} = 2.2$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(SCLK1)$	Serial I/O1, serial I/O2 clock output "H" pulse width	$t_c(SCLK1)/2-70$			ns
$t_{WL}(SCLK1)$	Serial I/O1, serial I/O2 clock output "L" pulse width	$t_c(SCLK1)/2-70$			ns
$t_d(SCLK1-TxD1)$	Serial I/O1, serial I/O2 output delay time			450	ns
$t_v(SCLK1-TxD1)$	Serial I/O1, serial I/O2 output valid time	-30			ns
$t_r(SCLK1)$	Serial I/O1, serial I/O2 clock output rising time			70	ns
$t_f(SCLK1)$	Serial I/O1, serial I/O2 clock output falling time			70	ns
$t_r(CMOS)$	CMOS output rising time (Note 1)		25	70	ns
$t_f(CMOS)$	CMOS output falling time (Note 1)		25	70	ns

Note 1: Pin XOUT is excluded.


Switching characteristics measurement circuit diagram (General purpose)

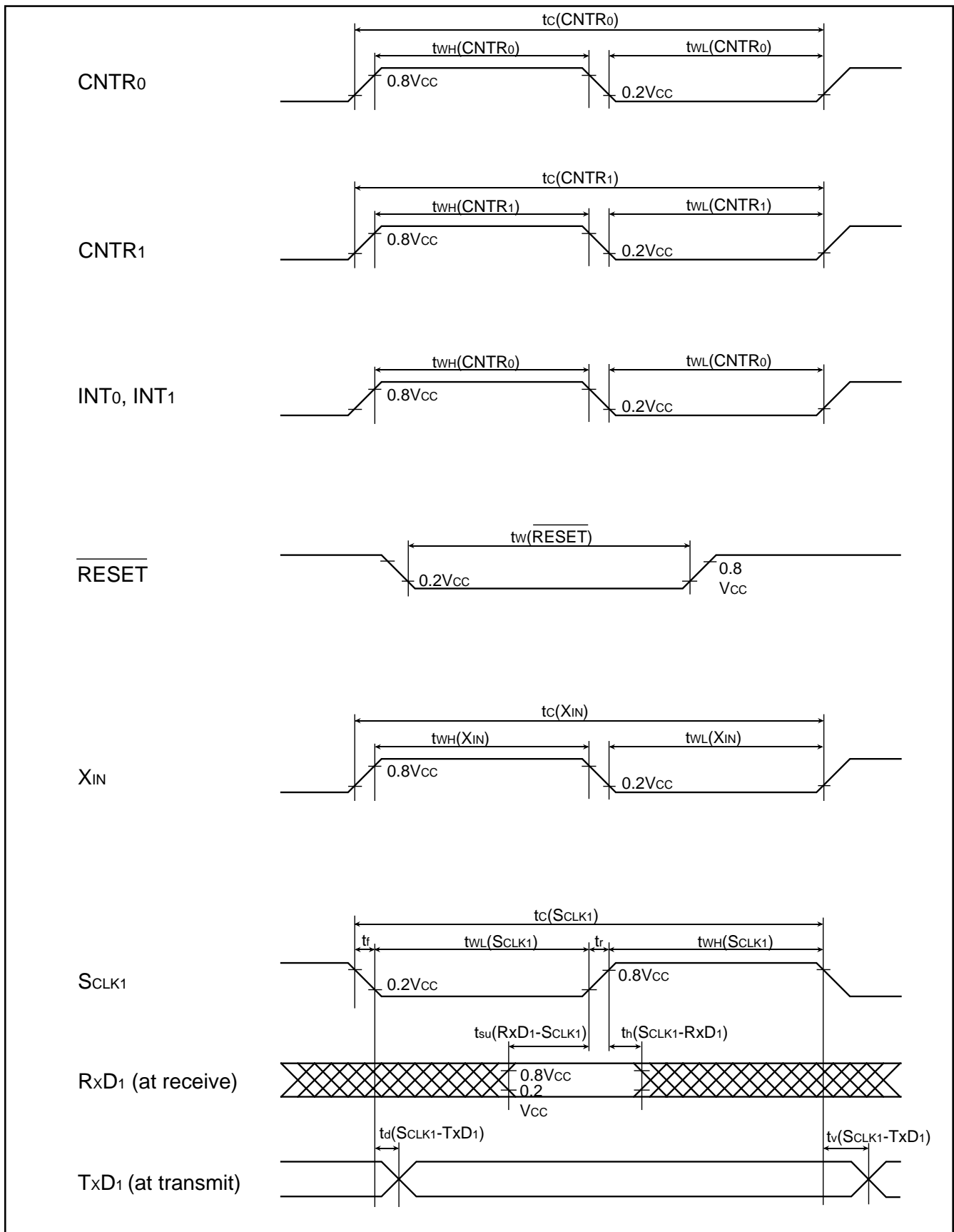
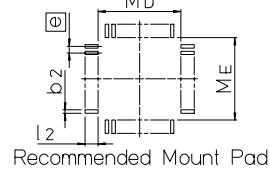
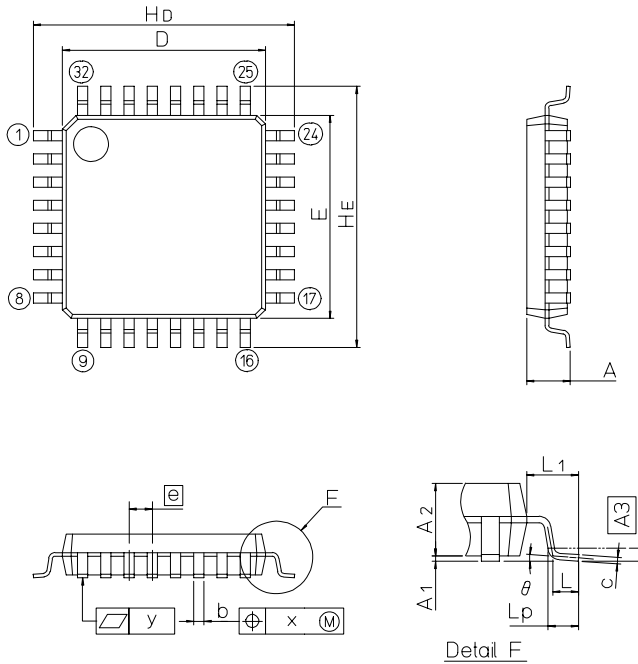


Fig. 99 Timing chart (General purpose)

PACKAGE OUTLINE**32P6U-A****Plastic 32pin 7×7mm body LQFP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-0707-0.80	—	—	Cu Alloy

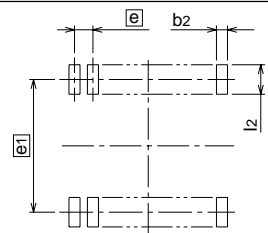
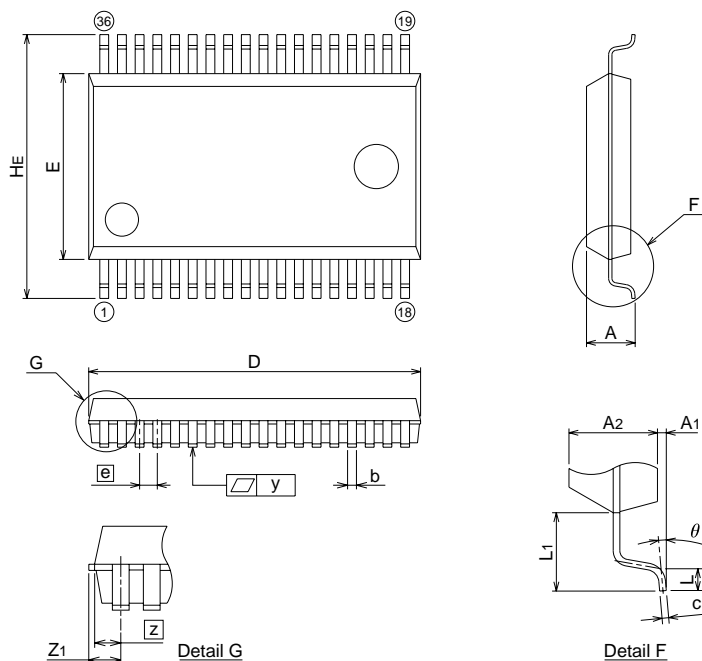
Scale: 4/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
[E]	—	0.8	—
Hd	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.3	0.5	0.7
L1	—	1.0	—
Lp	0.45	0.6	0.75
[A3]	—	0.25	—
x	—	—	0.2
y	—	—	0.1
θ	0°	—	8°
b2	—	0.5	—
l2	1.0	—	—
Md	—	7.4	—
ME	—	7.4	—

36P2R-A**Plastic 36pin 450mil SSOP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP36-P-450-0.80	—	0.53	Alloy 42



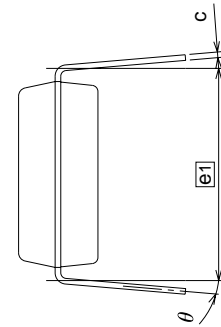
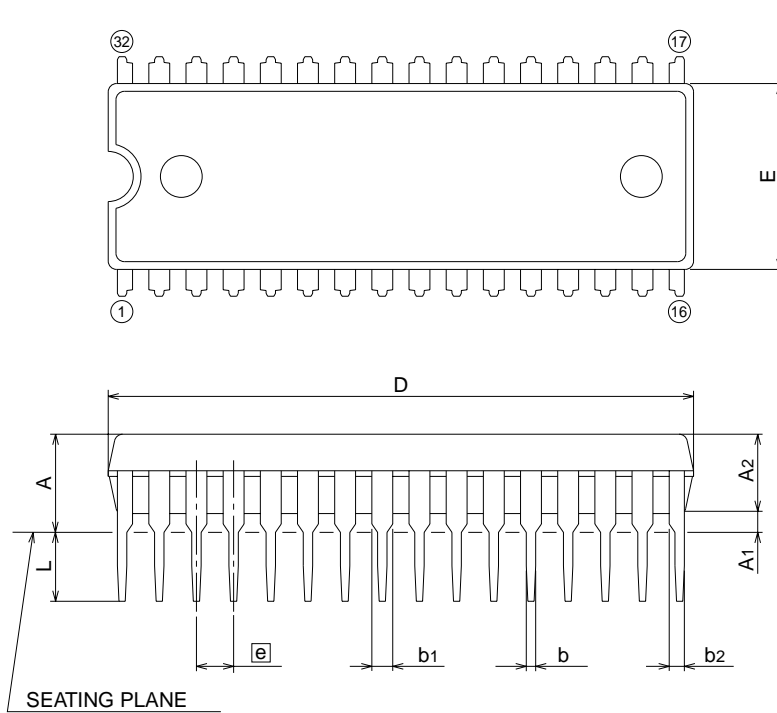
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.4
A1	0.05	—	—
A2	—	2.0	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	14.8	15.0	15.2
E	8.2	8.4	8.6
[e]	—	0.8	—
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	—	1.765	—
[Z]	—	0.7	—
Z1	—	—	0.85
y	—	—	0.15
θ	0°	—	10°
b2	—	0.5	—
[e1]	—	11.43	—
l2	1.27	—	—

32P4B

(MMP)

Plastic 32pin 400mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP32-P-400-1.78	—	2.2	Alloy 42/Cu Alloy



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.08
A1	0.51	—	—
A2	—	3.8	—
b	0.35	0.45	0.55
b1	0.9	1.0	1.3
b2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	—	1.778	—
e1	—	10.16	—
L	3.0	—	—
θ	0°	—	15°

Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.



<http://www.renesas.com>

Copyright © 2003. Renesas Technology Corporation, All rights reserved. Printed in Japan.

