

MC9S08SU16 16 KB Flash

40 MHz S08L Based Microcontroller

MC9S08SU16 and MC9S08SU8 are low-cost, high-performance and high integration UHV HCS08 8-bit microcontroller units (MCU). It uses the enhanced S08L central processor unit with 3-phase MOSFET pre-drivers unit which supports 3 high-side PMOSes and 3 low-side NMOSes, amplifiers for current measurement, OCP (over current protection) and OVP (over voltage protection). It is put into a 4mm x 4mm 24-pin QFN package, targeting drone electrical speed controller, low power motor control, small form cooling fan control and portable tools.

MC9S08SU16VFK
MC9S08SU8VFK



24-pin QFN (FK)
4 x 4 x 0.65 Pitch 0.5 mm

Core

- S08L core up to 40 MHz
- Bus up to 20 MHz

Memories

- 16 KB program flash memory for SU16 and 8 KB program flash memory for SU8
- 768 byte SRAM, 256 B of which is unrestricted, the other 512 B is restricted during Flash erasing and programming
- 8 bytes regfile

System peripherals

- Windowed COP with multiple clock sources (watch dog)
- Inter module connection module
- CRC

Clocks

- External clock input
- 32 kHz tunable internal RC oscillator
- 20 kHz low power clock

Operating Characteristics

- Voltage range: 4.5 to 18 V
- Temperature range (ambient): -40 to 105°C

Human-machine interface

- 5 V input/output for logical I/O

Communication interfaces

- One SCI module
- One I2C module supporting SMBus communications interface

Analog Modules

- Two 12-bit ADC with up to 8 channels
- Analog comparator with up to 4 inputs and internal 6-bit DAC
- High voltage GDU

Timers

- Two 16-bit pulse width timers (PWT)
- Two programmable delay block (PDB)
- One 16-bit FTM
- One 16-bit modulo timer (MTIM)
- One 16-bit 6-channel PWM

Security and integrity modules

- 64-bit unique identification number per chip

Ordering information

| Part Number | Memory | | Maximum number of I/O's |
|---------------|------------|-------------|-------------------------|
| | Flash (KB) | SRAM (Byte) | |
| MC9S08SU16VFK | 16 | 768 | 17 |
| MC9S08SU8VFK | 8 | 768 | 17 |

Related resources

| Type | Description | Resource |
|------------------|---|---|
| Selector Guide | The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector. | Solution Advisor |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. ¹ | MC9S08SU16RM |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. | MC9S08SU16 ¹ |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. | xN88M ² |
| Package drawing | Package dimensions are provided in package drawings. | QFN 24-pin: 98ASA00602D |

1. To find the associated resource, go to [nxp.com](#) and perform a search using this term.
2. To find the associated resource, go to [nxp.com](#) and perform a search using this term with the "x" replaced by the revision of the device you are using.

[Figure 1](#) shows the functional modules in the chip.

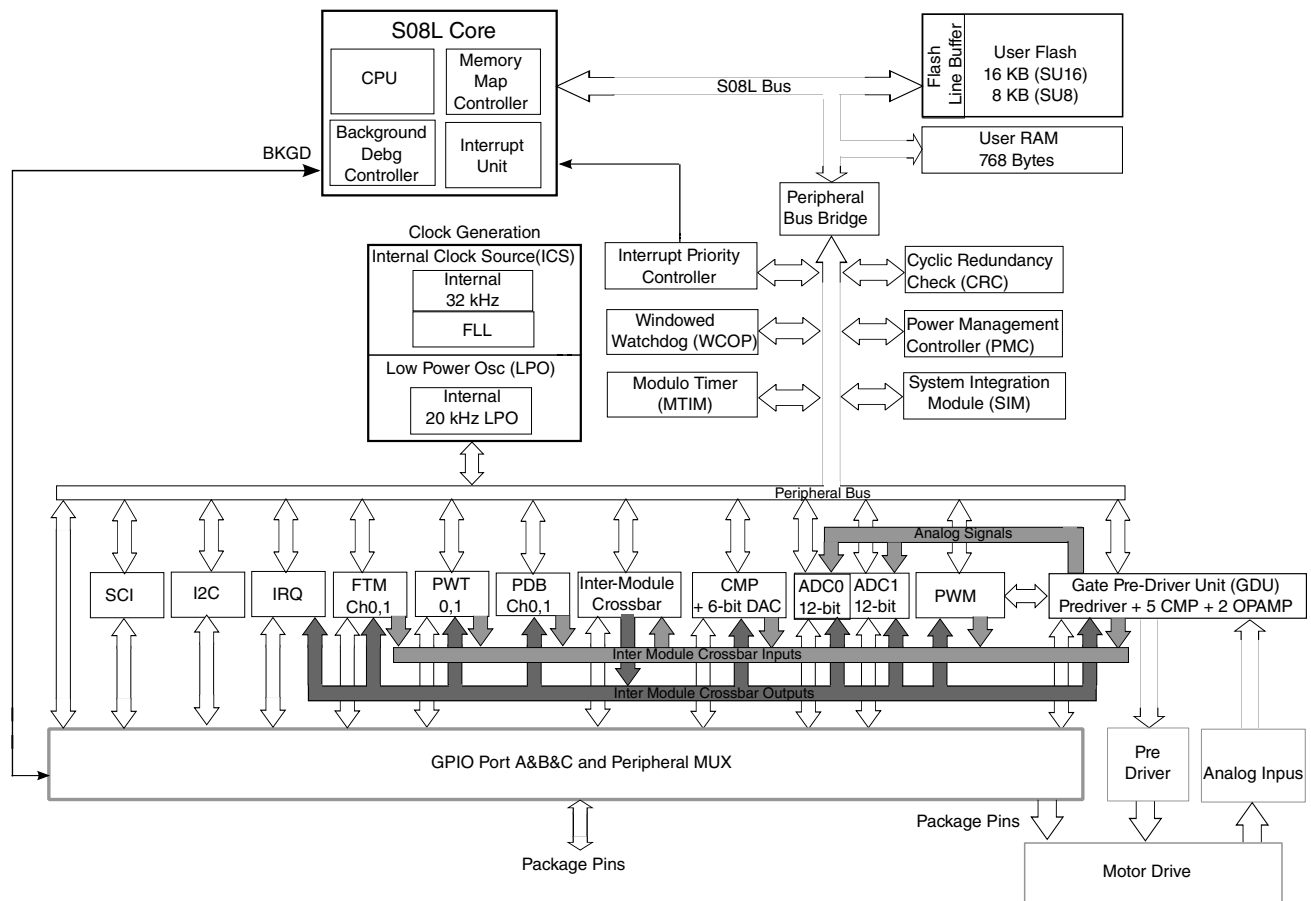


Figure 1. Functional block diagram

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1 Ratings

1.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T _{STG} | Storage temperature | −55 | 150 | °C | 1 |
| T _{SDR} | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|-------|-------|------|-------|
| V _{HBM} | Electrostatic discharge voltage, human body model | −2000 | +2000 | V | 1 |
| V _{CDM} | Electrostatic discharge voltage, charged-device model | −500 | +500 | V | 2 |
| I _{LAT} | Latch-up current at ambient temperature of 105°C | −100 | +100 | mA | |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

1.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DDX}) or the programmable pullup resistor associated with the pin is enabled.

| Symbol | Description | Min. | Max. | Unit |
|-----------|--|------|---------------|------|
| V_{DD} | Supply voltage | 4.5 | 18 | V |
| V_{DDX} | Supply voltage to digital I/O drivers ¹ | 4.20 | 5.25 | V |
| I_{DDX} | Maximum current into V_{DDX} | — | 50 | mA |
| V_{DIO} | Digital input voltage (except \overline{RESET} or true open drain pin PTA4 and PTA5) | -0.3 | $V_{DDX}+0.3$ | V |
| | Digital input voltage (true open drain pin PTA4 and PTA5) | -0.3 | $V_{DDX}+0.3$ | V |
| V_{AIO} | Analog ² , \overline{RESET} input voltage | -0.3 | $V_{DDX}+0.3$ | V |
| I_D | Instantaneous maximum current single pin limit (applies to all port pins) | -25 | 25 | mA |

1. See [Table 2](#) for detail.

2. All digital I/O pins, except open-drain pin PTA4 and PTA5, are internally clamped to V_{SS} and V_{DDX} . PTA4 and PTA5 is only clamped to V_{SS} .

2 General

2.1 Nonswitching electrical specifications

2.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 1. DC characteristics

| Symbol | C | Descriptions | | | Min | Typical ¹ | Max | Unit |
|--------------------|---|---|---|---|-------------------------|----------------------|-------------------------|------|
| — | — | Operating voltage | | | 4.5 | — | 18 | V |
| V _{OH} | P | Output high voltage | All I/O pins, standard-drive strength | 5 V, I _{load} = -5 mA | V _{DDX} - 0.8 | — | — | V |
| | P | | High current drive pins, high-drive strength ² | 5 V, I _{load} = -20 mA | V _{DDX} - 0.8 | — | — | V |
| I _{OHT} | D | Output high current | Max total I _{OH} for all ports | 5 V | — | — | -100 | mA |
| V _{OL} | P | Output low voltage | All I/O pins, standard-drive strength | 5 V, I _{load} = 5 mA | — | — | 0.8 | V |
| | P | | High current drive pins, high-drive strength ² | 5 V, I _{load} = 20 mA | — | — | 0.8 | V |
| I _{OLT} | D | Output low current | Max total I _{OL} for all ports | 5 V | — | — | 100 | mA |
| V _{IH} | P | Input high voltage | All digital inputs | V _{DDX} > 4.5V | 0.70 × V _{DDX} | — | — | V |
| | C | | | V _{DDX} > 2.7V | 0.75 × V _{DDX} | — | — | |
| V _{IL} | P | Input low voltage | All digital inputs | V _{DDX} > 4.5V | — | — | 0.30 × V _{DDX} | V |
| | C | | | V _{DDX} > 2.7V | — | — | 0.35 × V _{DDX} | |
| V _{hys} | C | Input hysteresis | All digital inputs | — | 0.06 × V _{DDX} | — | — | mV |
| I _{Iin} | P | Input leakage current | All input only pins (per pin) | V _{IN} = V _{DDX} or V _{SS} | — | 0.1 | 1 | μA |
| I _{OZTOT} | C | Total leakage combined for all inputs and Hi-Z pins | All input only and I/O | V _{IN} = V _{DDX} or V _{SS} | — | — | 2 | μA |

Table continues on the next page...

Table 1. DC characteristics (continued)

| Symbol | C | Descriptions | | | Min | Typical ¹ | Max | Unit |
|------------------------------|---|---|--|-------------------------------------|------|----------------------|------|------|
| R _{PU} | P | Pullup resistors | All digital inputs, when enabled (all I/O pins other than PTA4 and PTA5) | — | 30.0 | — | 50.0 | kΩ |
| R _{PU} ³ | P | Pullup resistors | PTA4 and PTA5 pin | — | 30.0 | — | 60.0 | kΩ |
| R _{PD} ⁴ | P | Pulldown resistors | PTB3, PTB4 and PTB5 pin | — | 30 | 40 | 50 | kΩ |
| I _{IC} | D | DC injection current ^{5, 6, 7} | Single pin limit | V _{IN} < V _{SS} , | -2 | — | 2 | mA |
| | | | Total MCU limit, includes sum of all stressed pins | V _{IN} > V _{DDX} | -5 | — | 25 | |
| C _{In} | C | Input capacitance, all pins | | | — | — | 7 | pF |
| V _{RAM} | C | RAM retention voltage | | | 2.0 | — | — | V |

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB3, PTB4, PTB5, and PTB7 are high drive pins, and support ultra-high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. The specified resistor value is the actual value internal to the device. The pulldown value may appear higher when measured externally on the pin.
5. All functional non-supply pins, except PTA4 and PTA5, are internally clamped to V_{SS} and V_{DDX}.
6. Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
7. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current (V_{IN} > V_{DD}) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 2. Power supply electrical characteristics

| Symbol | Description | Min. | Typical ¹ | Max. | Unit |
|-------------------|----------------------------------|---|----------------------|------------------|---------|
| V _{DDX} | Output voltage V _{DDX} | Run mode 4.5 V ≤ V _{DD} < 5.3 V | 4.20 | — | 5.25 V |
| | | Run mode V _{DD} ≥ 5.3 V | 4.75 | 4.99 | 5.25 V |
| | | Stop mode ² | 2.5 | — | 5.75 V |
| I _{DDX} | Load current V _{DDX} | Run mode 4.5 V ≤ V _{DD} < 5.3 V | 0 | — | 28 mA |
| | | Run mode V _{DD} ≥ 5.3 V | 0 | — | 50 mA |
| | | Stop mode ² | 0 | — | 5 mA |
| V _{REFH} | Output voltage V _{REFH} | V _{DD} ≥ 4.5 V | 4.166 | 4.2 ³ | 4.234 V |
| — | V _{REFH} accuracy | V _{DD} ≥ V _{REFH} + 0.3, 0—70 °C | — | — | 0.8 % |
| | | V _{DD} ≥ V _{REFH} + 0.3, -40—105 °C | — | — | 1.0 % |
| I _{REFH} | Output current V _{REFH} | V _{DD} ≥ V _{REFH} + 0.3 | 0 | — | 5 mA |

Table continues on the next page...

Table 2. Power supply electrical characteristics (continued)

| Symbol | Description | | Min. | Typical ¹ | Max. | Unit |
|-----------------------|---|---------------------------------|------|----------------------|------|-------|
| V _{LVWA} | V _{DDX} Low voltage warning assert level | PMC_LVCTLSTAT1[SLVWSEL] = 1b | 3.43 | 3.63 | 3.83 | V |
| | | PMC_LVCTLSTAT1[SLVWSEL] = 0b | 3.94 | 4.14 | 4.34 | |
| V _{LVWD} | V _{DDX} Low voltage warning deassert level | PMC_LVCTLSTAT1[SLVWSEL] = 1b | 3.54 | 3.74 | 3.94 | V |
| | | PMC_LVCTLSTAT1[SLVWSEL] = 0b | 4.08 | 4.28 | 4.48 | |
| V _{LVRA} | V _{DDX} low voltage reset assert | | 2.97 | 3.02 | — | V |
| V _{LVRD} | V _{DDX} low voltage reset deassertl | | — | — | 3.13 | V |
| V _{LVWREFHA} | Low voltage warning for V _{REFH} assert level ⁴ | PMC_VREFHLVW[LVWCFG]=00b | 3.34 | 3.54 | 3.74 | V |
| | | PMC_VREFHLVW[LVWCFG]=01b | 3.43 | 3.63 | 3.83 | V |
| | | PMC_VREFHLVW[LVWCFG]=10b | 3.86 | 4.06 | 4.26 | V |
| | | PMC_VREFHLVW[LVWCFG]=11b | 4.11 | 4.31 | 4.51 | V |
| V _{LVWREFHA} | Low voltage warning for V _{REFH} deassert level ⁴ | PMC_VREFHLVW[LVWCFG]=00b | 3.45 | 3.65 | 3.85 | V |
| | | PMC_VREFHLVW[LVWCFG]=01b | 3.55 | 3.75 | 3.95 | V |
| | | PMC_VREFHLVW[LVWCFG]=10b | 4.00 | 4.20 | 4.40 | V |
| | | PMC_VREFHLVW[LVWCFG]=11b | 4.27 | 4.47 | 4.67 | V |
| f _{LPOCLK} | Trimmed LPOCLK output frequency | | — | 20 | — | kHz |
| df _{LPOCLK} | Trimmed LPOCLK internal clock Δf / f _{NOMINAL} ⁵ | | -5 | — | 5 | % |
| t _{SDEL} | LPOCLK start up delay | | — | 25 | 50 | μs |
| dV _{HT} | Temperature sensor slope | | — | 5.07 | — | mV/°C |
| V _{HT} | Temperature sensor output voltage | | — | 1.73 | — | V |
| T _{HTIA} | High temperature interrupt assert ⁶ | | 110 | 130 | 150 | °C |
| T _{HTID} | High temperature interrupt deassert ⁶ | | 100 | 120 | 140 | °C |
| V _{BG} | Bandgap output voltage | | 1.13 | 1.2 | 1.32 | V |
| V _{HCBG} | HC Bandgap output voltage | | 1.14 | 1.15 | 1.16 | V |
| t _{STP_REC} | Recovery time from Stop | not including V _{REFH} | — | 15 | — | μs |
| | | including V _{REFH} | — | 1 | — | ms |

1. Typical values are measured at 25 °C.
2. Power supply enters reduced power mode when MCU is in Stop mode.
3. This typical value is configurable based on V_{REC}.
4. PMC_VREFHLVW[LVWCFG]=01b is recommended for the configuration.
5. User need to trim the LPOCLK in order to get ±5% LPOCLK
6. This is junction temperature.

Figure 2 illustrates the power distribution of this chip.

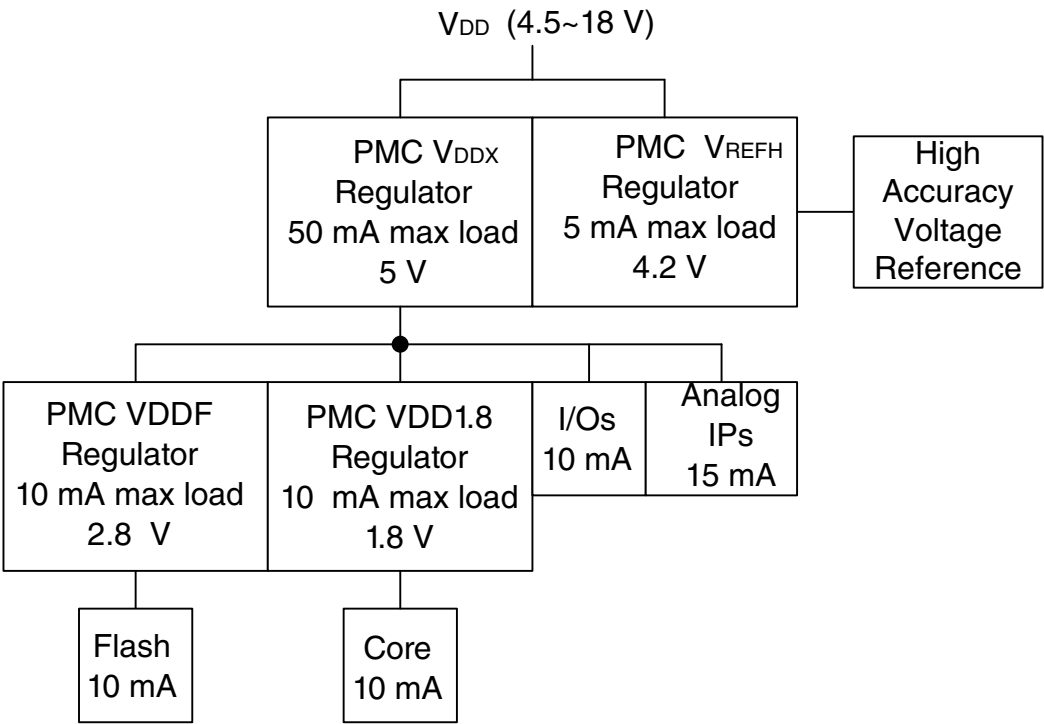


Figure 2. Power distribution

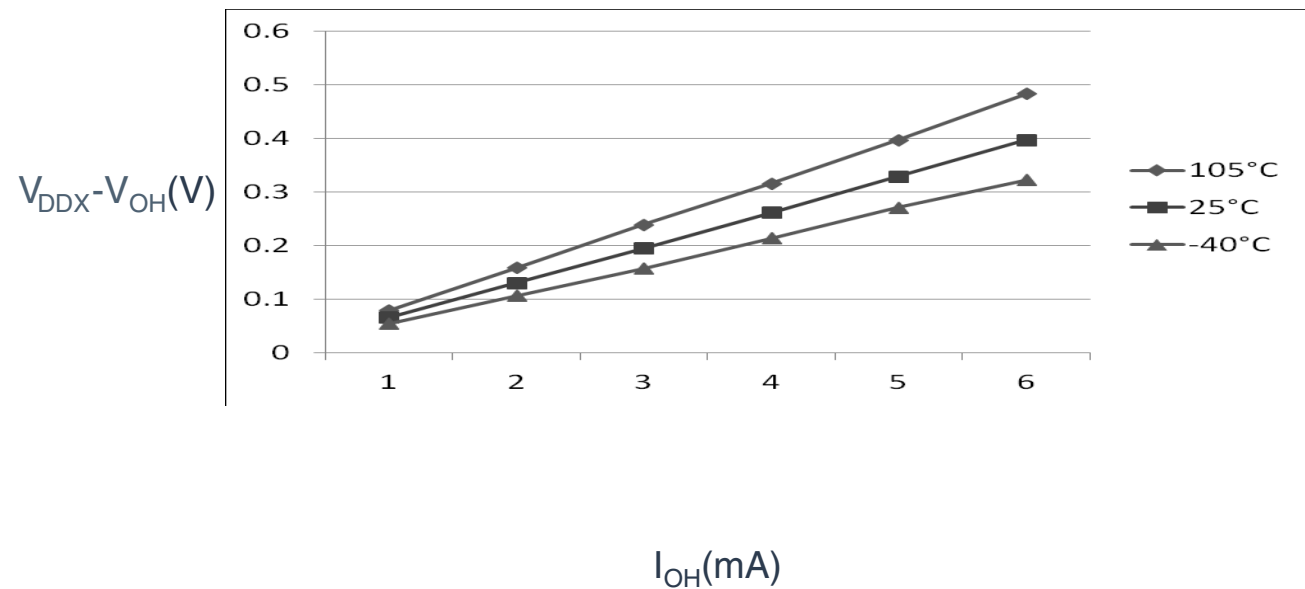


Figure 3. Typical I_{OH} Vs. $V_{DDX}-V_{OH}$ (standard drive strength) ($V_{DDX} = 5$ V)

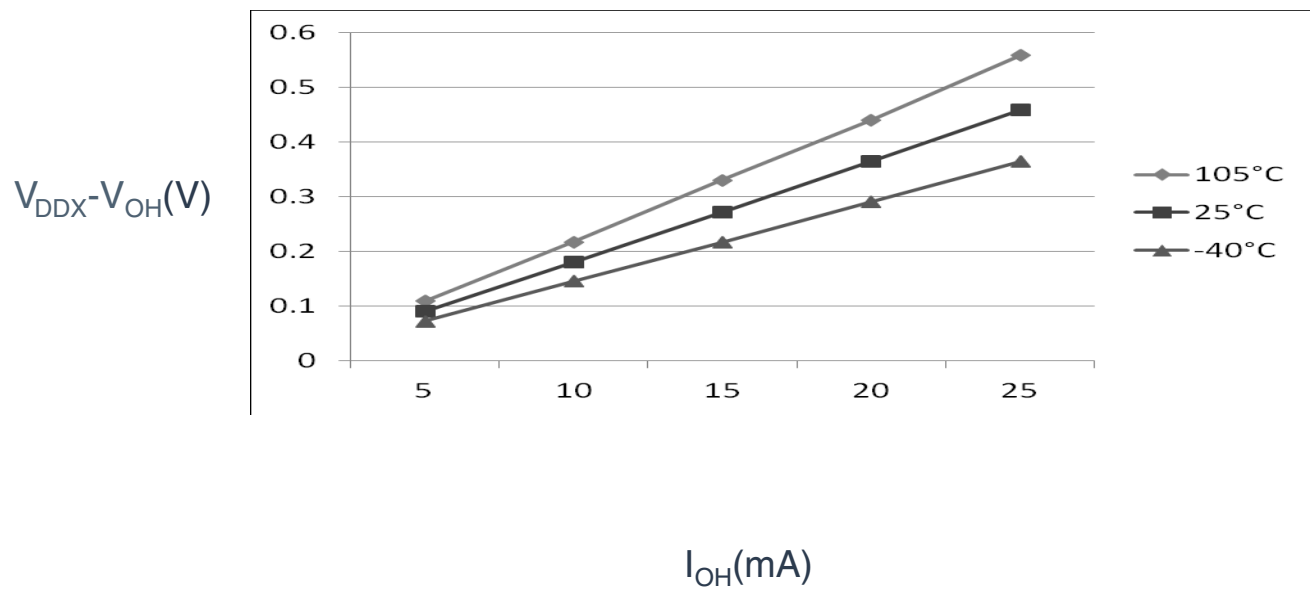


Figure 4. Typical I_{OH} Vs. $V_{DDX} - V_{OH}$ (high drive strength) ($V_{DDX} = 5$ V)

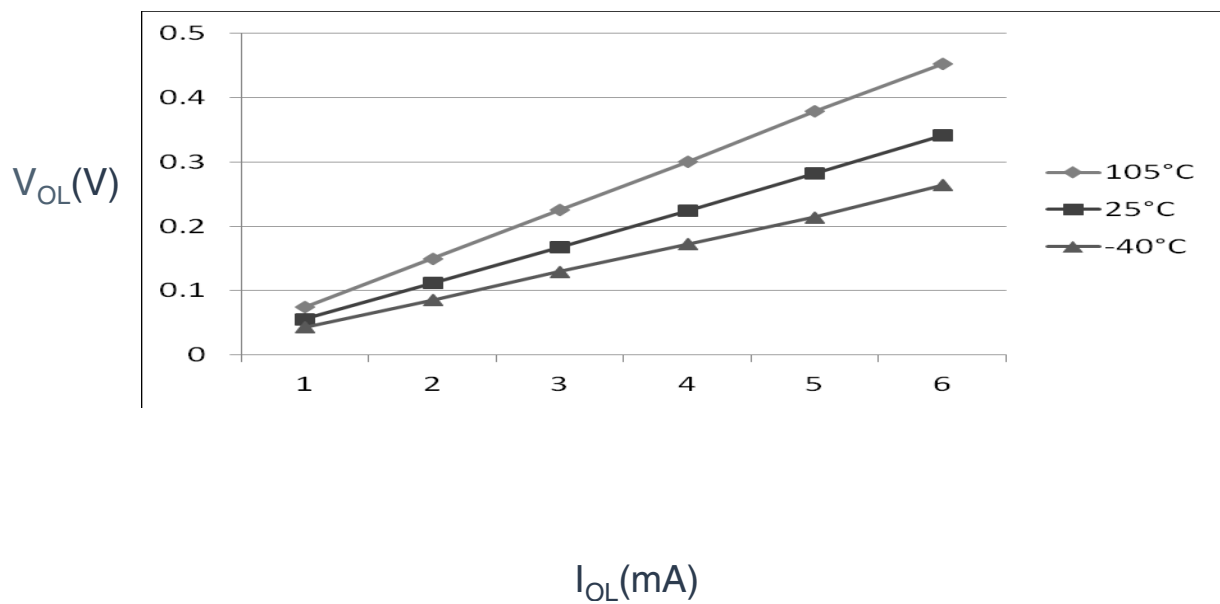


Figure 5. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DDX} = 5$ V)

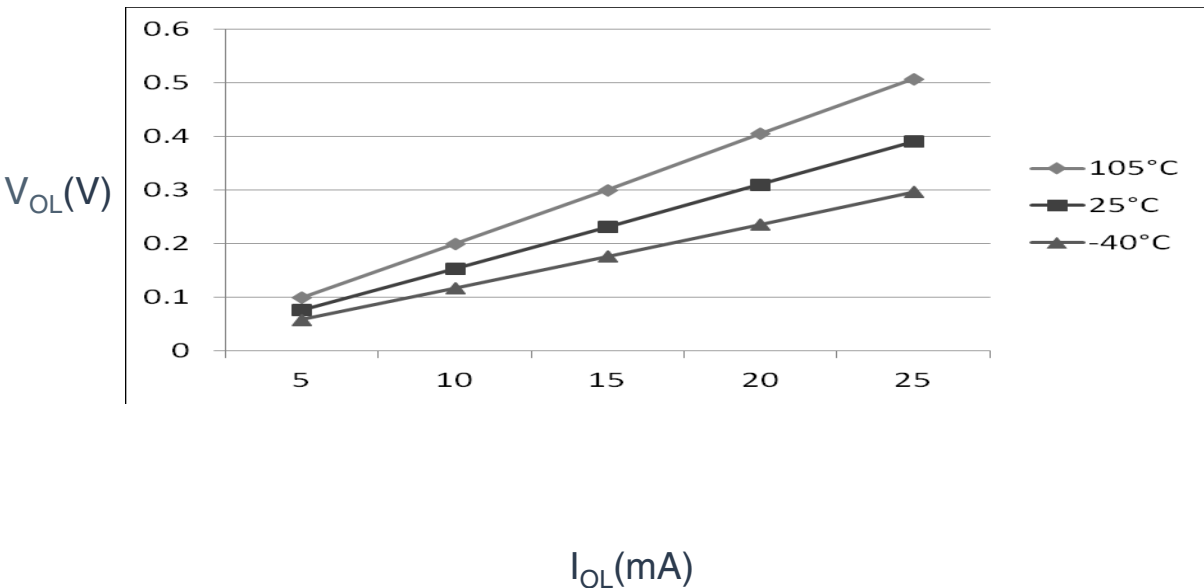


Figure 6. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DDX} = 5\text{ V}$)

2.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 3. Supply current characteristics

| C | Parameter | Symbol | Core/Bus Freq | V _{DD} (V) | Typical ¹ | Max | Unit | Temp |
|---|--|------------------|---------------|---------------------|----------------------|-----|------|---------------|
| C | Run supply current, FEI mode, all clock gate is off, code run from flash | R _{IDD} | 40/20 MHz | 18 | 11.00 | — | mA | -40 to 105 °C |
| C | | | 20/10 MHz | | 7.50 | — | | |
| | | | 20/1 MHz | | 6.00 | — | | |
| C | | | 20/20 MHz | 12 | 9.15 | — | | |
| | | | 20/10 MHz | | 7.50 | — | | |
| | | | 20/1 MHz | | 5.95 | — | | |
| | | | 20/20 MHz | 5.3 | 9.10 | — | | |
| | | | 20/10 MHz | | 7.45 | — | | |
| | | | 20/1 MHz | | 5.90 | — | | |
| | | | 20/20 MHz | 4.5 | 9.35 | — | | |
| | | | 20/10 MHz | | 7.65 | — | | |
| | | | 20/1 MHz | | 6.15 | — | | |

Table continues on the next page...

Table 3. Supply current characteristics (continued)

| C | Parameter | Symbol | Core/Bus Freq | V _{DD} (V) | Typical ¹ | Max | Unit | Temp |
|---|---|------------------|---------------|---------------------|----------------------|-----|------|---------------|
| C | Run supply current, FEI mode, all clock gate is on, code run from flash | RI _{DD} | 40/20 MHz | 18 | 13.05 | — | mA | -40 to 105 °C |
| C | | | 20/10 MHz | | 8.45 | — | | |
| | | | 20/1 MHz | | 6.05 | — | | |
| C | | | 20/20 MHz | 12 | 11.00 | — | | |
| C | | | 20/10 MHz | | 8.40 | — | | |
| | | | 20/1 MHz | | 6.00 | — | | |
| | | | 20/20 MHz | 5.3 | 10.95 | — | | |
| | | | 20/10 MHz | | 8.35 | — | | |
| | | | 20/1 MHz | | 6.00 | — | | |
| | | | 20/20 MHz | 4.5 | 11.20 | — | | |
| | | | 20/10 MHz | | 8.60 | — | | |
| | | | 20/1 MHz | | 6.20 | — | | |
| C | Run supply current, FBE mode, all clock gate is off, code run from SRAM | RI _{DD} | 40/20 MHz | 18 | 9.60 | — | mA | -40 to 105 °C |
| C | | | 20/10 MHz | | 6.05 | — | | |
| | | | 20/1 MHz | | 4.50 | — | | |
| C | | | 20/20 MHz | 12 | 7.80 | — | | |
| C | | | 20/10 MHz | | 6.05 | — | | |
| | | | 20/1 MHz | | 4.45 | — | | |
| | | | 20/20 MHz | 5.3 | 7.75 | — | | |
| | | | 20/10 MHz | | 6.00 | — | | |
| | | | 20/1 MHz | | 4.40 | — | | |
| | | | 20/20 MHz | 4.5 | 7.90 | — | | |
| | | | 20/10 MHz | | 6.20 | — | | |
| | | | 20/1 MHz | | 4.60 | — | | |
| C | Run supply current, FBE mode, all clock gate is on, code run from SRAM | RI _{DD} | 40/20 MHz | 18 | 11.65 | — | mA | -40 to 105 °C |
| C | | | 20/10 MHz | | 7.00 | — | | |
| | | | 20/1 MHz | | 4.60 | — | | |
| C | | | 20/20 MHz | 12 | 9.60 | — | | |
| C | | | 20/10 MHz | | 6.95 | — | | |
| | | | 20/1 MHz | | 4.55 | — | | |
| | | | 20/20 MHz | 5.3 | 9.60 | — | | |
| | | | 20/10 MHz | | 6.90 | — | | |
| | | | 20/1 MHz | | 4.50 | — | | |
| | | | 20/20 MHz | 4.5 | 9.75 | — | | |
| | | | 20/10 MHz | | 7.10 | — | | |
| | | | 20/1 MHz | | 4.70 | — | | |
| C | Wait mode current, FEI mode, all clock gate is on | WI _{DD} | 40/20 MHz | 18 | 7.80 | — | mA | -40 to 105 °C |

Table continues on the next page...

Table 3. Supply current characteristics (continued)

| C | Parameter | Symbol | Core/Bus Freq | V _{DD} (V) | Typical ¹ | Max | Unit | Temp |
|---|--|-----------------|---------------|---------------------|----------------------|-----|------|---------------|
| C | | | 20/10 MHz | | 6.05 | — | | |
| | | | 20/1 MHz | | 4.40 | — | | |
| C | | | 20/20 MHz | 12 | 7.70 | — | | |
| | | | 20/10 MHz | | 6.00 | — | | |
| | | | 20/1 MHz | | 4.40 | — | | |
| | | | 20/20 MHz | 5.3 | 7.65 | — | | |
| | | | 20/10 MHz | | 5.95 | — | | |
| | | | 20/1 MHz | | 4.35 | — | | |
| | | | 20/20 MHz | 4.5 | 7.85 | — | | |
| | | | 20/10 MHz | | 6.20 | — | | |
| | | | 20/1 MHz | | 4.60 | — | | |
| C | Stop mode supply current, no clocks active (except 20 kHz LPO clock) | I _{DD} | — | 18 | 19.85 | — | μA | -40 to 105 °C |
| C | | | | 12 | 19.05 | — | | |
| C | | | | 5.3 | 18.25 | — | | |
| C | | | | 4.5 | 17.65 | — | | |
| C | ADC adder to Stop | — | — | 18 | 88.80 | — | μA | -40 to 105 °C |
| C | ADLPC = 1 | | | 12 | 87.95 | — | | |
| C | ADLSMP = 1 | | | 5.3 | 86.70 | — | | |
| C | ADCO = 1 | | | 4.5 | 85.40 | — | | |

1. Data in Typical column was characterized at 25 °C or is typical recommended value.

2.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.1.3.1 EMC radiated emissions operating behaviors

NOTE

If using external reset switch to design hardware board, connect two 0.1 μF decoupling capacitors on $\overline{\text{RESET}}$ pin for

EMC-sensitive applications. One is near the $\overline{\text{RESET}}$ pin and the other is near the reset switch.

Table 4. EMC radiated emissions operating behaviors for 24-pin QFN package

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|---------------------|------------------------------------|----------------------|------|------|-------|
| V _{RE1} | Radiated emissions voltage, band 1 | 0.15–50 | 4 | dBμV | 1, 2 |
| V _{RE2} | Radiated emissions voltage, band 2 | 50–150 | 3 | dBμV | |
| V _{RE3} | Radiated emissions voltage, band 3 | 150–500 | 3 | dBμV | |
| V _{RE4} | Radiated emissions voltage, band 4 | 500–1000 | 4 | dBμV | |
| V _{RE_IEC} | IEC/SAE level | 0.15–1000 | O | — | 2, 3 |

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 12.0 V, T_A = 25 °C, f_{sys} = 40 MHz, f_{BUS} = 20 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2 Switching specifications

2.2.1 Control timing

Table 5. Control timing

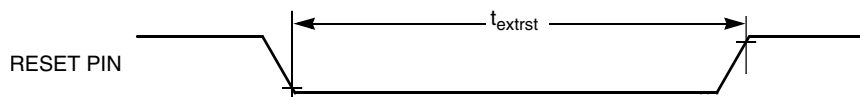
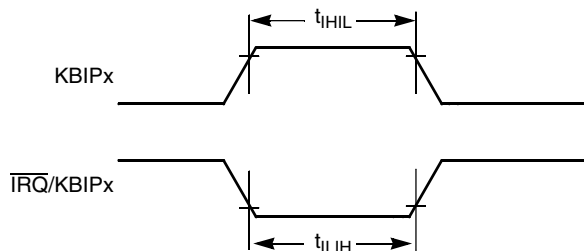
| C | Rating | | Symbol | Min | Typical ¹ | Max | Unit |
|---|--|--------------------------------|---------------------|------------------------|----------------------|-----|------|
| P | Bus frequency (t _{cyc} = 1/f _{Bus}) | | f _{Bus} | DC | — | 20 | MHz |
| P | Internal low power oscillator frequency | | f _{LPO} | 19 | 20 | 21 | KHz |
| D | External reset pulse width ² | | t _{extrst} | 100 | — | — | ns |
| D | BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes | | t _{MSSU} | 500 | — | — | ns |
| D | BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes ³ | | t _{MSH} | 100 | — | — | ns |
| D | IRQ pulse width | Asynchronous path ² | t _{LIH} | 100 | — | — | ns |
| D | | Synchronous path ⁴ | t _{IHL} | 1.5 × t _{cyc} | — | — | ns |
| D | Keyboard interrupt pulse width | Asynchronous path ² | t _{LIH} | 100 | — | — | ns |
| D | | Synchronous path | t _{IHL} | 1.5 × t _{cyc} | — | — | ns |

Table continues on the next page...

Table 5. Control timing (continued)

| C | Rating | Symbol | Min | Typical ¹ | Max | Unit |
|---|--|------------|-----|----------------------|-----|------|
| C | Port rise and fall time - Normal drive strength (HDRVE_PTXx = 0) (load = 50 pF) ⁵ | t_{Rise} | — | 10.2 | — | ns |
| C | | t_{Fall} | — | 9.5 | — | ns |
| C | Port rise and fall time - Extreme high drive strength (HDRVE_PTXx = 1) (load = 50 pF) ⁵ | t_{Rise} | — | 5.4 | — | ns |
| C | | t_{Fall} | — | 4.6 | — | ns |

1. Typical values are based on characterization data at $V_{DDX} = 5.0\text{ V}$, $25\text{ }^{\circ}\text{C}$ unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of t_{MSH} after V_{DDX} rises above V_{LVD} .
4. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
5. Timing is shown with respect to 20% V_{DDX} and 80% V_{DDX} levels. Temperature range $-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$.

**Figure 7. Reset timing****Figure 8. IRQ/KBIPx timing**

2.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

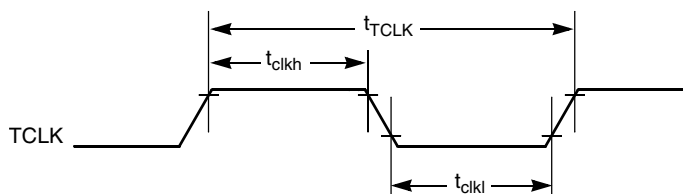
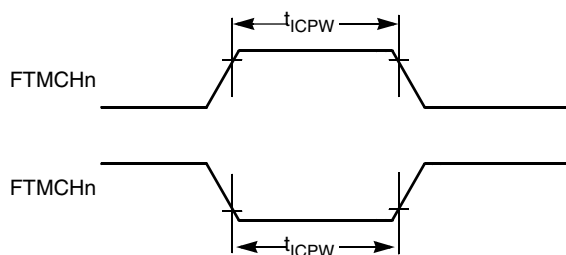
Table 6. FTM input timing

| No. | C | Function | Symbol | Min | Max | Unit |
|-----|---|--------------------------|------------|-----|-------------|-----------|
| 1 | D | External clock frequency | f_{TCLK} | 0 | $f_{Bus}/4$ | Hz |
| 2 | D | External clock period | t_{TCLK} | 4 | — | t_{cyc} |

Table continues on the next page...

Table 6. FTM input timing (continued)

| No. | C | Function | Symbol | Min | Max | Unit |
|-----|---|---------------------------|------------|-----|-----|-----------|
| 3 | D | External clock high time | t_{clkh} | 1.5 | — | t_{cyc} |
| 4 | D | External clock low time | t_{clkl} | 1.5 | — | t_{cyc} |
| 5 | D | Input capture pulse width | t_{ICPW} | 1.5 | — | t_{cyc} |

**Figure 9. Timer external clock****Figure 10. Timer input capture pulse**

2.3 Thermal specifications

2.3.1 Thermal operating requirements

Table 7. Thermal operating requirements

| Symbol | Description | Min. | Max. | Unit | Note |
|--------|--------------------------|------|------|------|------|
| T_J | Die junction temperature | −40 | 125 | °C | |
| T_A | Ambient temperature | −40 | 105 | °C | 1 |

- Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

2.3.2 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DDX} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DDX} will be very small.

Table 8. Thermal attributes

| Board type | Symbol | Description | 24-pin QFN | Unit | Notes |
|-------------------|------------------|---|------------|------|-------|
| Single-layer (1S) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 114 | °C/W | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 42 | °C/W | 1, 3 |
| Single-layer (1S) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 96 | °C/W | 1, 3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 36 | °C/W | 1, 3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 19 | °C/W | 4 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 3.4 | °C/W | 5 |
| — | Ψ_{JT} | Thermal characterization parameter, junction to package top outside center (natural convection) | 15 | °C/W | 6 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

3 Peripheral operating requirements and behaviors

3.1 ICS characteristics

Table 9. ICS specifications (temperature range = -40 to 105 °C ambient)

| C | Characteristic | | Symbol | Min | Typical ¹ | Max | Unit |
|---|---|--|---------------------|---------|----------------------|-----------|-------------|
| T | Internal reference start-up time | | t_{IRST} | — | 20 | 50 | μs |
| D | Square wave input clock frequency | FEE or FBE mode ² | f_{extal} | 0.03125 | — | 5 | MHz |
| D | | FBELP mode | | 0 | — | 40 | MHz |
| P | Average internal reference frequency - trimmed | | f_{int_t} | — | 39.0625 | — | kHz |
| P | DCO output frequency range - trimmed | | f_{dco_t} | 16 | — | 40 | MHz |
| P | Total deviation of DCO output from trimmed frequency ³ | Over full voltage and temperature range | Δf_{dco_t} | — | — | ± 2.0 | % f_{dco} |
| C | | Over fixed voltage and temperature range of 0 to 70 °C | | | | ± 1.0 | |
| C | FLL acquisition time ^{3, 4} | | $t_{Acquire}$ | — | — | 2 | ms |
| C | Long term jitter of DCO output clock (averaged over 2 ms interval) ⁵ | | C_{Jitter} | — | 0.02 | 0.2 | % f_{dco} |

1. Data in Typical column was characterized at $V_{DDX} = 5.0 V$, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. This parameter is characterized and not tested on each device.
4. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
5. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DDX} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

3.2 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash memories.

Table 10. Flash characteristics

| C | Characteristic | Symbol | Min ¹ | Typical ² | Max ³ | Unit ⁴ |
|---|----------------------------|--------------|------------------|----------------------|------------------|-------------------|
| D | NVM Bus frequency | f_{NVMBUS} | 1 | — | 20 | MHz |
| D | NVM Operating frequency | f_{NVMOP} | 0.8 | 1 | 1.05 | MHz |
| D | Erase Verify All Blocks | t_{VFYALL} | — | — | 2605 | t_{cyc} |
| D | Erase Verify Flash Block | t_{RD1BLK} | — | — | 2579 | t_{cyc} |
| D | Erase Verify Flash Section | t_{RD1SEC} | — | — | 485 | t_{cyc} |
| D | Read Once | t_{RDONCE} | — | — | 464 | t_{cyc} |

Table continues on the next page...

Table 10. Flash characteristics (continued)

| C | Characteristic | Symbol | Min ¹ | Typical ² | Max ³ | Unit ⁴ |
|---|---|----------------------|------------------|----------------------|------------------|-------------------|
| D | Program Flash (2 word) | t _{PGM2} | 0.12 | 0.13 | 0.31 | ms |
| D | Program Flash (4 word) | t _{PGM4} | 0.21 | 0.21 | 0.49 | ms |
| D | Program Once | t _{PGMONCE} | 0.20 | 0.21 | 0.21 | ms |
| D | Erase All Blocks | t _{ERSALL} | 95.42 | 100.18 | 100.30 | ms |
| D | Erase Flash Block | t _{ERSBLK} | 95.42 | 100.18 | 100.30 | ms |
| D | Erase Flash Sector | t _{ERSPG} | 19.10 | 20.05 | 20.09 | ms |
| D | Unsecure Flash | t _{UNSECU} | 95.42 | 100.19 | 100.31 | ms |
| D | Verify Backdoor Access Key | t _{VFYKEY} | — | — | 482 | t _{cyc} |
| D | Set User Margin Level | t _{MLOADU} | — | — | 415 | t _{cyc} |
| C | FLASH Program/erase endurance T _L to T _H = -40 °C to 105 °C | n _{FLPE} | 10 k | 100 k | — | Cycles |
| C | Data retention at an average junction temperature of T _{Javg} = 85°C after up to 10,000 program/erase cycles | t _{D_ret} | 15 | 100 | — | years |

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. t_{cyc} = 1 / f_{NVMBUS}

Program and erase operations do not require any special power sources other than the normal V_{DDX} supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

3.3 Analog

3.3.1 ADC characteristics

Table 11. 5 V 12-bit ADC operating conditions

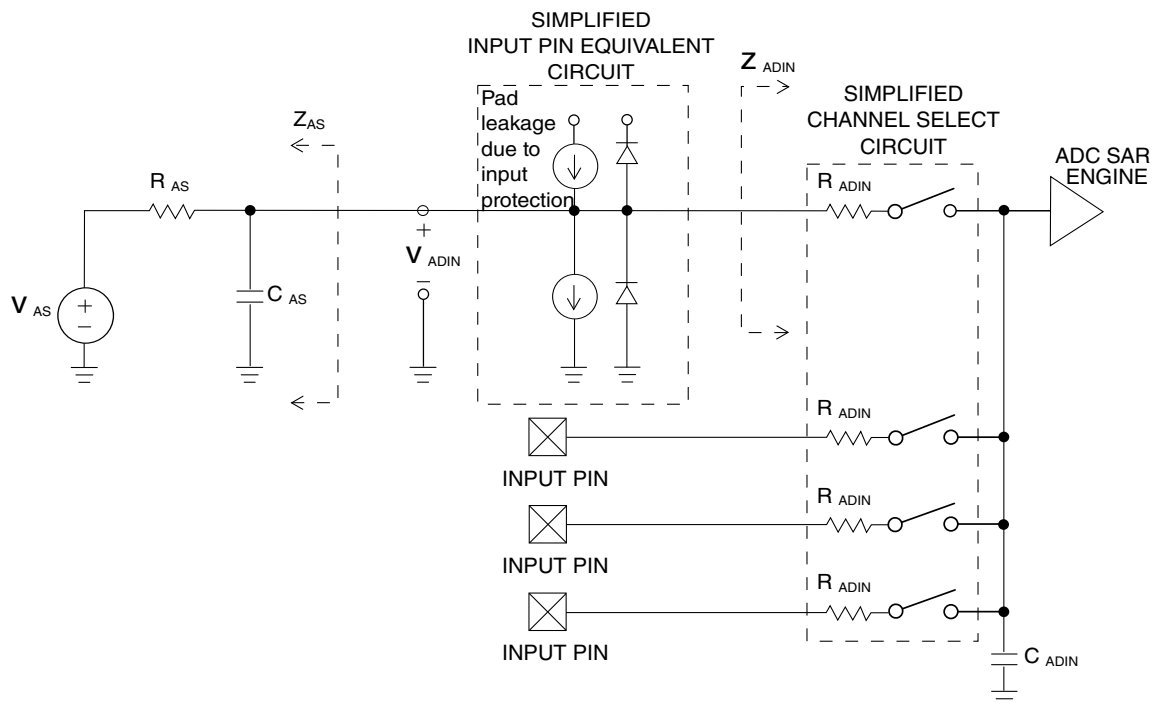
| Characteristic | Conditions | Symb | Min | Typ ¹ | Max | Unit | Comment |
|-------------------|------------|-------------------|-------------------|------------------|-------------------|------|---------|
| Input voltage | | V _{ADIN} | V _{REFL} | — | V _{REFH} | V | |
| Input capacitance | | C _{ADIN} | — | 4.5 | 5.5 | pF | |
| Input resistance | | R _{ADIN} | — | 3 | 5 | kΩ | — |

Table continues on the next page...

Table 11. 5 V 12-bit ADC operating conditions (continued)

| Characteristic | Conditions | Symb | Min | Typ ¹ | Max | Unit | Comment |
|--------------------------------|-------------------------|------------|-----|------------------|-----|------------|-----------------|
| Analog source resistance | 12-bit mode | R_{AS} | — | — | 2 | k Ω | External to MCU |
| | • $f_{ADCK} > 4$ MHz | | — | — | 5 | | |
| | • $f_{ADCK} < 4$ MHz | | — | — | 5 | | |
| | 10-bit mode | | — | — | 5 | | |
| | • $f_{ADCK} > 4$ MHz | | — | — | 10 | | |
| | • $f_{ADCK} < 4$ MHz | | — | — | 10 | | |
| | 8-bit mode | | — | — | 10 | | |
| | (all valid f_{ADCK}) | | — | — | 10 | | |
| | | | — | — | 10 | | |
| ADC conversion clock frequency | High speed (ADLPC=0) | f_{ADCK} | 0.4 | — | 8.0 | MHz | — |
| | Low power (ADLPC=1) | | 0.4 | — | 4.0 | | |

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK}=1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

**Figure 11. ADC input impedance equivalency diagram****Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)**

| Characteristic | Conditions | C | Symb | Min | Typ ¹ | Max | Unit |
|---|------------|---|-----------|-----|------------------|-----|---------|
| Supply current ADLPC = 1 ADLSMP = 1 | | T | I_{DDA} | — | 133 | — | μ A |

Table continues on the next page...

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Characteristic | Conditions | C | Symb | Min | Typ ¹ | Max | Unit |
|---|---------------------------|---|-------------|------|------------------|-----------|------------------|
| ADCO = 1 | | | | | | | |
| Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1 | | T | I_{DDA} | — | 218 | — | μA |
| Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1 | | T | I_{DDA} | — | 327 | — | μA |
| Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1 | | T | I_{DDAD} | — | 582 | 990 | μA |
| Supply current | Stop, reset, module off | T | I_{DDA} | — | 0.011 | 1 | μA |
| ADC asynchronous clock source | High speed (ADLPC = 0) | T | f_{ADACK} | 2 | 3.3 | 5 | MHz |
| | Low power (ADLPC = 1) | | | 1.25 | 2 | 3.3 | |
| Conversion time (including sample time) | Short sample (ADLSMP = 0) | T | t_{ADC} | — | 20 | — | ADCK cycles |
| | Long sample (ADLSMP = 1) | | | — | 40 | — | |
| Sample time | Short sample (ADLSMP = 0) | T | t_{ADS} | — | 3.5 | — | ADCK cycles |
| | Long sample (ADLSMP = 1) | | | — | 23.5 | — | |
| Total unadjusted Error ^{2, 3} | 12-bit mode | T | E_{TUE} | — | ± 5.5 | — | LSB ⁴ |
| | 10-bit mode | T | | — | ± 1.7 | ± 2.0 | |
| | 8-bit mode | T | | — | ± 0.9 | ± 1.0 | |
| Differential Non-Linearity ³ | 12-bit mode | T | DNL | — | 1.4 | — | LSB ⁴ |
| | 10-bit mode ⁵ | P | | — | 0.5 | — | |
| | 8-bit mode ⁵ | T | | — | 0.15 | — | |
| Integral Non-Linearity ³ | 12-bit mode | T | INL | — | 1.4 | — | LSB ⁴ |
| | 10-bit mode | T | | — | 0.5 | — | |
| | 8-bit mode | T | | — | 0.15 | — | |
| Zero-scale error ⁶ | 12-bit mode | C | E_{ZS} | — | ± 2.0 | — | LSB ⁴ |
| | 10-bit mode | T | | — | ± 0.25 | ± 1.0 | |
| | 8-bit mode | T | | — | ± 0.65 | ± 1.0 | |
| Full-scale error ⁷ | 12-bit mode | T | E_{FS} | — | ± 2.5 | — | LSB ⁴ |

Table continues on the next page...

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Characteristic | Conditions | C | Symb | Min | Typ ¹ | Max | Unit |
|----------------------------------|---------------|---|--------------|-------------------|------------------|------|------------------|
| | 10-bit mode | T | | — | ±0.5 | ±1.0 | |
| | 8-bit mode | T | | — | ±0.5 | ±1.0 | |
| Quantization error | ≤12 bit modes | D | E_Q | — | — | ±0.5 | LSB ⁴ |
| Input leakage error ⁸ | all modes | D | E_{IL} | $I_{in} * R_{AS}$ | | | mV |
| Temp sensor slope | -40°C– 25°C | D | m | — | 3.266 | — | mV/°C |
| | 25°C– 125°C | | | — | 3.638 | — | |
| Temp sensor voltage | 25°C | D | V_{TEMP25} | — | 1.36 | — | V |

1. Typical values assume $V_{DDX} = 5.0$ V, $V_{DD} \geq 5.3$ V, Temp = 25°C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. To get better ADC performance: For the application case of $V_{DD} < 5.3$ V, suggest to select V_{REFH} as ADC reference. For the application case $V_{DD} \geq 5.3$ V, suggest to select V_{DDX} as ADC reference.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
6. $V_{ADIN} = V_{SSA}$
7. $V_{ADIN} = V_{DDA}$
8. I_{in} = leakage current (refer to DC characteristics)

3.3.2 CMP and 6-bit DAC electrical specifications

Table 13. Comparator and 6-bit DAC electrical specifications

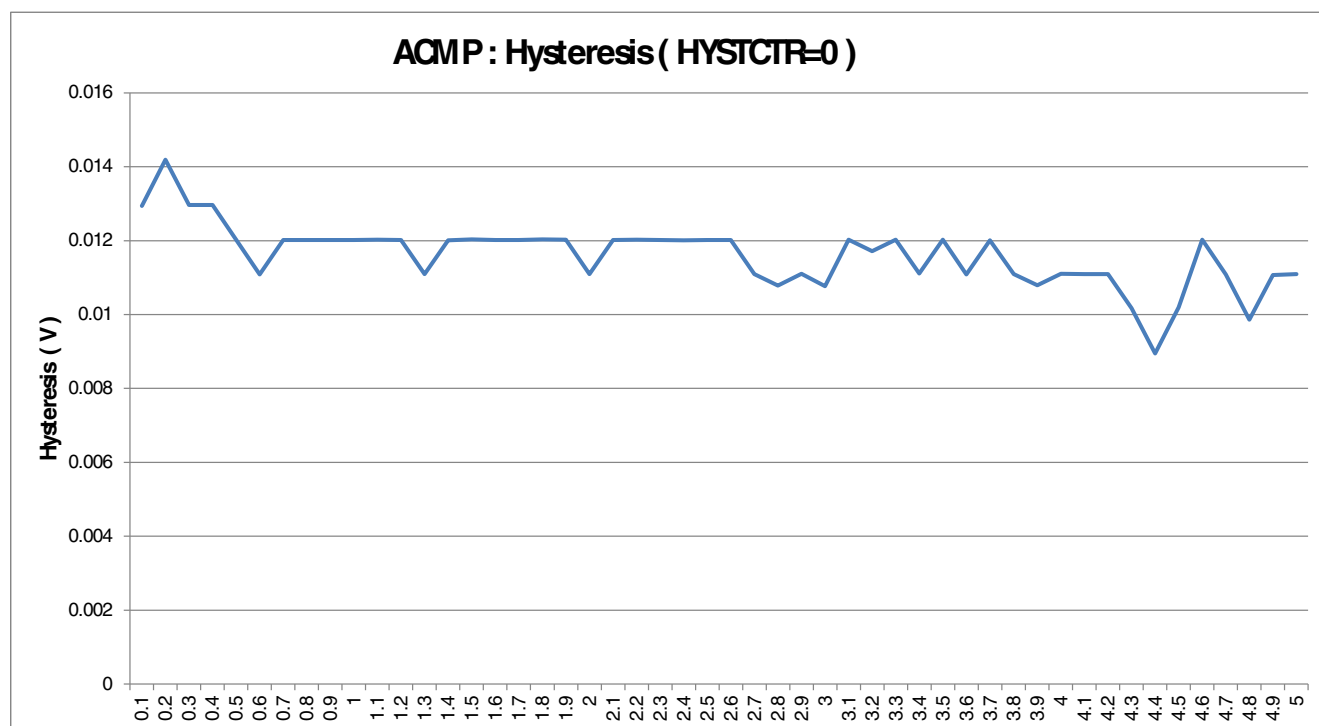
| Symbol | Description | | Min. | Typ. | Max. | Unit |
|-------------|--|----------------------|-----------------|------|-----------|------|
| V_{DDX} | Supply voltage | | 4.20 | 5.0 | 5.25 | V |
| I_{DDHS} | Supply current, high-speed mode (EN=1, PMODE=1) | | — | 100 | — | μA |
| $I_{DDL S}$ | Supply current, low-speed mode (EN=1, PMODE=0) | | — | 18 | 20 | μA |
| V_{AIN} | Analog input voltage | | $V_{SS} - 0.3$ | — | V_{DDX} | V |
| V_{AIO} | Analog input offset voltage | | — | — | 40 | mV |
| V_H | Analog comparator hysteresis | CR0[HYSTCTR] = 0 | — | 15 | 20 | mV |
| | | CR0[HYSTCTR] = 1 | — | 20 | 30 | mV |
| V_{CMPOH} | Output high | | $V_{DDX} - 0.5$ | — | — | V |
| V_{CMPOI} | Output low | | — | — | 0.5 | V |
| I_{ALKG} | Analog input leakage current | | — | — | 20 | nA |
| t_{DHS} | Propagation delay, high-speed mode (EN=1, PMODE=1) | 200 mV delta voltage | — | 70 | 120 | ns |
| | | 100 mV delta voltage | — | 100 | 150 | ns |
| | | 50 mV delta voltage | — | 200 | 250 | ns |
| t_{DLS} | Propagation delay, low-speed mode (EN=1, PMODE=0) | 200 mV delta voltage | — | 400 | 600 | ns |
| | | 100 mV delta voltage | — | 600 | 800 | ns |

Table continues on the next page...

Table 13. Comparator and 6-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------------------|---|------|------|------|------------------|
| | 50 mV delta voltage | — | 1000 | 1500 | ns |
| | Analog comparator initialization delay ¹ | — | — | 40 | μs |
| I _{DAC6b} | 6-bit DAC current adder (enabled) | — | 7 | — | μA |
| INL | 6-bit DAC integral non-linearity | −0.5 | — | 0.5 | LSB ² |
| DNL | 6-bit DAC differential non-linearity | −0.3 | — | 0.3 | LSB |

1. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
2. 1 LSB = $V_{\text{reference}}/64$

**Figure 12. Typical hysteresis vs. Vin level ($V_{DDX} = 5.0\text{ V}$, PMODE = 0)**

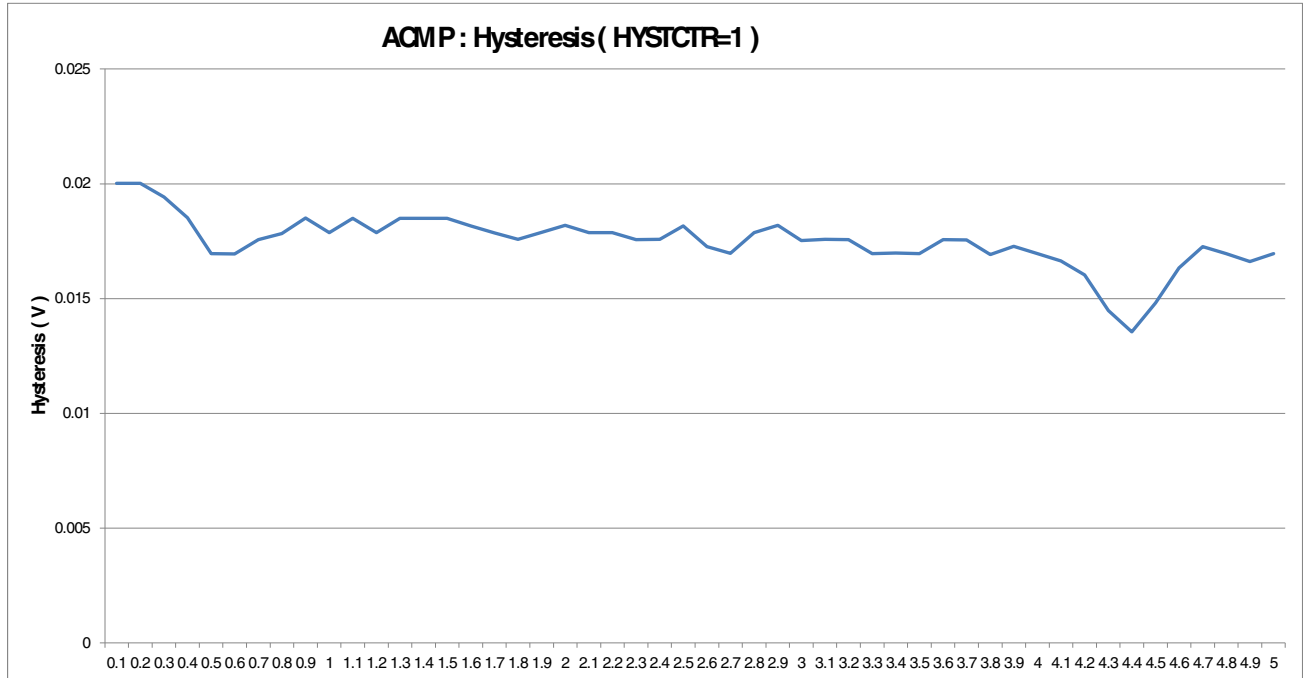


Figure 13. Typical hysteresis vs. Vin level ($V_{DDX} = 5.0\text{ V}$, PMODE = 1)

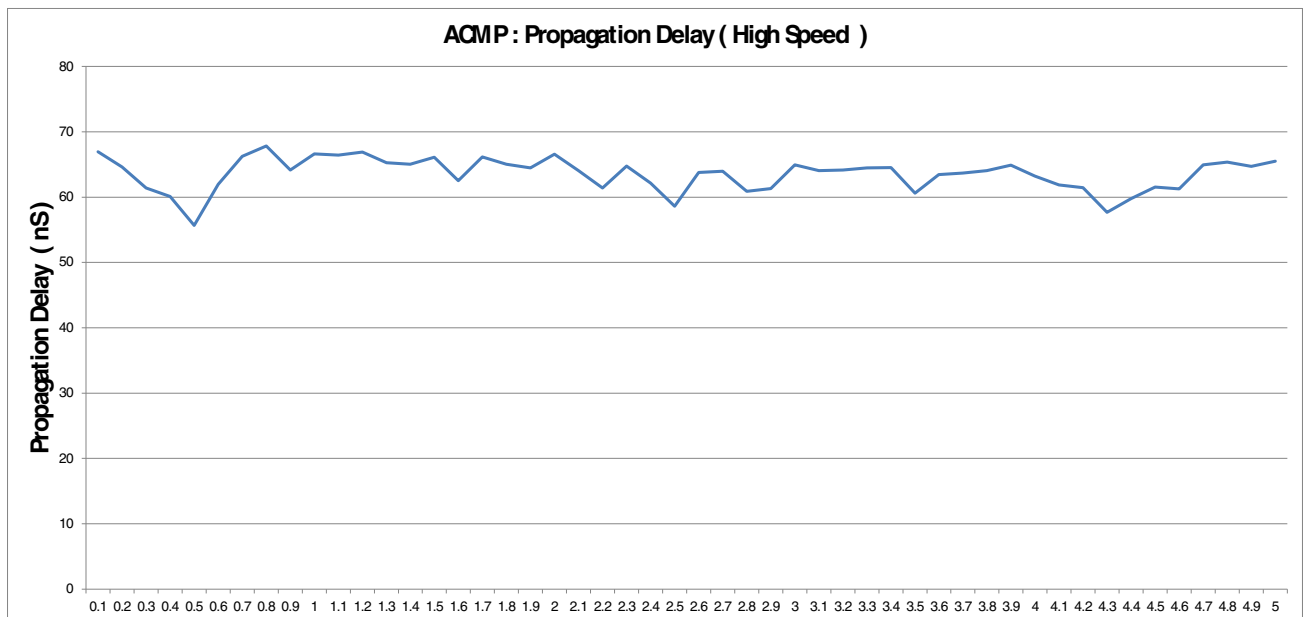


Figure 14. Typical propagation delay vs. Vin level ($V_{DDX} = 5.0\text{ V}$, high speed mode))

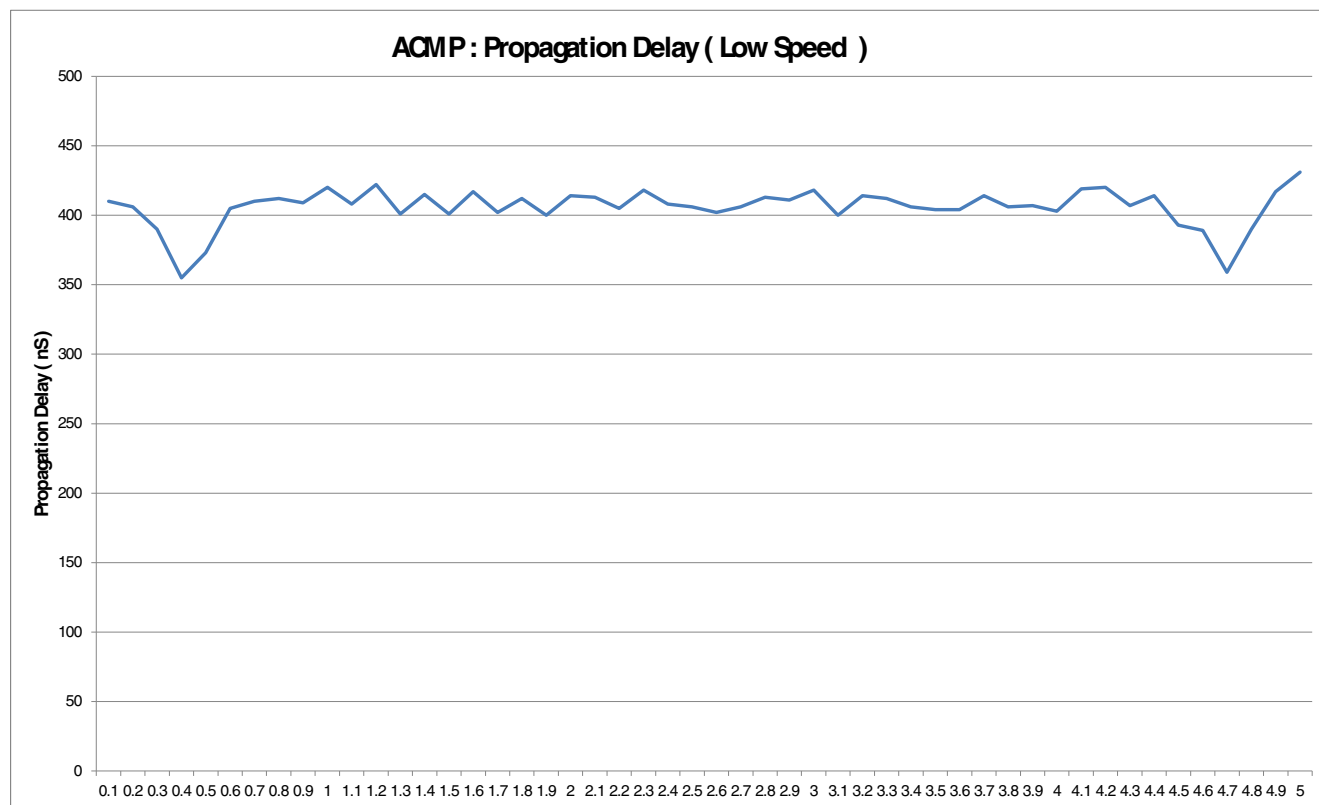


Figure 15. Typical propagation delay vs. V_{in} level ($V_{DDX}=5.0$ V, low speed mode))

3.3.3 GDU characteristics

Table 14. GDU electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Note |
|-------------|--|------------------|---------------|---------------|------------|------|
| R | Internal resistor for voltage divider | — | 17 | — | k Ω | 1 |
| R1 | PGA internal resistor 1 | — | 6.4x20 | — | k Ω | 2 |
| R2 | PGA internal resistor 2 | — | 6.4 | — | k Ω | 2 |
| V_{shant} | Current shunt resistor Delta voltage for negative and positive current sensor function | -80 | — | 80 | mV | 2 |
| V_{OH} | DC V_{OH} for HS, $V_{DDX}=5$ V, $V_{DD}=12$ V | $I_{Load}=5$ mA | $V_{DD}-570$ | $V_{DD}-301$ | — | mV |
| | | $I_{Load}=10$ mA | $V_{DD}-580$ | $V_{DD}-313$ | — | mV |
| | | $I_{Load}=15$ mA | $V_{DD}-590$ | $V_{DD}-323$ | — | mV |
| | | $I_{Load}=20$ mA | $V_{DD}-600$ | $V_{DD}-333$ | — | mV |
| | DC V_{OH} for LS, $V_{DDX}=5$ V, $V_{DD}=12$ V | $I_{Load}=5$ mA | $V_{DDX}-570$ | $V_{DDX}-360$ | — | mV |
| | | $I_{Load}=15$ mA | $V_{DDX}-580$ | $V_{DDX}-400$ | — | mV |
| | | $I_{Load}=20$ mA | $V_{DDX}-600$ | $V_{DDX}-420$ | — | mV |
| V_{OL} | DC V_{OL} for HS, $V_{DDX}=5$ V, $V_{DD}=12$ V | $I_{Load}=5$ mA | — | 295 | 570 | mV |
| | | $I_{Load}=10$ mA | — | 305 | 580 | mV |

Table continues on the next page...

Table 14. GDU electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Note |
|----------------|---|--|------|------|------|------------|
| | DC VOL for LS, $V_{DDX}=5$ V, $V_{DD}=12$ V | $I_{Load}=15$ mA | — | 317 | 590 | mV |
| | | $I_{Load}=20$ mA | — | 330 | 600 | mV |
| | | $I_{Load}=5$ mA | — | 290 | 570 | mV |
| | | $I_{Load}=15$ mA | — | 320 | 580 | mV |
| | | $I_{Load}=20$ mA | — | 335 | 600 | mV |
| I_{OH} | $V_{DDX}=5$ V, $V_{DD}=12$ V, $V_{Out}=V_{DD}-0.4$ V | DC IOH at lowest strength for HS | — | 7.45 | — | mA |
| | $V_{DDX}=5$ V, $V_{DD}=12$ V, $V_{Out}=V_{DDX}-0.4$ V | DC IOH at lowest strength for LS | — | 7.45 | — | mA |
| I_{OL} | $V_{DDX}=5$ V, $V_{DD}=12$ V, $V_{Out}=V_{clamp}+0.4$ V | DC IOL at lowest strength for HS | — | 6.45 | — | mA |
| | $V_{DDX}=5$ V, $V_{DD}=12$ V, $V_{Out}=V_{SS}+0.4$ V | DC IOL at lowest strength for LS | — | 6.45 | — | mA |
| R_{pullup} | Pullup resistor of HS predriver, gate to source of PFET | | 192 | 226 | 260 | k Ω |
| $R_{pulldown}$ | Pulldown resistor of LS predriver, gate to source of NFET | | 30 | 40 | 50 | k Ω |
| V_{clamp1} | $V_{DD}-V_{o_clamp}$ in regulation mode with 5.5 V $\leq V_{DD} \leq 18$ V, loading current is less than 10 mA | | 4.5 | 5 | 5.5 | V |
| V_{clamp2} | $V_{DD}-V_{o_clamp}$ in open loop mode with 4.5 V $\leq V_{DD} < 5.5$ V, loading current is less than 10 mA | | 4.0 | — | 5 | V |
| I_{Load} | The sink current capability | | — | — | 10 | mA |
| | Line regulation, ΔV_{clamp} over ΔV_{DD} | 4.5 V $\leq V_{DD} < 5.5$ V ³ | — | 1000 | — | mV/V |
| | | 5.5 V $\leq V_{DD} \leq 18$ V | — | 10 | — | mV/V |
| | Load regulation, ΔV_{clamp} over ΔI_{Load} | 4.5 V $\leq V_{DD} < 5.5$ V ³ | — | 25 | — | Ω |
| | | 5.5 V $\leq V_{DD} \leq 18$ V | — | 1 | — | Ω |
| OVP_22V_a | 22V over-voltage asserting threshold | | 21 | 22 | 23 | V |
| OVP_22V_d | 22V over-voltage de-asserting threshold | | 19 | 20 | 21 | V |
| OVP_22V_h | 22V over-voltage hysteresis | | 1.9 | 2 | 2.1 | V |
| OVP_24V_a | 24V over-voltage asserting threshold | | 23 | 24 | 25 | V |
| OVP_24V_d | 24V over-voltage de-asserting threshold | | 22 | 23 | 24 | V |
| OVP_24V_h | 24V over-voltage hysteresis | | 0.9 | 1 | 1.1 | V |

1. Customer need to add external resistor Rext1 for voltage divider. For example ,if Rext1=85 k Ω ,1/6 voltage divider; if Rext1=105 k Ω ,1/7 voltage divider.
2. PGA gain is default to 20X. User can cascade one external series resistor (Rext2) to reduce the PGA gain. To keep the current sensor PGA output without saturation distortion, the selected Rext2 must meet $PGA\ output = V_{REF} + (R1 / (R2 + R_{ext2})) \times V_{shunt}$, $V_{REF} = 0.5 \times V_{DDX}$, see reference manual for the R1 and R2.
3. This 5.5 V is a rough value, each part might has different value but around 5.5 V.

Table 15. GDU phase detector ACMP electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------------------|---|------------------------|------|---------------------|------|
| V _{DDX} | Supply voltage | 4.20 | 5.0 | 5.25 | V |
| I _{DDHS} | Supply current, high-speed mode (EN=1, PMODE=1) | — | 100 | — | μA |
| I _{DDL} | Supply current, low-speed mode (EN=1, PMODE=0) | — | 18 | 20 | μA |
| V _{AIN} | Analog input voltage | 0 | — | V _{DDX} -1 | V |
| V _{AIO} | Analog input offset voltage | — | — | 40 | mV |
| V _H | Analog comparator hysteresis <ul style="list-style-type: none"> CR0[HYSTCTR] = 0 CR0[HYSTCTR] = 1 | — | 15 | 20 | mV |
| | | — | 20 | 30 | mV |
| | | — | — | — | — |
| V _{CMPOH} | Output high | V _{DDX} - 0.5 | — | — | V |
| V _{CMPOI} | Output low | — | — | 0.5 | V |
| I _{ALKG} | Analog input leakage current | — | — | 20 | nA |
| t _{DHS} | Propagation delay, high-speed mode (EN=1, PMODE=1), 200mV delta voltage | — | 70 | 120 | ns |
| t _{DLS} | Propagation delay, low-speed mode (EN=1, PMODE=0), 200mV delta voltage | — | 400 | 600 | ns |
| | Analog comparator initialization delay ¹ | — | — | 40 | μs |

1. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.

Table 16. GDU over current protect ACMP electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------------------|---|------------------------|------|------------------|------------------|
| V _{DDX} | Supply voltage | 4.20 | 5.0 | 5.25 | V |
| I _{DDHS} | Supply current, high-speed mode (EN=1, PMODE=1) | — | 100 | — | μA |
| I _{DDL} | Supply current, low-speed mode (EN=1, PMODE=0) | — | 18 | 20 | μA |
| V _{AIN} | Analog input voltage | V _{SS} - 0.3 | — | V _{DDX} | V |
| V _{AIO} | Analog input offset voltage | — | 20 | 40 | mV |
| V _H | Analog comparator hysteresis <ul style="list-style-type: none"> CR0[HYSTCTR] = 0 CR0[HYSTCTR] = 1 | — | 15 | 20 | mV |
| | | — | 20 | 30 | mV |
| | | — | — | — | — |
| V _{CMPOH} | Output high | V _{DDX} - 0.5 | — | — | V |
| V _{CMPOI} | Output low | — | — | 0.5 | V |
| I _{ALKG} | Analog input leakage current | — | — | 20 | nA |
| t _{DHS} | Propagation delay, high-speed mode (EN=1, PMODE=1), 200mV delta voltage | — | 70 | 120 | ns |
| t _{DLS} | Propagation delay, low-speed mode (EN=1, PMODE=0), 200mV delta voltage ¹ | — | 400 | 600 | ns |
| | Analog comparator initialization delay ² | — | — | 40 | μs |
| INL | 6-bit DAC integral non-linearity | -0.5 | — | 0.5 | LSB ³ |

Table continues on the next page...

Table 16. GDU over current protect ACMP electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------|--------------------------------------|------|------|------|------|
| DNL | 6-bit DAC differential non-linearity | -0.3 | — | 0.3 | LSB |

1. This ACMP is used for over-current protection, customer can use low power mode to avoid sparkles. Digital filter can produce max of 12.8 μ s filter window.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{\text{reference}}/64$

3.4 Communication interfaces

3.4.1 Inter-Integrated Circuit Interface (I2C) timing

Table 17. I2C timing

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|--|-----------------------------|------------------|-------------------|----------------------------|------------------|---------|
| | | Minimum | Maximum | Minimum | Maximum | |
| SCL Clock Frequency | f_{SCL} | 0 | 100 | 0 | 400 ¹ | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{\text{HD}}; \text{STA}$ | 4 | — | 0.6 | — | μ s |
| LOW period of the SCL clock | t_{LOW} | 4.7 | — | 1.3 | — | μ s |
| HIGH period of the SCL clock | t_{HIGH} | 4 | — | 0.6 | — | μ s |
| Set-up time for a repeated START condition | $t_{\text{SU}}; \text{STA}$ | 4.7 | — | 0.6 | — | μ s |
| Data hold time for I ² C bus devices | $t_{\text{HD}}; \text{DAT}$ | 0 ² | 3.45 ³ | 0 ⁴ | 0.9 ² | μ s |
| Data set-up time | $t_{\text{SU}}; \text{DAT}$ | 250 ⁵ | — | 100 ^{3, 6} | — | ns |
| Rise time of SDA and SCL signals | t_r | — | 1000 | $20 + 0.1C_b$ ⁷ | 300 | ns |
| Fall time of SDA and SCL signals | t_f | — | 300 | $20 + 0.1C_b$ ⁶ | 300 | ns |
| Set-up time for STOP condition | $t_{\text{SU}}; \text{STO}$ | 4 | — | 0.6 | — | μ s |
| Bus free time between STOP and START condition | t_{BUF} | 4.7 | — | 1.3 | — | μ s |
| Pulse width of spikes that must be suppressed by the input filter | t_{SP} | N/A | N/A | 0 | 50 | ns |

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only achieved when using the High drive pins (see [DC characteristics](#)) or when using the Normal drive pins and $V_{\text{DDX}} \geq 2.7$ V
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum $t_{\text{HD}}; \text{DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.

Dimensions

7. C_h = total capacitance of the one bus line in pF.

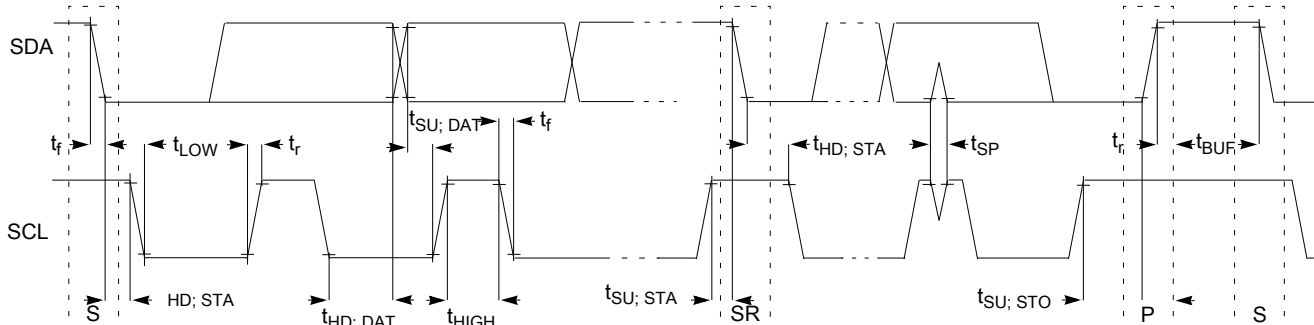


Figure 16. Timing definition for fast and standard mode devices on the I²C bus

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 24-pin QFN | 98ASA00602D |

5 Pinout

5.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 24 QFN | Pin Name | Default/ALT0 | ALT1 | ALT2 | ALT3 |
|--------|----------|--------------|------|------|------|
| 1 | PTB5 | PWM_WL | | | PTB5 |

| 24 QFN | Pin Name | Default/ALT0 | ALT1 | ALT2 | ALT3 |
|--------|----------------------|----------------------------------|------------|---------|---------------|
| 2 | PWM_UH | PWM_UH | | | |
| 3 | PWM_VH | PWM_VH | | | |
| 4 | PWM_WH | PWM_WH | | | |
| 5 | VCLAMP | VCLAMP | | | |
| 6 | VDD | VDD | | | |
| 7 | VDDX | VDDX | | | |
| 8 | VSS | VSS | | | |
| 9 | PTB6/ RESET_b | RESET_b | | TCLK | PTB6 |
| 10 | PTC0 | CMP_REF/ VREFH | PWM_FAULT0 | CLK_IN | PTC0 |
| 11 | PTB7/ BKGD/ MS | BKGD/ MS | | CLKOUT | PTB7 |
| 12 | PTA7 | PWT1 | TX | XB_OUT1 | PTA7/ KBI7 |
| 13 | PTA6 | PWT0 | RX | XB_IN1 | PTA6/ KBI6 |
| 14 | PTA5 | TX | SDA | XB_OUT0 | PTA5/ KBI5 |
| 15 | PTA4 | RX | SCL | XB_IN0 | PTA4/ KBI4 |
| 16 | PTA3 | AMP1_M/ ADC1AD1 | CLKOUT | XB_OUT1 | PTA3/ KBI3 |
| 17 | PTA2 | AMP1_P/ CMP2/ ADC1AD0 | XB_IN1 | XB_OUT0 | PTA2/ KBI2 |
| 18 | PTA1 | AMP0_M/ CMP1/ ADC0AD1 | XB_OUT0 | XB_IN1 | PTA1/ KBI1 |
| 19 | PTA0 | AMP0_P/ CMP0/ ADC0AD0 | CLK_IN | XB_IN0 | PTA0/ KBI0 |
| 20 | PTB0 | GDU_CMP0/ ADC0AD2/ ADC1AD2 | | | PTB0 |
| 21 | PTB1 | GDU_CMP1/ ADC0AD3/ ADC1AD3 | | | PTB1 |
| 22 | PTB2 | GDU_CMP2/ ADC0AD4/ ADC1AD4 | | | PTB2 |
| 23 | PTB3 | PWM_UL | | | PTB3 |
| 24 | PTB4 | PWM_VL | | | PTB4 |

5.2 Pinout

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see [Signal multiplexing and pin assignments](#).

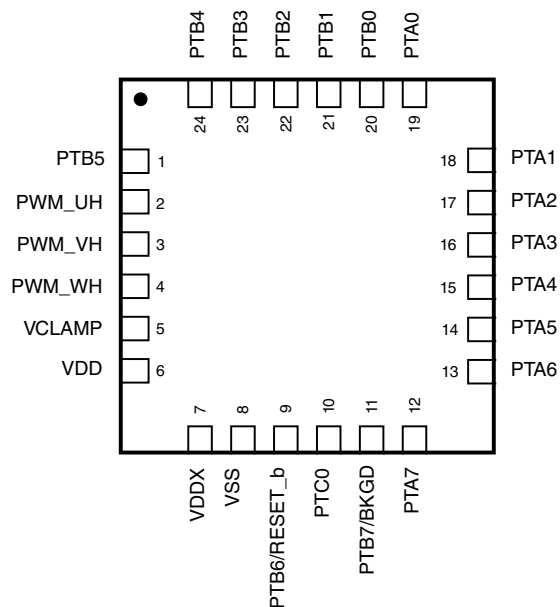


Figure 17. 24-pin QFN pinout diagram

6 Part identification

6.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

6.2 Format

Part numbers for this device have the following format:

MC 9 S08 SU AA B CC

6.3 Fields

This table lists the possible values for each field in the part number :

| Field | Description | Values |
|-------|------------------------------|---|
| MC | Qualification status | <ul style="list-style-type: none"> MC = fully qualified, general market flow |
| 9 | Memory | <ul style="list-style-type: none"> 9 = flash based |
| S08 | Core | <ul style="list-style-type: none"> S08 = 8-bit CPU |
| SU | Device family | <ul style="list-style-type: none"> SU |
| AA | Approximate flash size in KB | <ul style="list-style-type: none"> 8 = 8 KB 16 = 16 KB |
| B | Temperature range (°C) | <ul style="list-style-type: none"> V = -40 to 105 |
| CC | Package designator | <ul style="list-style-type: none"> FK = 24-pin QFN |

6.4 Example

This is an example part number:

MC9S08SU16VFK

7 Terminology and guidelines

7.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

7.1.1 Example

This is an example of an operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|----------|---------------------------|------|------|------|
| V_{DD} | 1.0 V core supply voltage | 0.9 | 1.1 | V |

7.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

7.2.1 Example

This is an example of an operating behavior:

| Symbol | Description | Min. | Max. | Unit |
|----------|--|------|------|---------|
| I_{WP} | Digital I/O weak pullup/pulldown current | 10 | 130 | μA |

7.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

7.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|--------|---------------------------------|------|------|------|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

7.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

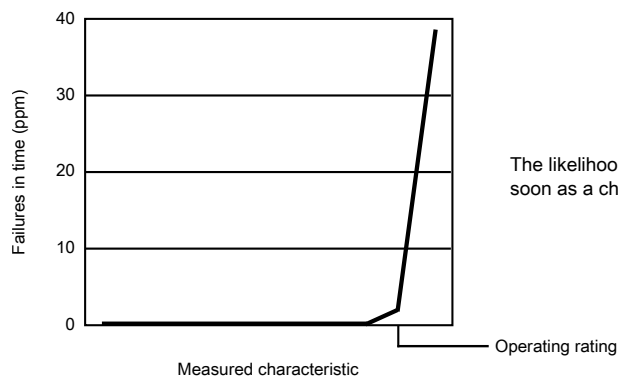
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

7.4.1 Example

This is an example of an operating rating:

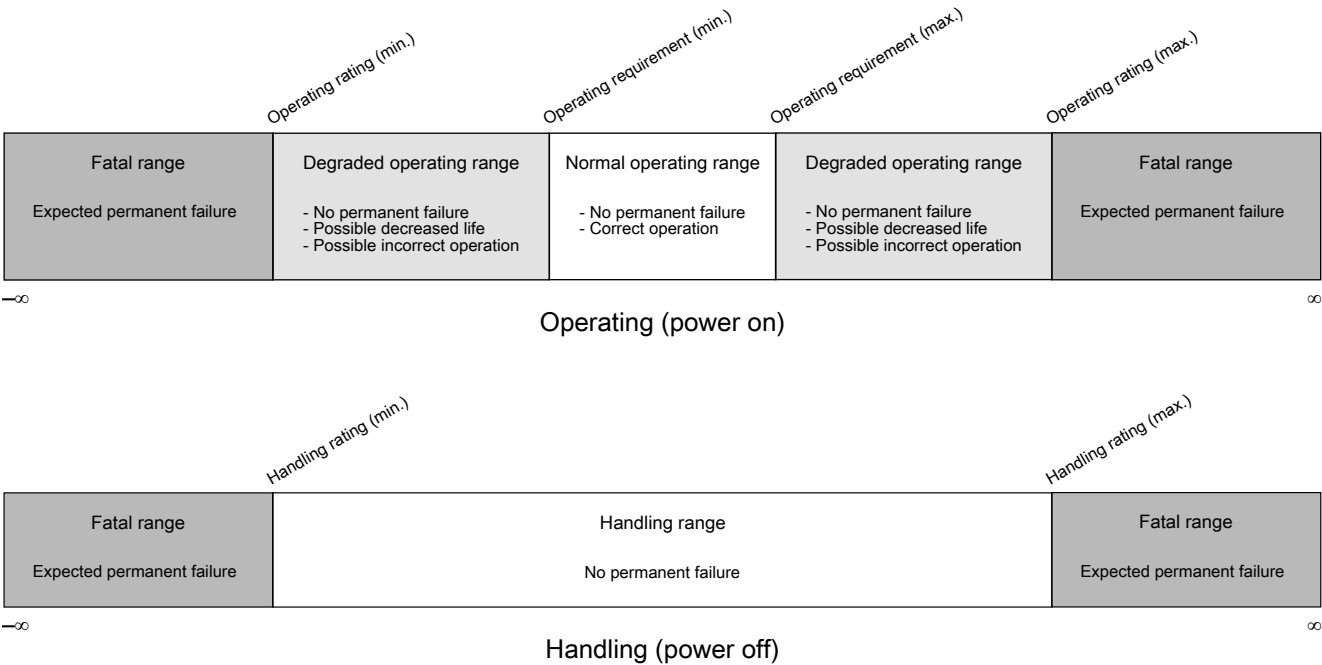
| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | −0.3 | 1.2 | V |

7.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

7.6 Relationship between ratings and operating requirements



7.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

7.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

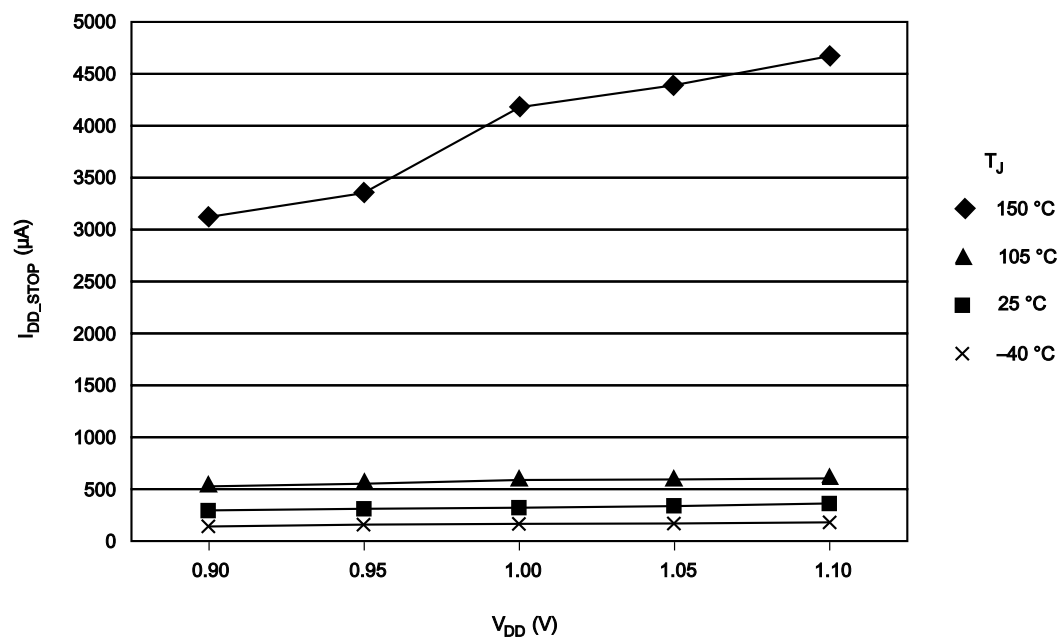
7.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|----------|--|------|------|------|---------|
| I_{WP} | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | μA |

7.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



7.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 18. Typical value conditions

| Symbol | Description | Value | Unit |
|----------|----------------------|-------|------|
| T_A | Ambient temperature | 25 | °C |
| V_{DD} | 3.3 V supply voltage | 3.3 | V |

7.10 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 19. Parameter Classifications

| | |
|---|--|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

8 Revision history

The following table provides a revision history for this document.

Table 20. Revision history

| Rev. No. | Date | Substantial Changes |
|----------|---------|--|
| 1 | 09/2016 | <ul style="list-style-type: none"> Initial public release. |
| 2 | 11/2016 | <ul style="list-style-type: none"> Added MC9S08SU8VFK part. |

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