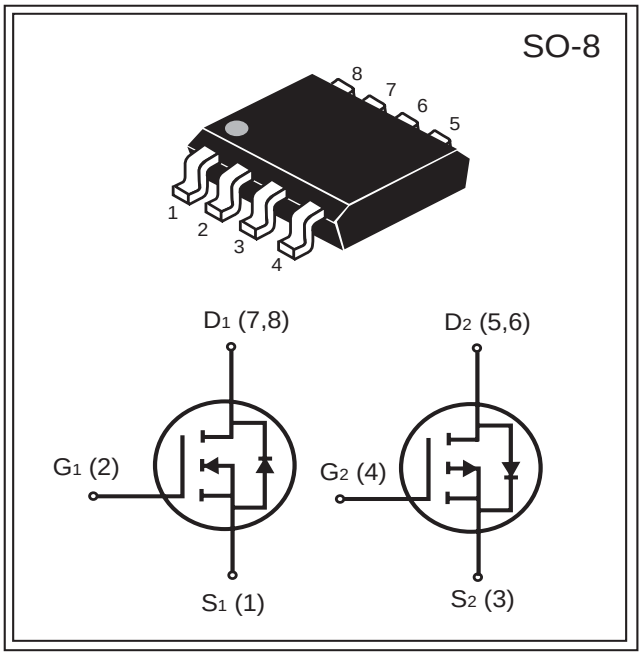
South Sea Semiconductor

SSM8402

Dual Enhancement Mode MOSFET

Product Summary (N-Channel)		
V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (mΩ) Max
30V	6.2A	32 @V_{GS} = 10V
		57 @V_{GS} = 4.5V

Product Summary (P-Channel)		
V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (mΩ) Max
-30V	-5A	45 @V_{GS} = -10V
		60 @V_{GS} = -4.5V



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
Parameter	Symbol	N-Channel Limited	P-Channel Limited	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	±20	±20	
Drain Current-Continuous @ Ta	I_D	6.2	-5	A
-Pulsed [b]	I_{DM}	25	-20	
Drain-Source Diode Forward Current [a]	I_S	1.7	-1.7	
Maximum Power Dissipation [a]	P_D	2.0		W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C
THERMAL CHRACTERISTICS				
Thermal Resistance, Junction-to-Ambient [a]	$R_{\theta JA}$	62.5		°C/W

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N-Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V			1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} I_D=250μA	1	1.7	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=9A		27	32	mΩ
		V_{GS}=4.5V, I_D=7A		52	57	
On-State Drain Current	$I_{D(ON)}$	V_{DS}=10V, V_{GS}=10V	18			A
Forward Transconductance	g_{FS}	V_{DS}=10V, I_D=5A		8		S
Input Capacitance	C_{ISS}	V_{DS}=15V V_{GS}=0V f=1.0MHz		520		pF
Output Capacitance	C_{OSS}			84		
Reverse Transfer Capacitance	C_{RSS}			60		
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=15V, I_D=1A, V_{GS}=10V, R_{GEN}=6Ω		13		ns
Rise Time	t_r			6.6		
Turn-Off Delay Time	$t_{D(OFF)}$			17		
Fall Time	t_f			9.5		
Total Gate Charge	Q_g	V_{DS}=15V, I_D=9A, V_{GS}=10V		13.5		nC
		V_{DS}=15V, I_D=9A, V_{GS}=4.5V		9.5		
Gate-Source Charge	Q_{gs}	V_{DS}=15V I_D=9A, V_{GS}=10V		2.8		
Gate-Drain Charge	Q_{gd}			3		
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_D=1.7A		0.8	1.2	V

P-Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V, V_{GS}=0V			-1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} I_D=-250μA	-1	-1.5	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-4.5A		35	45	mΩ
		V_{GS}=-4.5V, I_D=-3.6A		50	60	
On-State Drain Current	$I_{D(ON)}$	V_{DS}=-5V, V_{GS}=-10V	-15			A
Forward Transconductance	g_{FS}	V_{DS}=-5V, I_D=-5A		5		S
Input Capacitance	C_{ISS}	V_{DS}=-15V		625		pF
Output Capacitance	C_{OSS}	V_{GS}=0V		165		
Reverse Transfer Capacitance	C_{RSS}	f=1.0MHz		71		
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=-15V,		12		ns
Rise Time	t_r	R_L=15		14.4		
Turn-Off Delay Time	$t_{D(OFF)}$	V_{GS}=-10V,		77		
Fall Time	t_f	R_{GEN}=6Ω,		37		
Total Gate Charge	Q_g	V_{DS}=-15V, I_D=-5A, V_{GS}=-10V		17.5		nC
		V_{DS}=-15V, I_D=-5A, V_{GS}=-4.5V		9		
Gate-Source Charge	Q_{gs}	V_{DS}=-15V, I_D=-4.9A, V_{GS}=-10V		3.5		
Gate-Drain Charge	Q_{gd}			3		
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_D=-1.7A		-0.8	-1.2	V

Notes：

a. Surface Mounted on FR4 Board, t ≤10 sec.

b. Pulse Test：Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

c. Guaranteed by design, not subject to production testing.

N-Channel

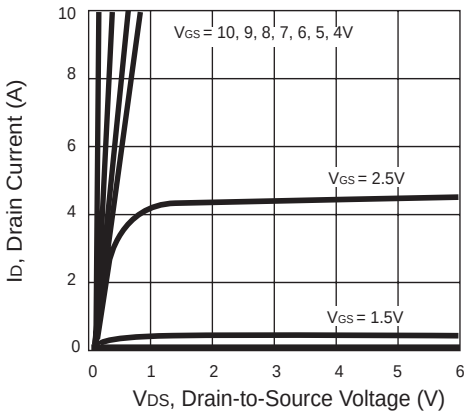


Figure 1. Output Characteristics

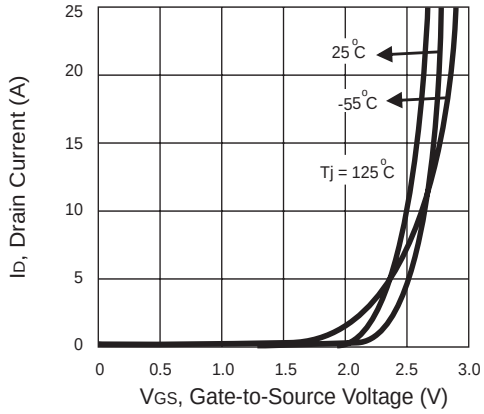


Figure 2. Thansfer Characteristics

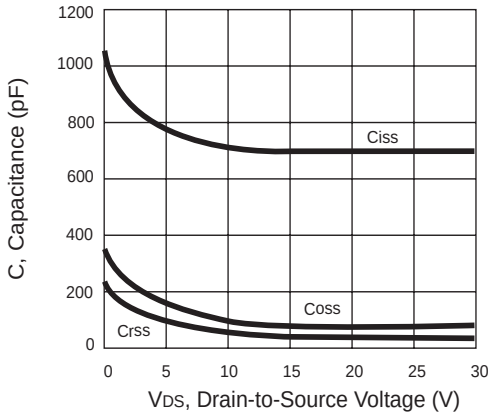
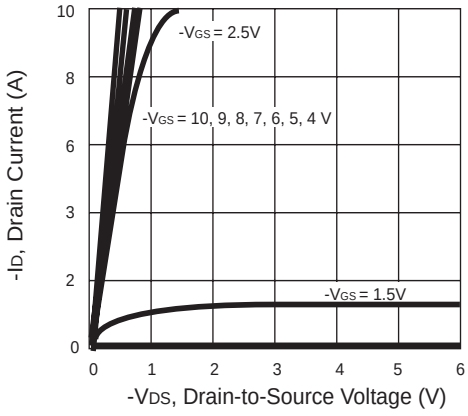


Figure 3. Capacitance

P-Channel



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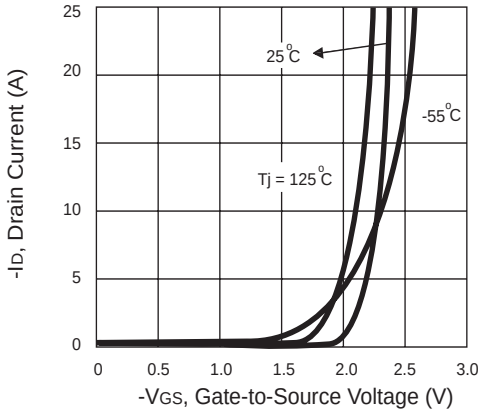
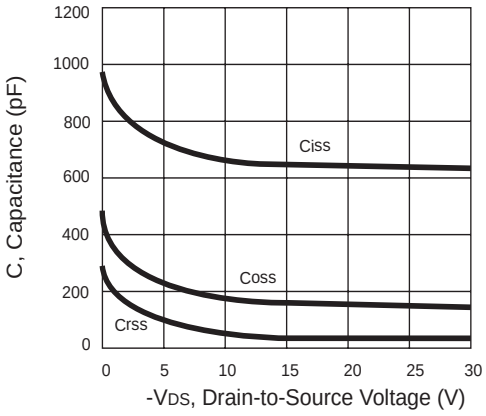


Figure 2. Thansfer Characteristics



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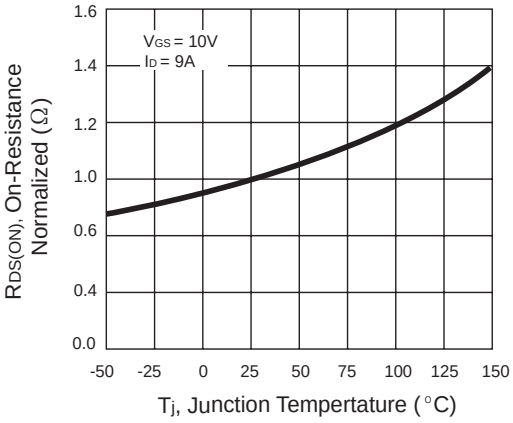


Figure 4. On-Resistance Variation with Temperature

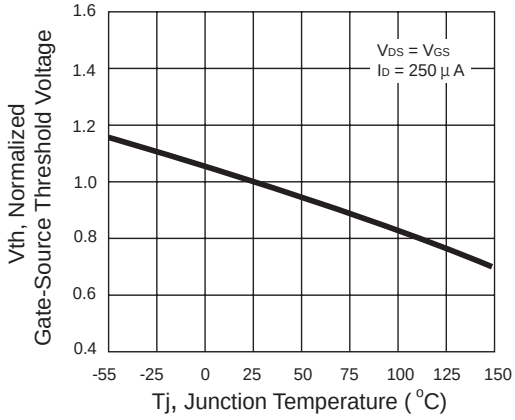


Figure 5. Gate Threshold Variation with Temperature

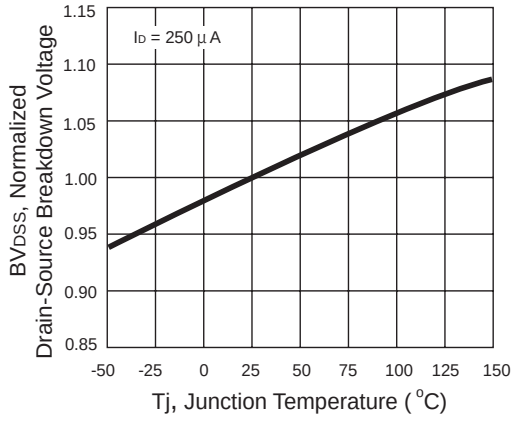
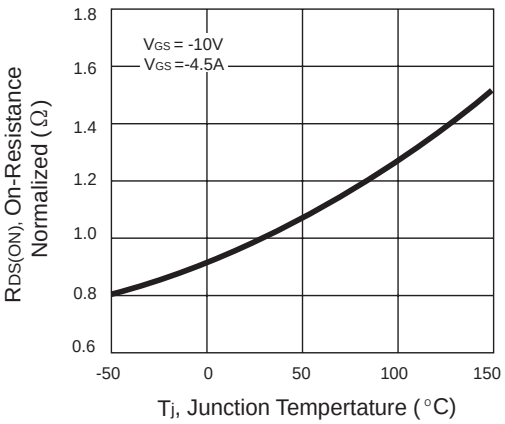


Figure 6. Breakdown Voltage Variation with Temperature

P-Channel



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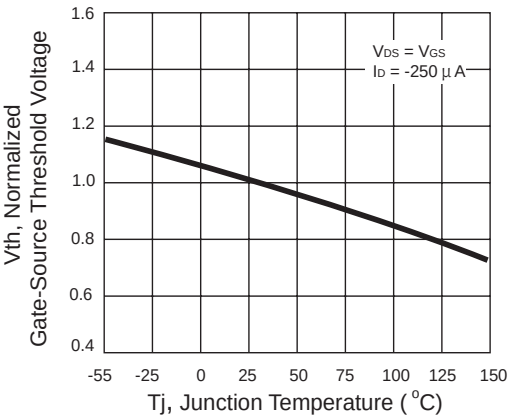

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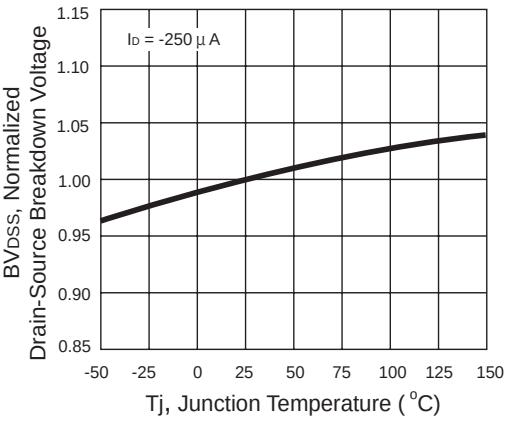

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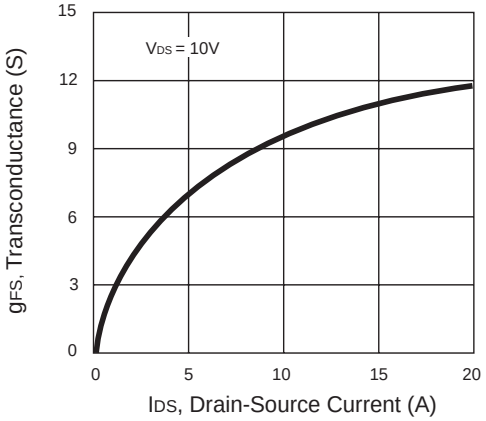


Figure 7. Transconductance Variation with Drain Current

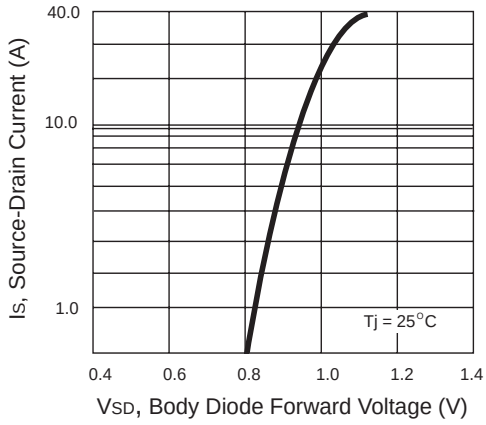


Figure 8. Body Diode Forward Voltage Variation with Source Current

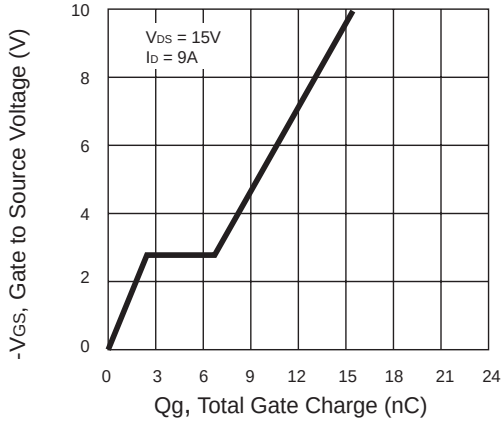
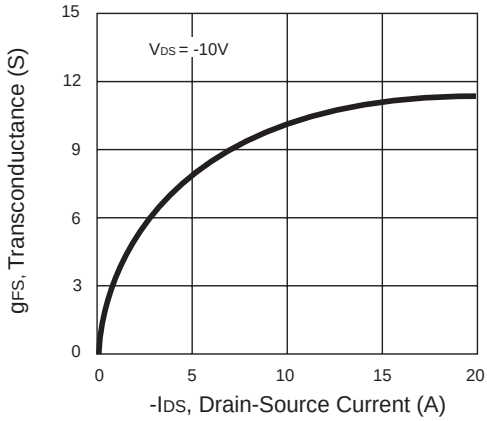


Figure 9. Gate Charge

P-Channel



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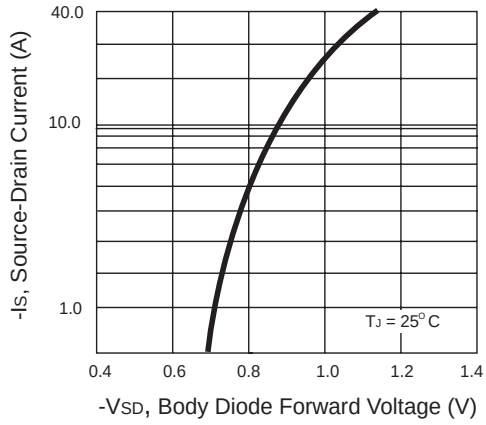

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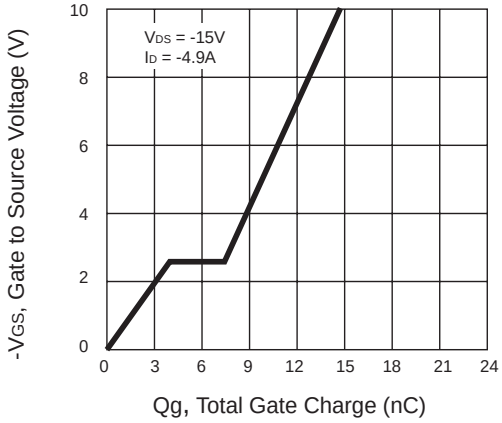

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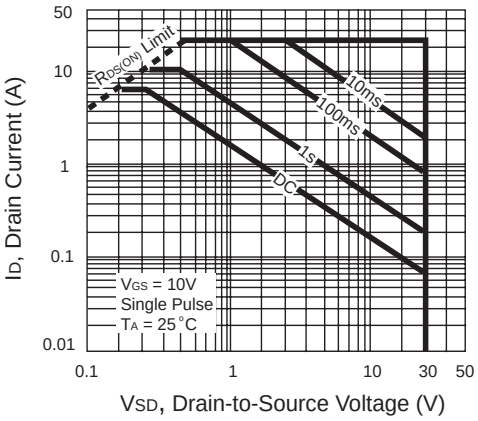
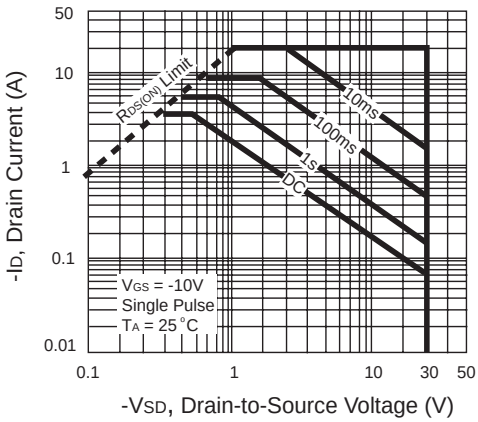


Figure 10. Maximum Safe Operating Area

P-Channel



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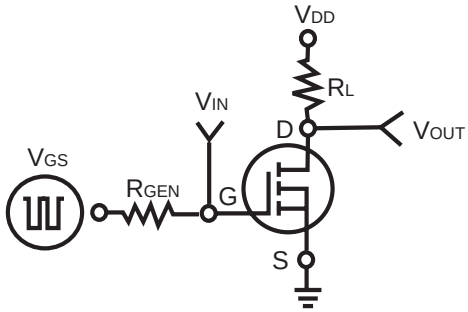


Figure 11. Switching Test Circuit

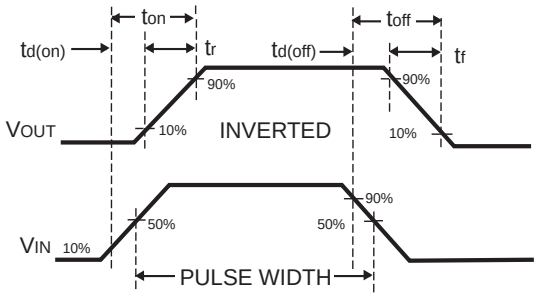


Figure 12. Switching Waveforms

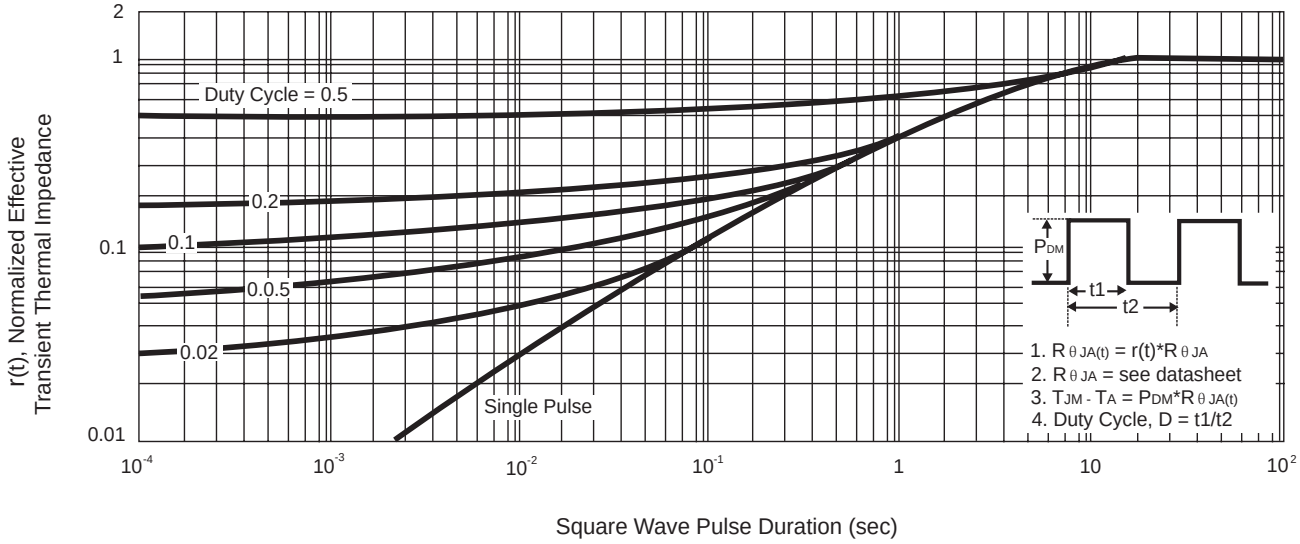
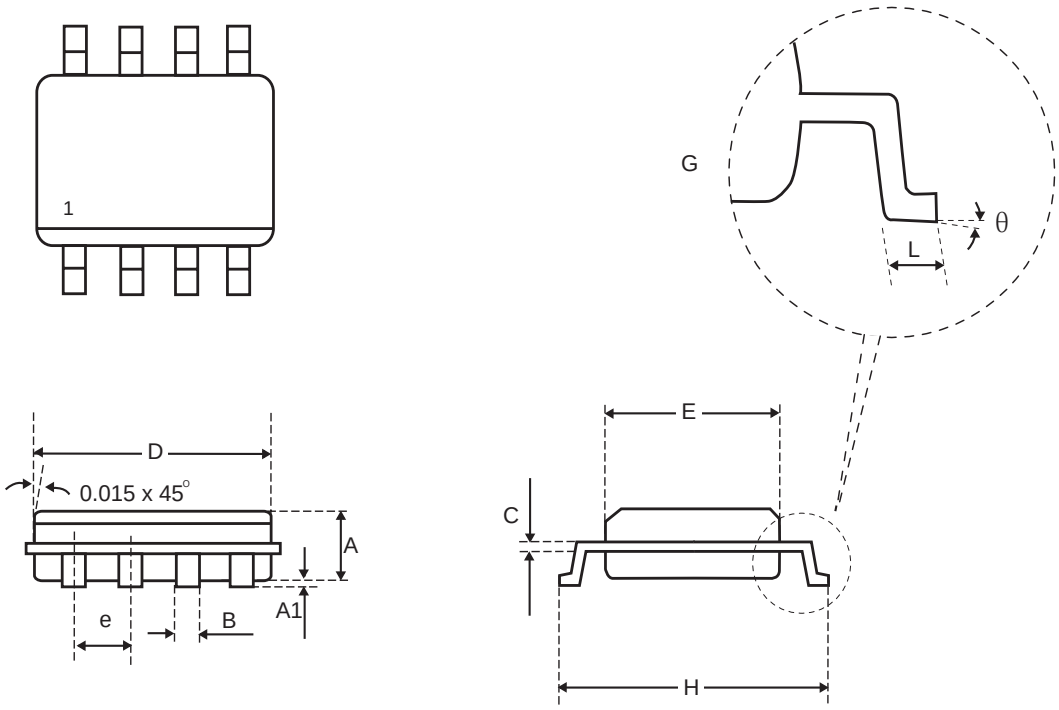


Figure 13. Normalized Thermal Transient Impedance Curve

Package Outline Dimensions

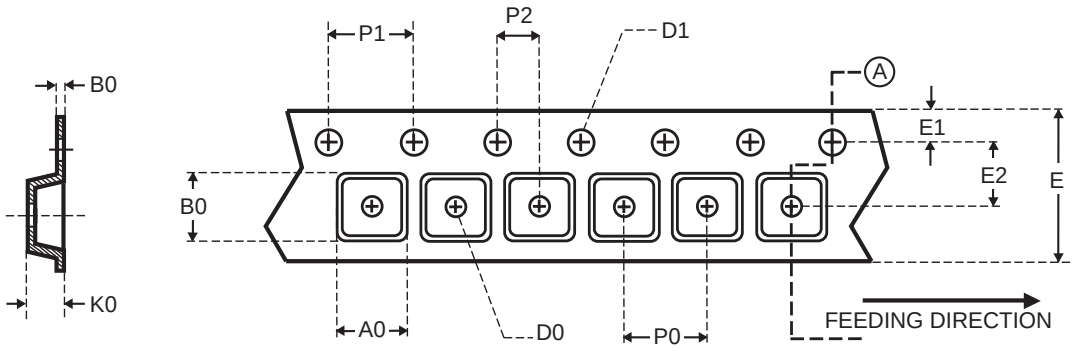
SO-8



SYMBOLS	MILLIMETERS		INCHES	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.41 Typ.		0.016 Typ.	
C	0.20 Typ.		0.008 Typ.	
D	4.80	4.98	0.189	0.196
E	3.81	3.99	0.150	0.157
e	1.25 Typ.		0.05 Typ.	
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
θ	0°	8°	0°	8°

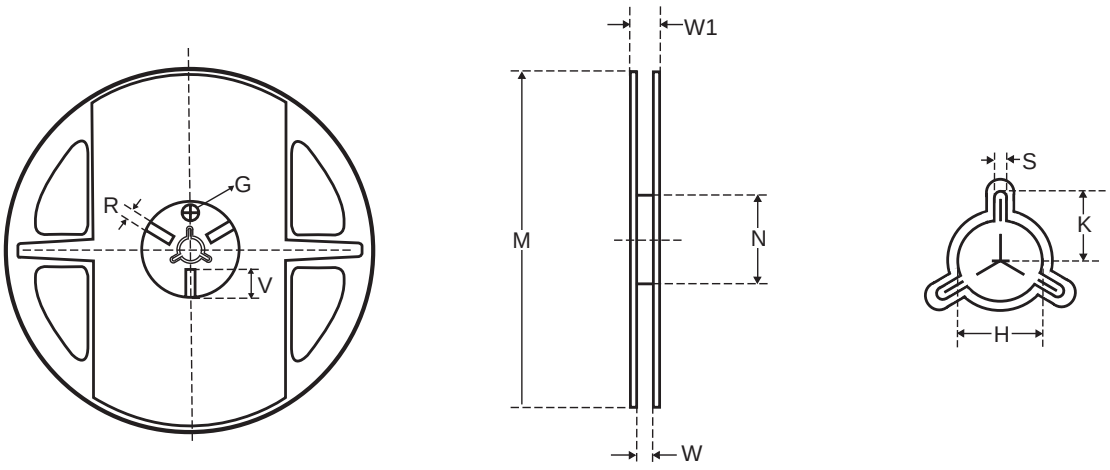
Carrier Tape & Reel Dimensions

SO-8



Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOP 8N 150 mil	6.40	5.20	2.10	ψ1.50 (Min.)	ψ1.50 +0.10 −0.10	12.00 ±0.30	1.75	5.50 ± 0.05	8.00	4.00	2.00 ± 0.05	0.30 ± 0.05

UNIT：mm



Tape size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ψ330	330 ± 1	62 ±1.5	12.4 ±0.2	16.8 −0.4	ψ12.75 ±0.15	–	2.0 ±0.15	–	–	–

UNIT：mm