

# SN54LVC574A, SN74LVC574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS301J – JANUARY 1993 – REVISED JULY 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- Power Off Disables Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)

## description

The SN54LVC574A octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V  $V_{CC}$  operation and the SN74LVC574A octal edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels at the data (D) inputs.

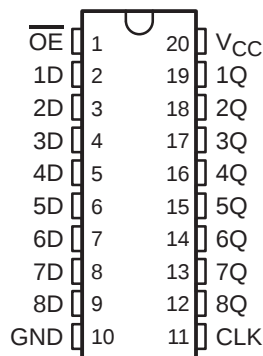
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

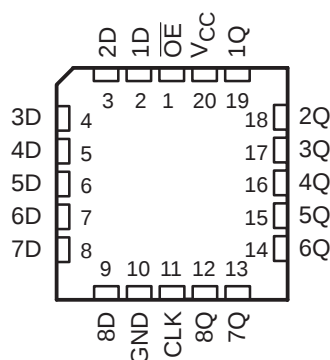
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

SN54LVC574A . . . J OR W PACKAGE  
SN74LVC574A . . . DB, DW, OR PW PACKAGE  
(TOP VIEW)



SN54LVC574A . . . FK PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54LVC574A, SN74LVC574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS301J – JANUARY 1993 – REVISED JULY 1998

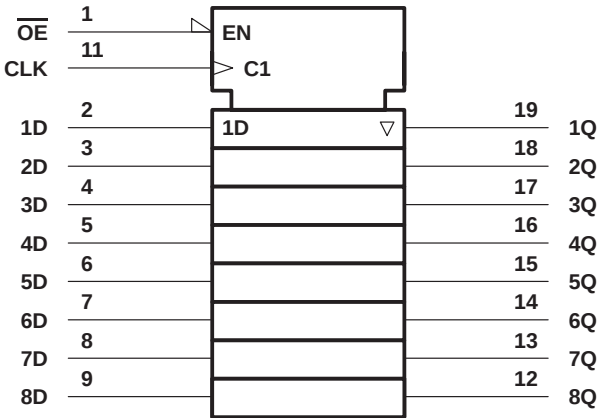
## description (continued)

The SN54LVC574A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVC574A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE  
(each flip-flop)

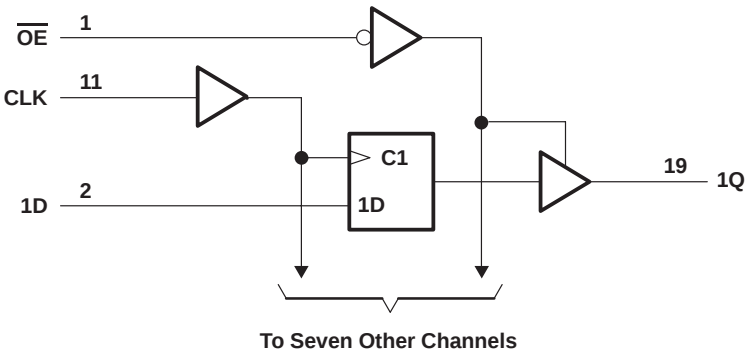
| INPUTS                 |     |   | OUTPUT<br>Q    |
|------------------------|-----|---|----------------|
| $\overline{\text{OE}}$ | CLK | D |                |
| L                      | ↑   | H | H              |
| L                      | ↑   | L | L              |
| L                      | L   | X | Q <sub>0</sub> |
| H                      | X   | X | Z              |

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



# SN54LVC574A, SN74LVC574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS301J – JANUARY 1993 – REVISED JULY 1998

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                                                     |                            |
|-----------------------------------------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$                                                                      | –0.5 V to 6.5 V            |
| Input voltage range, $V_I$ (see Note 1)                                                             | –0.5 V to 6.5 V            |
| Voltage range applied to any output in the high-impedance or power-off state, $V_O$<br>(see Note 1) | –0.5 V to 6.5 V            |
| Voltage range applied to any output in the high or low state, $V_O$<br>(see Notes 1 and 2)          | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                                                         | –50 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                                                        | –50 mA                     |
| Continuous output current, $I_O$                                                                    | ±50 mA                     |
| Continuous current through $V_{CC}$ or GND                                                          | ±100 mA                    |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package                                   | 115°C/W                    |
| DW package                                                                                          | 97°C/W                     |
| PW package                                                                                          | 128°C/W                    |
| Storage temperature range, $T_{stg}$                                                                | –65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.  
3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 4)

|                                                        |                               |  | SN54LVC574A |          | SN74LVC574A          |          | UNIT |
|--------------------------------------------------------|-------------------------------|--|-------------|----------|----------------------|----------|------|
|                                                        |                               |  | MIN         | MAX      | MIN                  | MAX      |      |
| $V_{CC}$ Supply voltage                                | Operating                     |  | 2           | 3.6      | 1.65                 | 3.6      | V    |
|                                                        | Data retention only           |  | 1.5         |          | 1.5                  |          |      |
| $V_{IH}$ High-level input voltage                      | $V_{CC} = 1.65$ V to $1.95$ V |  |             |          | $0.65 \times V_{CC}$ |          | V    |
|                                                        | $V_{CC} = 2.3$ V to $2.7$ V   |  |             |          | 1.7                  |          |      |
|                                                        | $V_{CC} = 2.7$ V to $3.6$ V   |  | 2           |          | 2                    |          |      |
| $V_{IL}$ Low-level input voltage                       | $V_{CC} = 1.65$ V to $1.95$ V |  |             |          | $0.35 \times V_{CC}$ |          | V    |
|                                                        | $V_{CC} = 2.3$ V to $2.7$ V   |  |             |          | 0.7                  |          |      |
|                                                        | $V_{CC} = 2.7$ V to $3.6$ V   |  |             | 0.8      | 0.8                  |          |      |
| $V_I$ Input voltage                                    |                               |  | 0           | 5.5      | 0                    | 5.5      | V    |
| $V_O$ Output voltage                                   | High or low state             |  | 0           | $V_{CC}$ | 0                    | $V_{CC}$ | V    |
|                                                        | 3 state                       |  | 0           | 5.5      | 0                    | 5.5      |      |
| $I_{OH}$ High-level output current                     | $V_{CC} = 1.65$ V             |  |             |          | –4                   |          | mA   |
|                                                        | $V_{CC} = 2.3$ V              |  |             |          | –8                   |          |      |
|                                                        | $V_{CC} = 2.7$ V              |  |             | –12      | –12                  |          |      |
|                                                        | $V_{CC} = 3$ V                |  |             | –24      | –24                  |          |      |
| $I_{OL}$ Low-level output current                      | $V_{CC} = 1.65$ V             |  |             |          | 4                    |          | mA   |
|                                                        | $V_{CC} = 2.3$ V              |  |             |          | 8                    |          |      |
|                                                        | $V_{CC} = 2.7$ V              |  |             | 12       | 12                   |          |      |
|                                                        | $V_{CC} = 3$ V                |  |             | 24       | 24                   |          |      |
| $\Delta t/\Delta v$ Input transition rise or fall rate |                               |  | 0           | 6        | 0                    | 6        | ns/V |
| $T_A$ Operating free-air temperature                   |                               |  | –55         | 125      | –40                  | 85       | °C   |

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54LVC574A, SN74LVC574A

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

SCAS301J – JANUARY 1993 – REVISED JULY 1998

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER        | TEST CONDITIONS                                                                 |                             | V <sub>CC</sub> | SN54LVC574A          |      |     | SN74LVC574A          |      |     | UNIT |
|------------------|---------------------------------------------------------------------------------|-----------------------------|-----------------|----------------------|------|-----|----------------------|------|-----|------|
|                  |                                                                                 |                             |                 | MIN                  | TYP† | MAX | MIN                  | TYP† | MAX |      |
| V <sub>OH</sub>  | I <sub>OH</sub> = –100 μA                                                       |                             | 1.65 V to 3.6 V |                      |      |     | V <sub>CC</sub> –0.2 |      |     | V    |
|                  |                                                                                 |                             | 2.7 V to 3.6 V  | V <sub>CC</sub> –0.2 |      |     |                      |      |     |      |
|                  | I <sub>OH</sub> = –4 mA                                                         |                             | 1.65 V          |                      |      |     | 1.2                  |      |     |      |
|                  | I <sub>OH</sub> = –8 mA                                                         |                             | 2.3 V           |                      |      |     | 1.7                  |      |     |      |
|                  | I <sub>OH</sub> = –12 mA                                                        |                             | 2.7 V           | 2.2                  |      |     | 2.2                  |      |     |      |
|                  |                                                                                 |                             | 3 V             | 2.4                  |      |     | 2.4                  |      |     |      |
|                  | I <sub>OH</sub> = –24 mA                                                        |                             | 3 V             | 2.2                  |      |     | 2.2                  |      |     |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 μA                                                        |                             | 1.65 V to 3.6 V |                      |      |     | 0.2                  |      |     | V    |
|                  |                                                                                 |                             | 2.7 V to 3.6 V  | 0.2                  |      |     |                      |      |     |      |
|                  | I <sub>OL</sub> = 4 mA                                                          |                             | 1.65 V          |                      |      |     | 0.45                 |      |     |      |
|                  | I <sub>OL</sub> = 8 mA                                                          |                             | 2.3 V           |                      |      |     | 0.7                  |      |     |      |
|                  | I <sub>OL</sub> = 12 mA                                                         |                             | 2.7 V           | 0.4                  |      |     | 0.4                  |      |     |      |
|                  | I <sub>OL</sub> = 24 mA                                                         |                             | 3 V             | 0.55                 |      |     | 0.55                 |      |     |      |
|                  | I <sub>I</sub>                                                                  | V <sub>I</sub> = 0 to 5.5 V |                 | 3.6 V                | ±5   |     |                      | ±5   |     |      |
| I <sub>off</sub> | V <sub>I</sub> or V <sub>O</sub> = 5.5 V                                        |                             | 0               |                      |      |     | ±10                  |      |     | μA   |
| I <sub>OZ</sub>  | V <sub>O</sub> = 0 to 5.5 V                                                     |                             | 3.6 V           | ±15                  |      |     | ±10                  |      |     | μA   |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                                         |                             | 3.6 V           | 10                   |      |     | 10                   |      |     | μA   |
|                  | 3.6 V ≤ V <sub>I</sub> ≤ 5.5 V‡                                                 |                             |                 | 10                   |      |     | 10                   |      |     |      |
| ΔI <sub>CC</sub> | One input at V <sub>CC</sub> – 0.6 V,<br>Other inputs at V <sub>CC</sub> or GND |                             | 2.7 V to 3.6 V  | 500                  |      |     | 500                  |      |     | μA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                         |                             | 3.3 V           | 4                    |      |     | 4                    |      |     | pF   |
| C <sub>o</sub>   | V <sub>O</sub> = V <sub>CC</sub> or GND                                         |                             | 3.3 V           | 5.5                  |      |     | 5.5                  |      |     | pF   |

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This applies in the disabled state only.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)**

|                    |                                 | SN54LVC574A             |     |                                    |     | UNIT |
|--------------------|---------------------------------|-------------------------|-----|------------------------------------|-----|------|
|                    |                                 | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     |      |
|                    |                                 | MIN                     | MAX | MIN                                | MAX |      |
| f <sub>clock</sub> | Clock frequency                 | 150                     |     | 150                                |     | MHz  |
| t <sub>W</sub>     | Pulse duration, CLK high or low | 3.3                     |     | 3.3                                |     | ns   |
| t <sub>SU</sub>    | Setup time, data before CLK↑    | 2                       |     | 2                                  |     | ns   |
| t <sub>H</sub>     | Hold time, data after CLK↑      | 2                       |     | 2                                  |     | ns   |



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54LVC574A, SN74LVC574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS301J – JANUARY 1993 – REVISED JULY 1998

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

|                    |                                 | SN74LVC574A                         |     |                                    |     |                         |     |                                    |     | UNIT |
|--------------------|---------------------------------|-------------------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
|                    |                                 | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |     | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     |      |
|                    |                                 | MIN                                 | MAX | MIN                                | MAX | MIN                     | MAX | MIN                                | MAX |      |
| f <sub>clock</sub> | Clock frequency                 | †                                   |     | †                                  |     | 150                     |     | 150                                |     | MHz  |
| t <sub>w</sub>     | Pulse duration, CLK high or low | †                                   |     | †                                  |     | 3.3                     |     | 3.3                                |     | ns   |
| t <sub>su</sub>    | Setup time, data before CLK↑    | †                                   |     | †                                  |     | 2                       |     | 2                                  |     | ns   |
| t <sub>h</sub>     | Hold time, data after CLK↑      | †                                   |     | †                                  |     | 1.5                     |     | 1.5                                |     | ns   |

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER        | FROM<br>(INPUT)        | TO<br>(OUTPUT) | SN54LVC574A             |     |                                    |     | UNIT |
|------------------|------------------------|----------------|-------------------------|-----|------------------------------------|-----|------|
|                  |                        |                | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     |      |
|                  |                        |                | MIN                     | MAX | MIN                                | MAX |      |
| f <sub>max</sub> |                        |                | 150                     |     | 150                                |     | MHz  |
| t <sub>pd</sub>  | CLK                    | Q              | 8                       |     | 1                                  | 7   | ns   |
| t <sub>en</sub>  | $\overline{\text{OE}}$ | Q              | 9                       |     | 1                                  | 7.5 | ns   |
| t <sub>djs</sub> | $\overline{\text{OE}}$ | Q              | 7                       |     | 0.5                                | 6.4 | ns   |

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

| PARAMETER                       | FROM<br>(INPUT)        | TO<br>(OUTPUT) | SN74LVC574A                         |     |                                    |     |                         |     |                                    |     | UNIT |
|---------------------------------|------------------------|----------------|-------------------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
|                                 |                        |                | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |     | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     |      |
|                                 |                        |                | MIN                                 | MAX | MIN                                | MAX | MIN                     | MAX | MIN                                | MAX |      |
| f <sub>max</sub>                |                        |                | †                                   |     | †                                  |     | 150                     |     | 150                                |     | MHz  |
| t <sub>pd</sub>                 | CLK                    | Q              | †                                   | †   | †                                  | †   | 8                       |     | 2.2                                | 7   | ns   |
| t <sub>en</sub>                 | $\overline{\text{OE}}$ | Q              | †                                   | †   | †                                  | †   | 8.5                     |     | 1.5                                | 7.5 | ns   |
| t <sub>dis</sub>                | $\overline{\text{OE}}$ | Q              | †                                   | †   | †                                  | †   | 7                       |     | 1.7                                | 6.4 | ns   |
| t <sub>sk(0)</sub> <sup>‡</sup> |                        |                |                                     |     |                                    |     |                         |     | 1                                  |     | ns   |

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics,  $T_A = 25^\circ\text{C}$

| PARAMETER       |                                                |                  | TEST<br>CONDITIONS  | $V_{CC} = 1.8\text{ V}$<br>$\pm 0.15\text{ V}$ | $V_{CC} = 2.5\text{ V}$<br>$\pm 0.2\text{ V}$ | $V_{CC} = 3.3\text{ V}$<br>$\pm 0.3\text{ V}$ | UNIT |
|-----------------|------------------------------------------------|------------------|---------------------|------------------------------------------------|-----------------------------------------------|-----------------------------------------------|------|
|                 |                                                |                  |                     | TYP                                            | TYP                                           | TYP                                           |      |
| $C_{\text{pd}}$ | Power dissipation capacitance<br>per flip-flop | Outputs enabled  | $f = 10\text{ MHz}$ | †                                              | †                                             | 43                                            | pF   |
|                 |                                                | Outputs disabled |                     | †                                              | †                                             | 15                                            |      |

† This information was not available at the time of publication.



# SN54LVC574A, SN74LVC574A

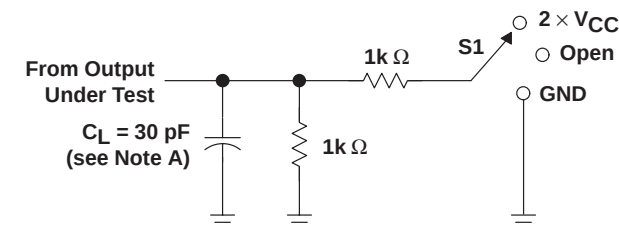
## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

SCAS301J – JANUARY 1993 – REVISED JULY 1998

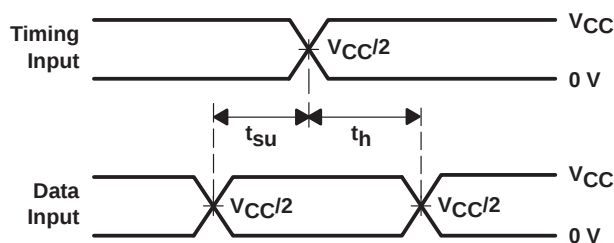
#### PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

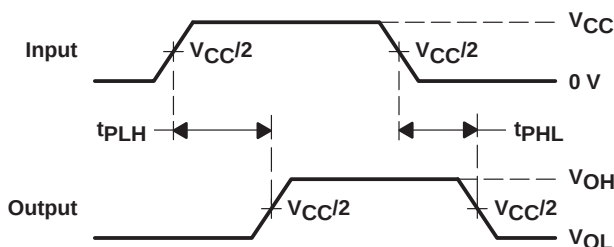


LOAD CIRCUIT

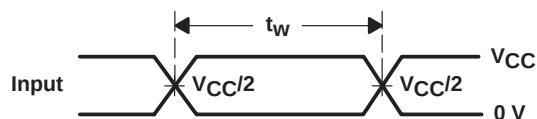
| TEST              | S1                |
|-------------------|-------------------|
| $t_{pd}$          | Open              |
| $t_{PLZ}/t_{PZL}$ | 2 $\times V_{CC}$ |
| $t_{PHZ}/t_{PHZ}$ | Open              |



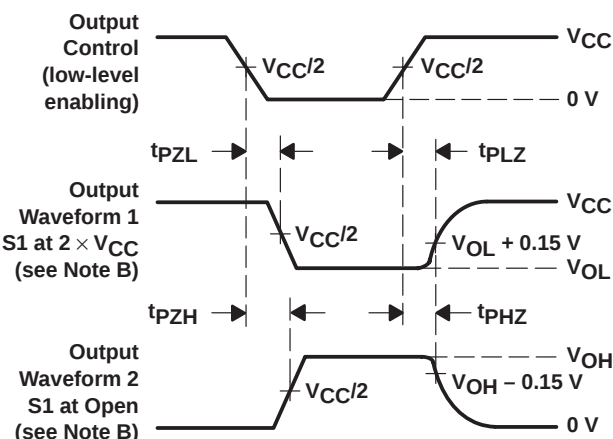
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

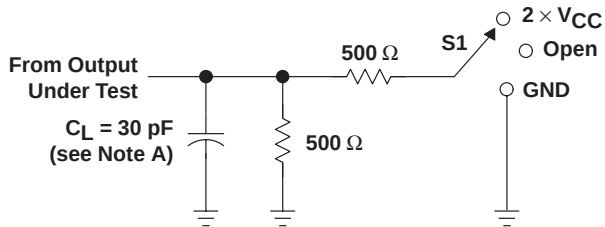
Figure 1. Load Circuit and Voltage Waveforms

# SN54LVC574A, SN74LVC574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS301J – JANUARY 1993 – REVISED JULY 1998

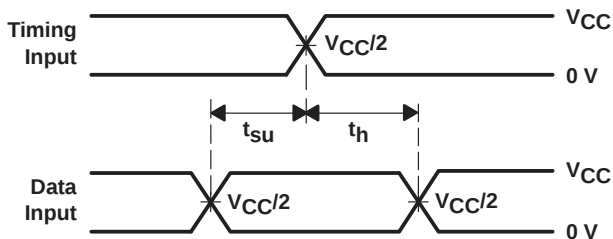
## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

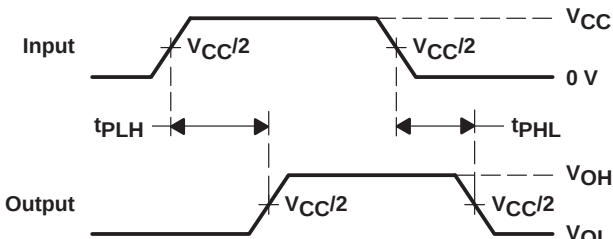


LOAD CIRCUIT

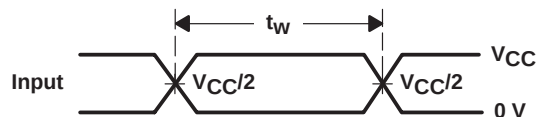
| TEST              | S1                |
|-------------------|-------------------|
| $t_{pd}$          | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |



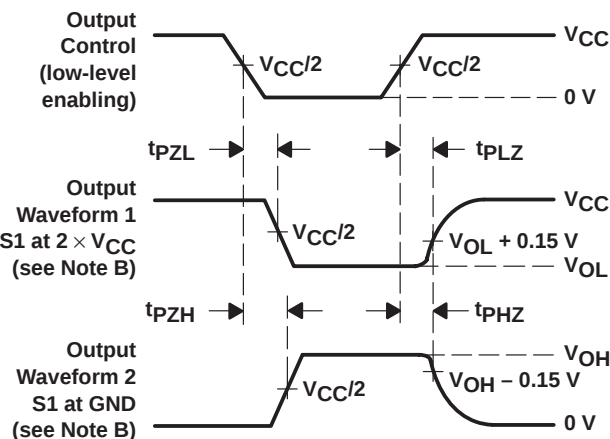
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

# SN54LVC574A, SN74LVC574A

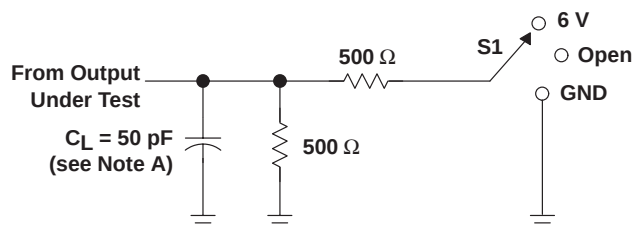
## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

SCAS301J – JANUARY 1993 – REVISED JULY 1998

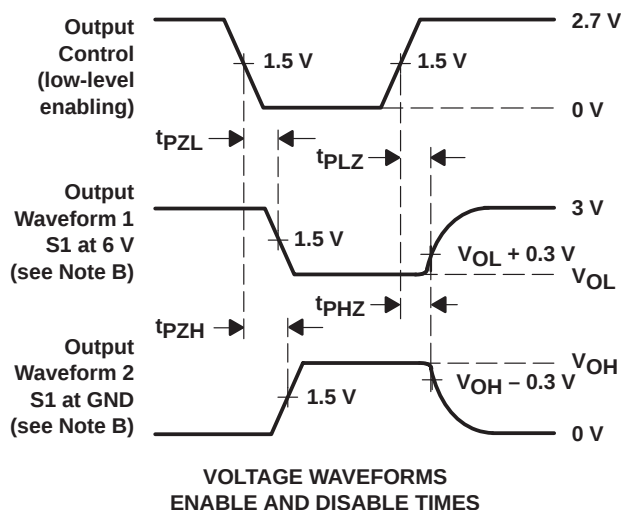
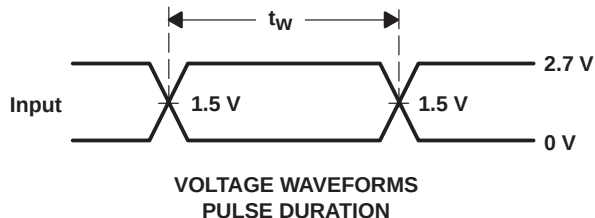
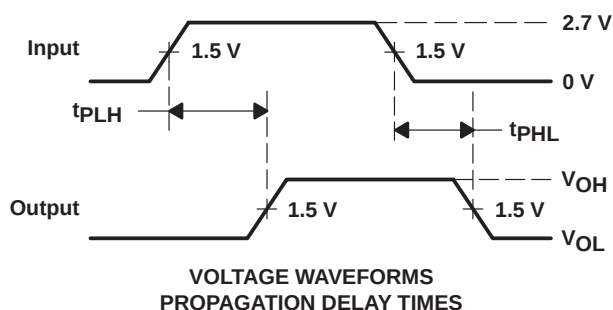
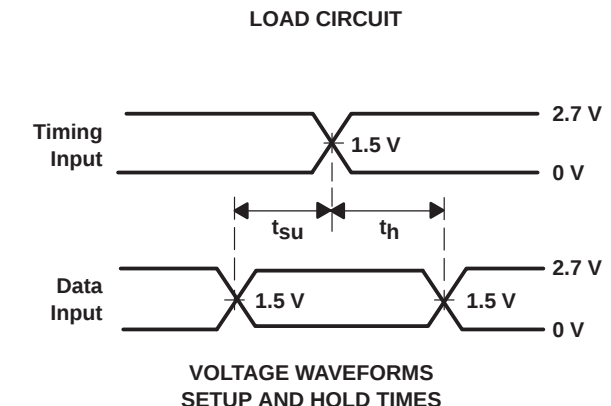
#### PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

| TEST              | S1   |
|-------------------|------|
| $t_{pd}$          | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V  |
| $t_{PHZ}/t_{PZH}$ | GND  |



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.