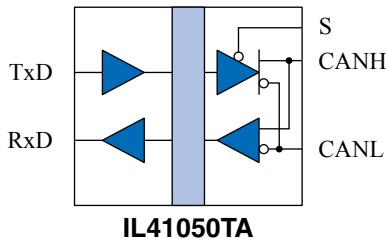


# High-Speed, Low-Power Isolated CAN Transceiver

## Functional Diagram



<b>V<sub>DD2</sub> (V)</b>	<b>TxD<sup>(1)</sup></b>	<b>S</b>	<b>CANH</b>	<b>CANL</b>	<b>Bus State</b>	<b>RxD</b>
4.75 to 5.25	↓	Low <sup>(2)</sup>	High	Low	Dominant	Low
4.75 to 5.25	X	High	V <sub>DD2</sub> /2	V <sub>DD2</sub> /2	Recessive	High
4.75 to 5.25	↑	X	V <sub>DD2</sub> /2	V <sub>DD2</sub> /2	Recessive	High
<2V (no pwr)	X	X	0<V<2.5	0<V<2.5	Recessive	High
2<V <sub>DD2</sub> <4.75	>2V	X	0<V<2.5	0<V<2.5	Recessive	High

**Table 1.** Function table.

### Notes:

1. TxD input is edge triggered: ↑ = Logic Lo to Hi, ↓ = Hi to Lo
2. Valid for logic state as described or open circuit

X = don't care

## Features

- 180 ns typical loop delay
- 70 mA maximum bus-side dynamic supply current
- 12 mA maximum quiescent recessive supply current
- 1 Mbps
- Fully compliant with the ISO 11898 CAN standard
- -55°C to +125°C operating temperature
- 3 V to 5.5 V power supplies
- >110-node fan-out
- 1000 V<sub>RMS</sub>/1500 V<sub>DC</sub> high voltage endurance
- 44000 year barrier life
- ±500 V CDM ESD
- 50 kV/μs typ.; 30 kV/μs min. common mode transient immunity
- No carrier or clock for low emissions and EMI susceptibility
- Silent mode to disable transmitter
- Transmit data (TxD) dominant time-out function
- Edge triggered, non-volatile input improves noise performance
- Thermal shutdown protection
- Bus power short-circuit protection
- 0.15", 0.3", or True 8™ mm 16-pin SOIC packages
- UL 1577 recognized; IEC 60747-5-5 (VDE 0884) certified

## Applications

- Factory automation
- Battery management systems
- Noise-critical CAN
- DeviceNet
- Equipment covered under IEC 61010-1 Edition 3

## Description

The IL41050TA is a galvanically isolated, CAN (Controller Area Network) transceiver, designed as the interface between the CAN protocol controller and the physical bus.

Quiescent and dynamic supply current is significantly lower than NVE's higher speed CAN (Controller Area Network) transceivers.

The IL41050 family provides isolated differential transmit capability to the bus and isolated differential receive capability to the CAN controller via NVE's patented\* IsoLoop spintronic Giant Magnetoresistance (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

Advanced features facilitate reliable bus operation. Unpowered nodes do not disturb the bus, and a unique non-volatile programmable power-up feature prevents unstable nodes. The devices also have a hardware-selectable silent mode that disables the transmitter.

Designed for harsh CAN and DeviceNet environments, IL41050TA transceivers have transmit data dominant time-out, bus pin transient protection, a rugged Charged Device Model ESD rating, thermal shutdown protection, and short-circuit protection. Unique edge-triggered inputs improve noise performance.

ISOLOOP® is a registered trademark of NVE Corporation.  
\*U.S. Patent number 5,831,426; 6,300,617 and others.

**Absolute Maximum Ratings<sup>(1)(2)</sup>**

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage temperature	T <sub>S</sub>	-55		150	°C	
Junction temperature	T <sub>J</sub>	-55		150	°C	
Ambient operating temperature	T <sub>A</sub>	-55		125	°C	
DC voltage at CANH and CANL pins	V <sub>CANH</sub> , V <sub>CANL</sub>	-45		45	V	0 V < V <sub>DD2</sub> < 5.25 V; indefinite duration
Supply voltage	V <sub>DD1</sub> , V <sub>DD2</sub>	-0.3		7	V	
Digital input voltage	V <sub>TxD</sub> , V <sub>S</sub>	-0.3		V <sub>DD</sub> + 0.3	V	
Digital output voltage	V <sub>RxD</sub>	-0.3		V <sub>DD</sub> + 0.3	V	
DC voltage at V <sub>REF</sub>	V <sub>REF</sub>	-0.3		V <sub>DD</sub> + 0.3	V	
Transient voltage at CANH or CANL	V <sub>trt(CAN)</sub>	-150		150	V	
Electrostatic discharge at all pins	V <sub>esd</sub>	-4000		4000	V	Human body model
Electrostatic discharge at all pins	V <sub>esd</sub>	-500		500	V	Machine model

**Recommended Operating Conditions**

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply voltage	V <sub>DD1</sub>	3.0		5.5	V	
	V <sub>DD2</sub>	4.75		5.25		
Junction temperature	T <sub>J</sub>	-55		140	°C	
Input voltage at any bus terminal (separately or common mode)	V <sub>CANH</sub> V <sub>CANL</sub>	-12		12	V	
High-level digital input voltage <sup>(3)(4)</sup>	V <sub>IH</sub>	2.0 2.4 2.0		V <sub>DD1</sub> V <sub>DD1</sub> V <sub>DD2</sub>	V	V <sub>DD1</sub> = 3.3 V V <sub>DD1</sub> = 5.0 V V <sub>DD2</sub> = 5.0 V
Low-level digital input voltage <sup>(3)(4)</sup>	V <sub>IL</sub>	0		0.8	V	
Digital output current (RxD)	I <sub>OH</sub>	-8		8	mA	V <sub>DD1</sub> = 3.3 V to 5 V
Ambient operating temperature	T <sub>A</sub>	-55		125	°C	
Digital input signal rise and fall times	t <sub>IR</sub> , t <sub>IF</sub>			1	μs	

**Insulation Specifications**

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage distance (external)	IL41050TA-3E IL41050TAE		4.0 8.03	8.3	mm	Per IEC 60601
Total barrier thickness (internal)		0.012	0.013		mm	
Barrier resistance	R <sub>IO</sub>		>10 <sup>14</sup>		Ω	500 V
Barrier capacitance	C <sub>IO</sub>		7		pF	f = 1 MHz
Leakage current			0.2		μA <sub>RMS</sub>	240 V <sub>RMS</sub> , 60 Hz
Comparative Tracking Index	CTI	≥175			V	Per IEC 60112
High voltage endurance (maximum barrier voltage for indefinite life)	AC DC	V <sub>IO</sub>	1000 1500		V <sub>RMS</sub> V <sub>DC</sub>	At maximum operating temperature
Barrier life			44000		Years	100°C, 1000 V <sub>RMS</sub> , 60% CL activation energy

**Thermal Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction-ambient thermal resistance	IL41050TA-3E IL41050TAE	θ <sub>JA</sub>		100 60	°C/W	Soldered to double-sided board; free air
Junction-case thermal resistance	IL41050TA-3E IL41050TAE	Ψ <sub>JT</sub>		25 12	°C/W	
Power dissipation	IL41050TA-3E IL41050TAE	P <sub>D</sub>		625 800	mW	

## **Safety and Approvals**

### **IEC 60747-5-5 (VDE 0884)** (File Number 5016933-4880-0001)

- Working Voltage ( $V_{IORM}$ ) 600 V<sub>RMS</sub> (848 V<sub>PK</sub>); basic insulation; pollution degree 2
- Transient overvoltage ( $V_{IOTM}$ ) and surge voltage ( $V_{IOSM}$ ) 4000 V<sub>PK</sub>
- Each part tested at 1590 V<sub>PK</sub> for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V<sub>PK</sub> for 60 sec.; then 1358 V<sub>PK</sub> for 10 sec. with 5 pC partial discharge limit

### **IEC 61010-1** (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)

Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-3	SOIC	150 V <sub>RMS</sub>
None	Wide-body SOIC/True 8™	300 V <sub>RMS</sub>

### **UL 1577** (Component Recognition Program File Number E207481)

Each part tested at 3000 V<sub>RMS</sub> (4240 V<sub>PK</sub>) for 1 second; each lot sample tested at 2500 V<sub>RMS</sub> (3530 V<sub>PK</sub>) for 1 minute

## **Soldering Profile**

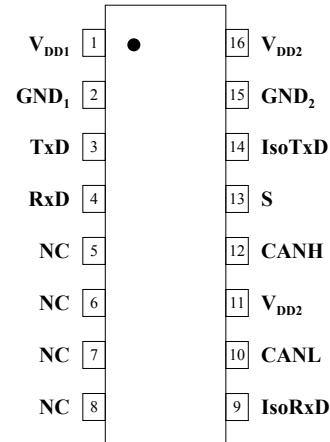
Per JEDEC J-STD-020C; MSL=1

## **Notes:**

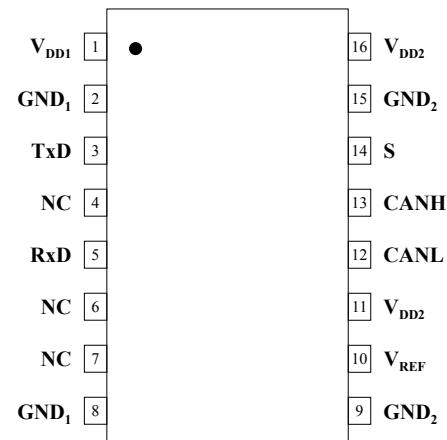
1. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. All voltages are with respect to network ground except differential I/O bus voltages.
3. The TxD input is edge sensitive. Voltage magnitude of the input signal is specified, but edge rate specifications must also be met.
4. The maximum time allowed for a logic transition at the TxD input is 1  $\mu$ s.

**IL41050-3 Pin Connections (0.15" SOIC Package)**

1	V <sub>DD1</sub>	V <sub>DD1</sub> power supply input
2	GND <sub>1</sub>	V <sub>DD1</sub> power supply ground return
3	TxD	Transmit Data input
4	RxD	Receive Data output
5	NC	No internal connection
6	NC	No internal connection
7	NC	No internal connection
8	NC	No internal connection
9	IsoRxD	Isolated RxD output. No connection should be made to this pin.
10	CANL	Low level CANbus line
11	V <sub>DD2</sub>	V <sub>DD2</sub> CAN I/O bus circuitry power supply input*
12	CANH	High level CANbus line
13	S	Mode select input. Leave open or set low for normal operation; set high for silent mode.
14	IsoTxD	Isolated TxD output. No connection should be made to this pin.
15	GND <sub>2</sub>	V <sub>DD2</sub> power supply ground return
16	V <sub>DD2</sub>	V <sub>DD2</sub> isolation power supply input*

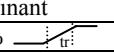

**IL41050 Pin Connections (0.3" SOIC Package)**

1	V <sub>DD1</sub>	V <sub>DD1</sub> power supply input
2	GND <sub>1</sub>	V <sub>DD1</sub> power supply ground return (pin 2 is internally connected to pin 8)
3	TxD	Transmit Data input
4	NC	No internal connection
5	RxD	Receive Data output
6	NC	No internal connection
7	NC	No internal connection
8	GND <sub>1</sub>	V <sub>DD1</sub> power supply ground return (pin 8 is internally connected to pin 2)
9	GND <sub>2</sub>	V <sub>DD2</sub> power supply ground return (pin 9 is internally connected to pin 15)
10	V <sub>REF</sub>	Reference voltage output (nominally 50% of V <sub>DD2</sub> )
11	V <sub>DD2</sub>	V <sub>DD2</sub> CAN I/O bus circuitry power supply input*
12	CANL	Low level CANbus line
13	CANH	High level CANbus line
14	S	Mode select input. Leave open or set low for normal operation; set high for silent mode.
15	GND <sub>2</sub>	V <sub>DD2</sub> power supply ground return (pin 15 is internally connected to pin 9)
16	V <sub>DD2</sub>	V <sub>DD2</sub> isolation power supply input*



\*NOTE: Pin 11 is not internally connected to pin 16; both should be connected to the V<sub>DD2</sub> power supply for normal operation.

## Operating Specifications

Electrical Specifications (T <sub>min</sub> to T <sub>max</sub> and V <sub>DD1</sub> , V <sub>DD2</sub> = 4.75 V to 5.25 V unless otherwise stated)						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
<b>Power Supply Current</b>						
Quiescent supply current (recessive)	I <sub>Q<sub>VDD1</sub></sub>	1 0.7	1.75 1.4	3.0 2.0	mA	dr = 0 bps; V <sub>DD1</sub> = 5 V dr = 0 bps; V <sub>DD1</sub> = 3.3 V
Dynamic supply current (dominant)	I <sub>VDD1</sub>	1.2 0.9	2.0 1.6	3.2 2.2	mA	dr = 1 Mbps, R <sub>L</sub> = 60Ω; V <sub>DD1</sub> = 5 V dr = 1 Mbps, R <sub>L</sub> = 60Ω; V <sub>DD1</sub> = 3.3 V
Quiescent supply current (recessive)	I <sub>Q<sub>VDD2</sub></sub>	3.5	7	12	mA	0 bps
Dynamic supply current (dominant)	I <sub>VDD2</sub>	26	52	70	mA	1 Mbps, R <sub>L</sub> = 60Ω
<b>Transmitter Data input (TxD)<sup>(1)</sup></b>						
High level input voltage ↑	V <sub>IH</sub>	2.4		5.25	V	V <sub>DD1</sub> = 5 V; recessive
High level input voltage ↑	V <sub>IH</sub>	2.0		3.6	V	V <sub>DD1</sub> = 3.3 V; recessive
Low level input voltage ↓	V <sub>IL</sub>	-0.3		0.8	V	Output dominant
TxD input rise and fall time <sup>(2)</sup>	t <sub>r</sub>			1	μs	10% to 90% 
High level input current	I <sub>IH</sub>	-10		10	μA	V <sub>TxD</sub> = V <sub>DD1</sub>
Low level input current	I <sub>IL</sub>	10		10	μA	V <sub>TxD</sub> = 0 V
<b>Mode select input (S)</b>						
High level input voltage	V <sub>IH</sub>	2.0		V <sub>DD2</sub> + 0.3	V	Silent mode
Low level input voltage	V <sub>IL</sub>	-0.3		0.8	V	High-speed mode
High level input current	I <sub>IH</sub>	20	30	50	μA	V <sub>S</sub> = 2 V
Low level input current	I <sub>IL</sub>	15	30	45	μA	V <sub>S</sub> = 0 V
<b>Receiver Data output (RxD)</b>						
High level output current	I <sub>OH</sub>	-2	-8.5	-20	mA	V <sub>RxD</sub> = 0.8 V <sub>DD1</sub>
Low level output current	I <sub>OL</sub>	2	8.5	20	mA	V <sub>RxD</sub> = 0.45 V
Failsafe supply voltage <sup>(4)</sup>	V <sub>DD2</sub>	3.6		3.9	V	
<b>Reference Voltage output (V<sub>REF</sub>)</b>						
Reference Voltage output	V <sub>REF</sub>	0.45 V <sub>DD2</sub>	0.5 V <sub>DD2</sub>	0.55 V <sub>DD2</sub>	V	-50 μA < I <sub>VREF</sub> < +50 μA
<b>Bus lines (CANH and CANL)</b>						
Recessive voltage at CANH pin	V <sub>O(recess)</sub> CANH	2.0	2.5	3.0	V	V <sub>TxD</sub> = V <sub>DD1</sub> , no load
Recessive voltage at CANL pin	V <sub>O(recess)</sub> CANL	2.0	2.5	3.0	V	V <sub>TxD</sub> = V <sub>DD1</sub> , no load
Recessive current at CANH pin	I <sub>O(recess)</sub> CANH	-2.5		+2.5	mA	-27V < V <sub>CANH</sub> < +32V; 0V < V <sub>DD2</sub> < 5.25V
Recessive current at CANL pin	I <sub>O(recess)</sub> CANL	-2.5		+2.5	mA	-27V < V <sub>CANL</sub> < +32V; 0V < V <sub>DD2</sub> < 5.25V
Dominant voltage at CANH pin	V <sub>O(dom)</sub> CANH	3.0	3.6	4.25	V	V <sub>TxD</sub> = 0 V
Dominant voltage at CANL pin	V <sub>O(dom)</sub> CANL	0.5	1.4	1.75	V	V <sub>TxD</sub> = 0 V
Differential bus input voltage (V <sub>CANH</sub> - V <sub>CANL</sub> )	V <sub>i(dif)(bus)</sub>	1.5	2.25	3.0	V	V <sub>TxD</sub> = 0 V; dominant 42.5 Ω < R <sub>L</sub> < 60 Ω
		-120	0	+50	mV	V <sub>TxD</sub> = V <sub>DD1</sub> ; recessive; no load
Short-circuit output current at CANH	I <sub>O(sc)</sub> CANH	-45	-70	-95	mA	V <sub>CANH</sub> = 0 V, V <sub>TxD</sub> = 0
Short-circuit output current at CANL	I <sub>O(sc)</sub> CANL	45	70	120	mA	V <sub>CANL</sub> = 36 V, V <sub>TxD</sub> = 0
Differential receiver threshold voltage	V <sub>i(dif)(th)</sub>	0.5	0.7	0.9	V	-5 V < V <sub>CANL</sub> < +10 V; -5 V < V <sub>CANH</sub> < +10 V
Differential receiver input voltage hysteresis	V <sub>i(dif)(hys)</sub>	50	70	100	mV	-5 V < V <sub>CANL</sub> < +10 V; -5 V < V <sub>CANH</sub> < +10 V
Common Mode input resistance at CANH	R <sub>i(CM)(CANH)</sub>	15	25	37	kΩ	
Common Mode input resistance at CANL	R <sub>i(CM)(CANL)</sub>	15	25	37	kΩ	
Matching between Common Mode input resistance at CANH, CANL	R <sub>i(CM)(m)</sub>	-3	0	+3	%	V <sub>CANL</sub> = V <sub>CANH</sub>

Electrical Specifications ( $T_{min}$ to $T_{max}$ and $V_{DD1}, V_{DD2} = 4.5$ V to 5.5 V unless otherwise stated)						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
<b>Bus lines (....cont)</b>						
Differential input resistance	$R_{i(dif)}$	25	50	75	k $\Omega$	
Input capacitance, CANH	$C_{i(CANH)}$		7.5	20	pF	$V_{TxD} = V_{DD1}$
Input capacitance, CANL	$C_{i(CANL)}$		7.5	20	pF	$V_{TxD} = V_{DD1}$
Differential input capacitance	$C_{i(dif)}$		3.75	10	pF	$V_{TxD} = V_{DD1}$
Input leakage current at CANH	$I_{LI(CANH)}$	100	170	250	$\mu A$	$V_{CANH} = 5$ V, $V_{DD2} = 0$
Input leakage current at CANL	$I_{LI(CANL)}$	100	170	250	$\mu A$	$V_{CANL} = 5$ V, $V_{DD2} = 0$
<b>Thermal Shutdown</b>						
Shutdown junction temperature	$T_{j(SD)}$	155	165	180	°C	

Timing Characteristics (60 $\Omega$ / 100 pF bus loading; 20 pF RxD load; see Fig. 1)						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
TxD to bus active delay	$t_{d(TxD-BUSon)}$	44 36	93 96	160 128	ns	$V_S = 0$ V; $V_{DD1} = 5$ V $V_S = 0$ V; $V_{DD1} = 3.3$ V
TxD to bus inactive delay	$t_{d(TxD-BUSoff)}$	34 37	68 71	110 113	ns	$V_S = 0$ V; $V_{DD1} = 5$ V $V_S = 0$ V; $V_{DD1} = 3.3$ V
Bus active to RxD delay	$t_{d(BUSon-RxD)}$	29 32	63 66	125 128	ns	$V_S = 0$ V; $V_{DD1} = 5$ V $V_S = 0$ V; $V_{DD1} = 3.3$ V
Bus inactive to RxD delay	$t_{d(BUSoff-RxD)}$	69 72	108 111	170 173	ns	$V_S = 0$ V; $V_{DD1} = 5$ V $V_S = 0$ V; $V_{DD1} = 3.3$ V
Loop delay low-to-high or high-to-low	$T_{LOOP}$	74	180	250	ns	$V_S = 0$ V; "Typ." at 25°C and nominal loads
TxD dominant time for timeout	$T_{dom(TxD)}$	250	457	765	$\mu s$	$V_{TxD} = 0$ V $3.0$ V > $V_{DD1} < 5.5$ V
Common Mode Transient Immunity (TxD Logic High or Logic Low)	$ CM_H ,  CM_L $	30	50		kV/ $\mu s$	$R_L = 60$ $\Omega$ ; $V_{CM} = 1500$ V <sub>DC</sub> ; $t_{TRANSIENT} = 25$ ns

Magnetic Field Immunity <sup>(3)</sup> ( $V_{DD2} = 5$ V, $3V < V_{DD1} < 5.5$ V)					
Power Frequency Magnetic Immunity	$H_{PF}$	4000	6000		A/m
Pulse Magnetic Field Immunity	$H_{PM}$	6000	7000		A/m
Damped Oscillatory Magnetic Field	$H_{OSC}$	6000	7000		A/m
Cross-axis Immunity Multiplier	$K_X$		2		See Fig. 4

**Notes:**

1. The TxD input is edge sensitive. Voltage magnitude of the input signal is specified, but edge rate specifications must also be met.
2. The maximum time allowed for a logic transition at the TxD input is 1  $\mu$ s.
3. Test and measurement methods are given in the Electromagnetic Compatibility section on p. 10.
4. If  $V_{DD2}$  falls below the specified failsafe supply voltage, RxD will go High.

## Timing Test Circuit

Timing parameters are measured with  $60\ \Omega$  /  $100\ \text{pF}$  bus line loading and  $20\ \text{pF}$  on RxD as shown in Figure 1 below:

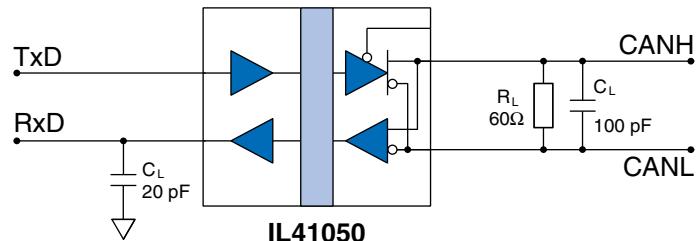


Figure 1. Timing characteristics test circuit.

## Block Diagram

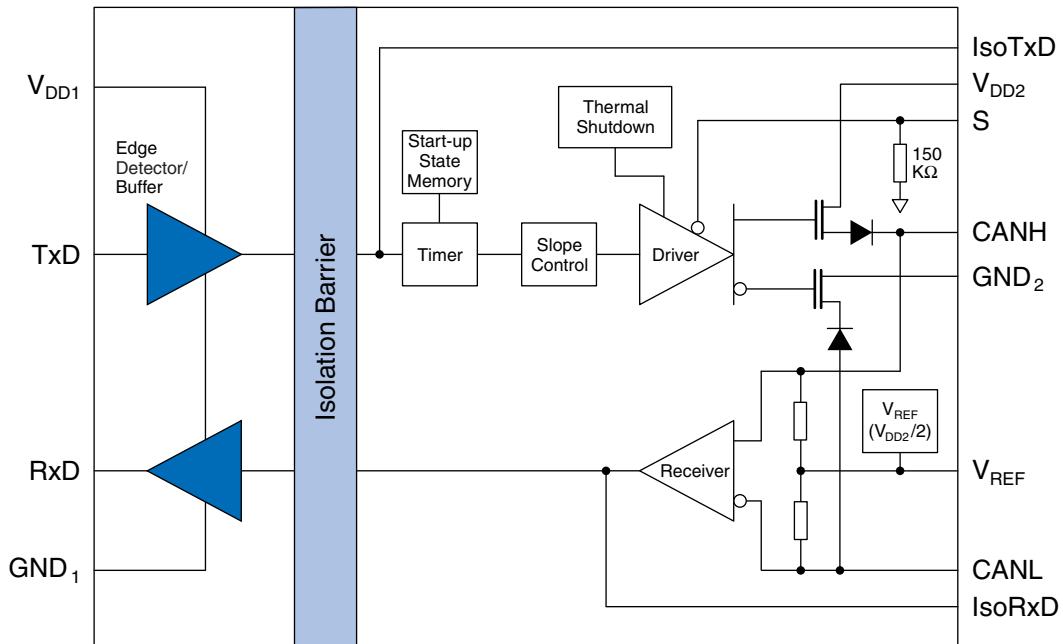
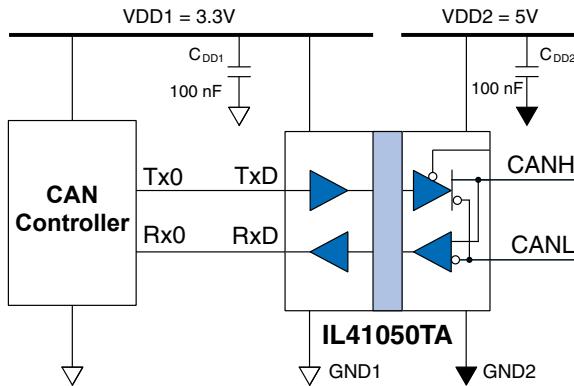


Figure 2. IL41050TA detailed functional diagram.

## Application Information

As Figure 3 shows, the IL41050TA can provide isolation and level shifting between a 5 volt CAN bus and a 3 volt microcontroller:



**Figure 3. Isolated CAN node using the IL41050TA.**

### Bus-Side Power Supply Pins

Both  $V_{DD2}$  power supply inputs (pins 11 and 16) must be connected to the bus-side power supply. Pin 11 powers the bus side of the CAN I/O circuitry, while pin 16 powers the bus-side isolation circuitry. For testing purposes, they are not internally connected, but the part will not operate without both pins powered, and operation without both pins powered can cause damage.

### Power Supply Decoupling

Both  $V_{DD1}$  and  $V_{DD2}$  must be bypassed with 100 nF ceramic capacitors. These supply the dynamic current required for the isolator switching and should be placed as close as possible to  $V_{DD}$  and their respective ground return pins.

### Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

### Input Configurations

The TxD input should not be left open as the state will be indeterminate. If connected to an open-drain or open collector output, a pull-up resistor (typically 16 k $\Omega$ ) should be connected from the input to  $V_{DD1}$ .

The Mode Select (“S”) input has a nominal 150 k $\Omega$  internal pull-down resistor. It can be left open or set low for normal operation.

### Dominant Mode Time-out and Failsafe Receiver Functions

CAN bus latch up is prevented by an integrated Dominant mode timeout function. If the TxD pin is forced permanently low by hardware or software application failure, the time-out returns the RxD output to the high state no more than 765  $\mu$ s after TxD is asserted dominant. The timer is triggered by a negative edge on TxD. If the duration of the low is longer than the internal timer value, the transmitter is disabled, driving the bus to the recessive state. The timer is reset by a positive edge on pin TxD.

If power is lost on  $V_{DD2}$ , the IL41050 asserts the RxD output high when the supply voltage falls below 3.8 V. RxD will return to normal operation when  $V_{DD2}$  rises above approximately 4.2 V.

### Programmable Power-Up

A unique non-volatile programmable power-up feature prevents unstable nodes. A state that needs to be present at node power up can be programmed at the last power down. For example if a CAN node is required to “pulse” dominant at power up, TxD can be sent low by the controller immediately prior to power down. When power is resumed, the node will immediately go dominant allowing self-check code in the microcontroller to verify node operation. If desired, the node can also power up silently by presetting the TxD line high at power down. At the next power on, the IL41050 will remain silent, awaiting a dominant state from the bus.

The microcontroller can check that the CAN node powered down correctly before applying power at the next “power on” request. If the node powered down as intended, RxD will be set high and stored in the IL41050’s non-volatile memory. The level stored in the RxD bit can be read before isolated node power is enabled, avoiding possible CAN bus disruption due to an unstable node.

## Replacing Non-Isolated Transceivers

The IL41050 is designed to replace common non-isolated CAN transceivers such as the Philips/NXP TJA1050 with minimal circuit changes. Some notable differences:

- Some non-isolated CAN transceivers have internal TxD pull-up resistors, but the IL41050 TxD input should not be left open. If connected to an open-drain or open collector output, a pull-up resistor (typically 16 kΩ) should be connected from the input to  $V_{DD1}$ .
- Initialization behavior varies between CAN transceivers. To ensure the desired power-up state, the IL41050 should be initialized with a TxD pulse (low-to-high for recessive initialization), or shut down the transceiver in the desired power-up state (the “programmable power-up feature”).
- Many non-isolated CAN transceivers have a  $V_{REF}$  output. Such a reference is available on the IL41050 wide-body version.

## The VREF Output

$V_{REF}$  is a reference voltage output used to drive bus threshold comparators in some legacy systems and is provided on the IL41050 wide-body version. The output is half of the bus supply  $\pm 10\%$  (*i.e.*,  $0.45 V_{DD2} < V_{REF} < 0.55 V_{DD2}$ ), and can drive up to 50  $\mu A$ .

## IsoRxD / IsoTxD Outputs

The IsoRxD and IsoTxD outputs are isolated versions of the RxD and TxD signals. These outputs are provided for troubleshooting on the narrow-body version, but normally no connections should be made to the pins.

## The Isolation Advantage

Battery fire caused by over or under charging of individual lithium ion cells is a major concern in multi-cell high voltage electric and hybrid vehicle batteries. To combat this, each cell is monitored for current flow, cell voltage, and in some advanced batteries, magnetic susceptibility. The IL41050 allows seamless connection of the monitoring electronics of every cell to a common CAN bus by electrically isolating inputs from outputs, effectively isolating each cell from all other cells. Cell status is then monitored via the CAN controller in the Battery Management System (BMS).

Another major advantage of isolation is the tremendous increase in noise immunity it affords the CAN node, even if the power source is a battery. Inductive drives and inverters can produce transient swings in excess of 20 kV/μs. The traditional, non-isolated CAN node provides some protection due to differential signaling and symmetrical driver/receiver pairs, but the IL41050 typically provides more than twice the dV/dt protection of a traditional CAN node.

## **Electrostatic Discharge Sensitivity**

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

## **Electromagnetic Compatibility**

The IL41050 is fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. The IsoLoop Isolator's Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. NVE conducted compliance tests in the categories below:

### EN50081-1

Residential, Commercial & Light Industrial  
Methods EN55022, EN55014

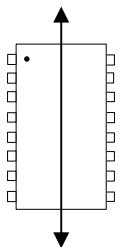
### EN50082-2: Industrial Environment

Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)

### ENV50204

Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is higher if the field direction is "end-to-end" (rather than to "pin-to-pin") as shown in the diagram below:

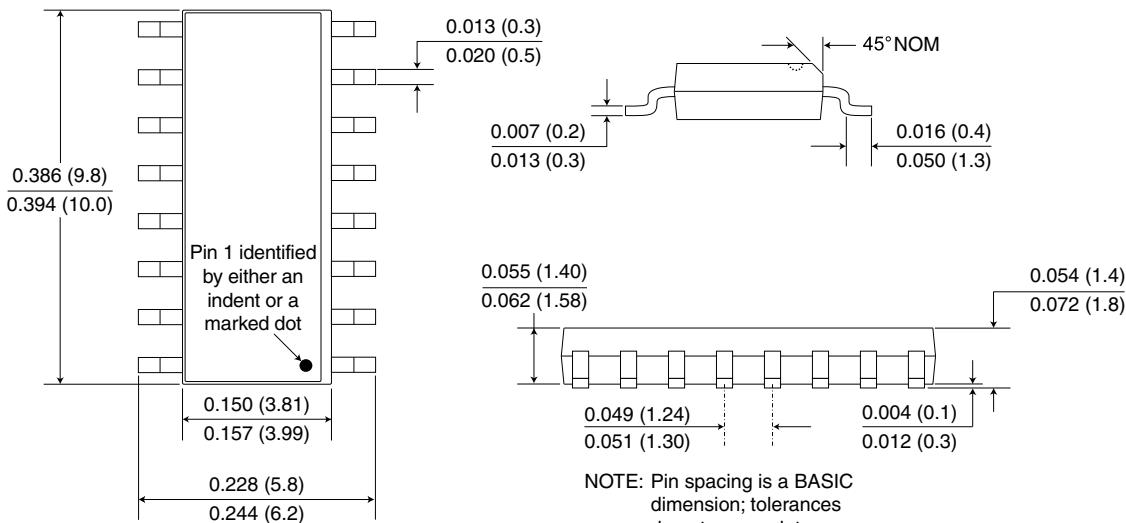


**Figure 4. Orientation for high field immunity.**

**Package Drawings**

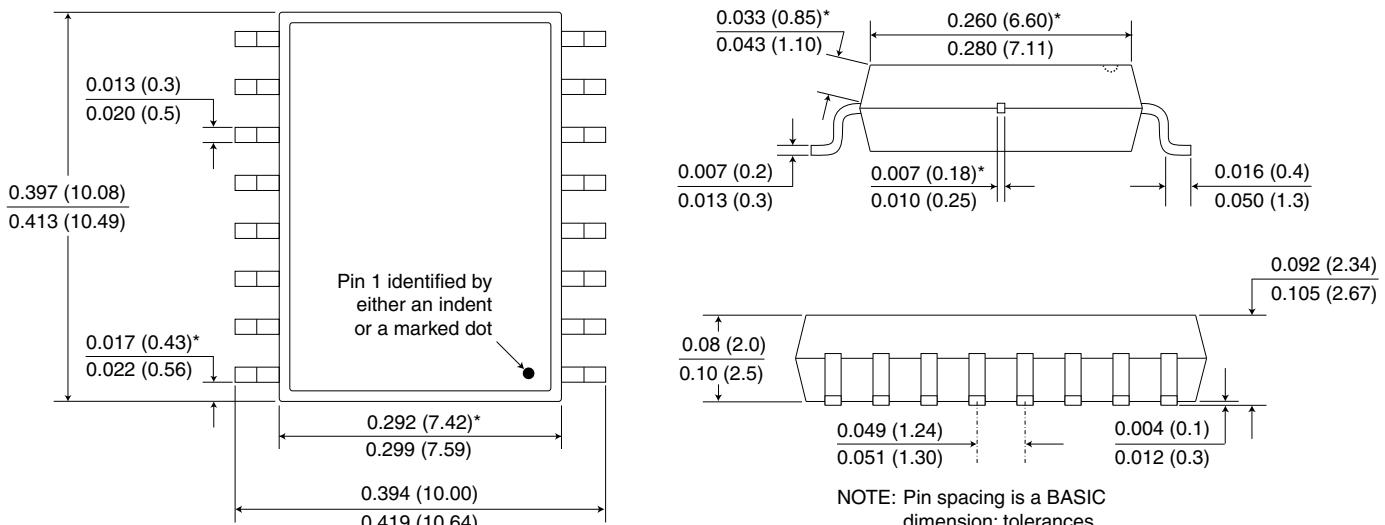
**0.15" 16-pin SOIC Package (-3 suffix)**

Dimensions in inches (mm); scale = approx. 5X



**0.3" 16-pin SOIC Package (no suffix)**

Dimensions in inches (mm); scale = approx. 5X

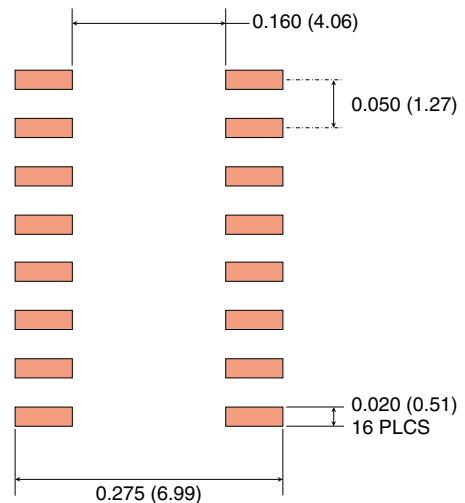


\*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

**Recommended Pad Layouts**

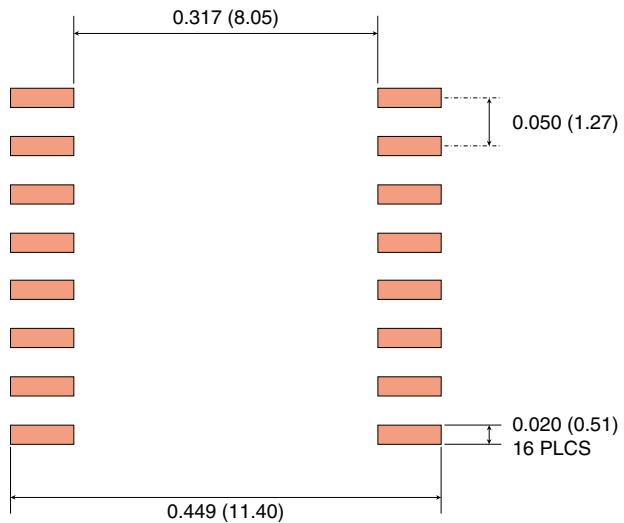
**0.15" 16-pin SOIC Pad Layout**

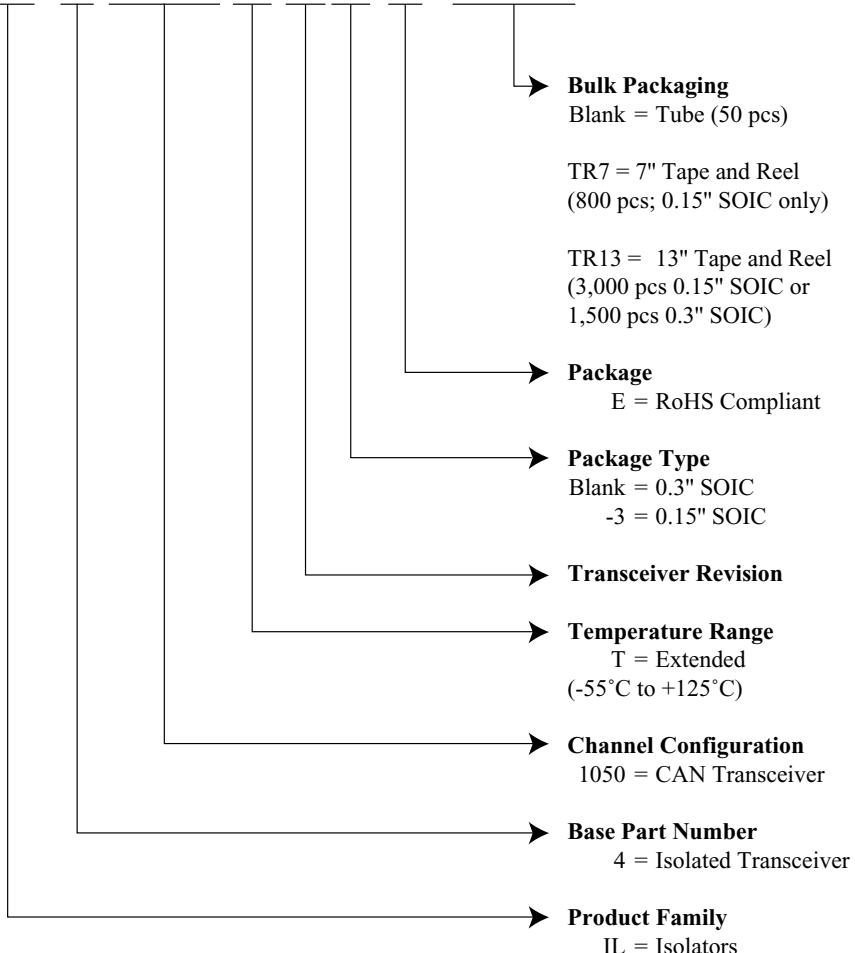
Dimensions in inches (mm); scale = approx. 5X



**0.3" 16-pin SOIC Pad Layout**

Dimensions in inches (mm); scale = approx. 5X



**Ordering Information and Valid Part Numbers**
**IL 4 1050 T A-3 E TR13**

**Valid Part Numbers**

IL41050TAE  
IL41050TAE TR13  
IL41050TA-3E  
IL41050TA-3E TR7  
IL41050TA-3E TR13

**RoHS  
COMPLIANT**

**Revision History****ISB-DS-001-IL41050TA-H****November 2013****Change**

- IEC 60747-5-5 (VDE 0884) certification.
- Upgraded from MSL 2 to MSL 1.

**ISB-DS-001-IL41050TA-G****June 2013****Change**

- Added VDE 0884 pending.
- Added transient immunity specifications.
- Added high voltage endurance specification (p. 2).
- Increased magnetic immunity specifications (p. 6).
- Updated package drawings.
- Added recommended solder pad layouts.

**ISB-DS-001-IL41050TA-F****January 2013****Change**

- Added thermal characteristics (p. 2).
- Cosmetic changes.

**ISB-DS-001-IL41050TA-E****December 2012****Changes**

- UL 1577 recognition and IEC 61010-1 approval.
- Detailed isolation and barrier specifications.
- Style and cosmetic changes.

**ISB-DS-001-IL41050TA-D****October 2012****Changes**

- Changed title to highlight speed.
- Added block diagram (detailed functional diagram).
- Rearranged and repaginated.

**ISB-DS-001-IL41050TA-C****July 2012****Changes**

- Tightened and clarified typical loop delay specification.
- Clarified IsoRxD / IsoTxD outputs on narrow-body package.

**ISB-DS-001-IL41050TA-B****July 2012****Changes**

- Specified timing characteristics test conditions and added test circuit (p. 5).
- More detailed application diagram (p. 6).
- Misc. cosmetic changes.

**ISB-DS-001-IL41050TA-A****May 2012****Changes**

- Initial release.

**ISB-DS-001-IL41050TA-Preview****February 2012****Changes**

- Released product preview.

### **Datasheet Limitations**

The information and data provided in datasheets shall define the specification of the product as agreed between NVE and its customer, unless NVE and customer have explicitly agreed otherwise in writing. All specifications are based on NVE test protocols. In no event however, shall an agreement be valid in which the NVE product is deemed to offer functions and qualities beyond those described in the datasheet.

### **Limited Warranty and Liability**

Information in this document is believed to be accurate and reliable. However, NVE does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NVE be liable for any indirect, incidental, punitive, special or consequential damages (including, without limitation, lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

### **Right to Make Changes**

NVE reserves the right to make changes to information published in this document including, without limitation, specifications and product descriptions at any time and without notice. This document supersedes and replaces all information supplied prior to its publication.

### **Use in Life-Critical or Safety-Critical Applications**

Unless NVE and a customer explicitly agree otherwise in writing, NVE products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical devices or equipment. NVE accepts no liability for inclusion or use of NVE products in such applications and such inclusion or use is at the customer's own risk. Should the customer use NVE products for such application whether authorized by NVE or not, the customer shall indemnify and hold NVE harmless against all claims and damages.

### **Applications**

Applications described in this datasheet are illustrative only. NVE makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NVE products, and NVE accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NVE product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customers. Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NVE does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customers. The customer is responsible for all necessary testing for the customer's applications and products using NVE products in order to avoid a default of the applications and the products or of the application or use by customer's third party customers. NVE accepts no liability in this respect.

### **Limiting Values**

Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the recommended operating conditions of the datasheet is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

### **Terms and Conditions of Sale**

In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NVE hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NVE products by customer.

### **No Offer to Sell or License**

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### **Export Control**

This document as well as the items described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

### **Automotive Qualified Products**

Unless the datasheet expressly states that a specific NVE product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NVE accepts no liability for inclusion or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NVE's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NVE's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NVE for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NVE's standard warranty and NVE's product specifications.

An ISO 9001 Certified Company

NVE Corporation  
11409 Valley View Road  
Eden Prairie, MN 55344-3617 USA  
Telephone: (952) 829-9217  
Fax: (952) 829-9189  
[www.nve.com](http://www.nve.com)  
e-mail: [iso-info@nve.com](mailto:iso-info@nve.com)

©NVE Corporation  
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

ISB-DS-001-IL41050TA-H

*November 2013*