

32K x 8 Static RAM

Features

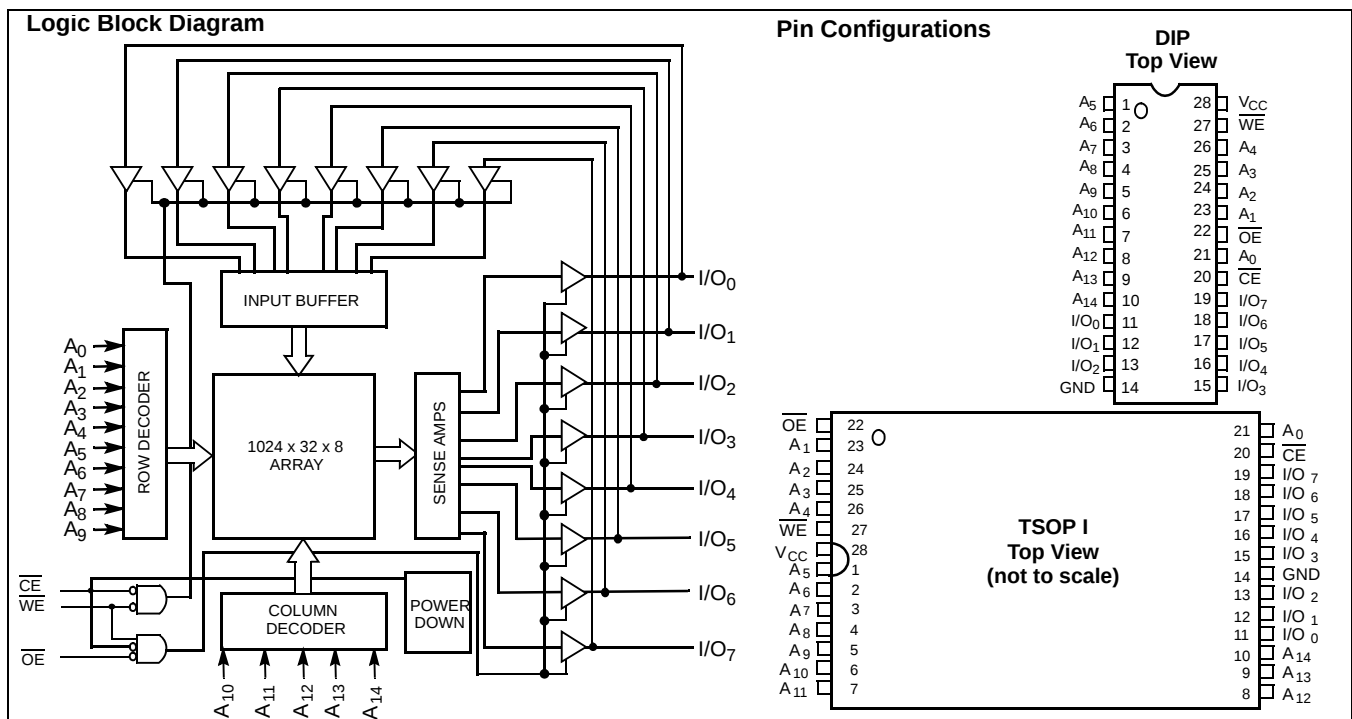
- **High speed**
— 12 ns
- **Fast t_{DOE}**
- **CMOS for optimum speed/power**
- **Low active power**
— 467 mW (max, 12 ns “L” version)
- **Low standby power**
— 0.275 mW (max, “L” version)
- **2V data retention (“L” version only)**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C199N is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and active LOW Output Enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199NN is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW Write Enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable ($\overline{WE}$) is HIGH. A die coat is used to improve alpha immunity.



Selection Guide

		-12	-15	-20	-25	-35	-55	Unit
Maximum Access Time		12	15	20	25	35	55	ns
Maximum Operating Current		160	155	150	150	140	140	mA
	L	90	90	90	80	70	70	
Maximum CMOS Standby Current		10	10	10	10	10	10	mA
	L	0.05	0.05	0.05	0.05	0.05	0.05	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) -0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	-12		-15		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	V
V_{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	-5	+5	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-5	+5	-5	+5	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	Com'l	160		155	mA
			L	85		100	mA
			Mil			180	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	Com'l	30		30	mA
			L	5		5	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$	Com'l	10		10	mA
			L	0.05		0.05	mA
			Mil			15	mA

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	-20		-25		-35		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	V
V_{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	-5	+5	-5	+5	-5	+5	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	Com'l	150		150		140		140	mA
			L	90		80		70		70	mA
			Mil	170		150		150		150	mA

Notes:

- $V_{IL}(\text{min.}) = -2.0V$ for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

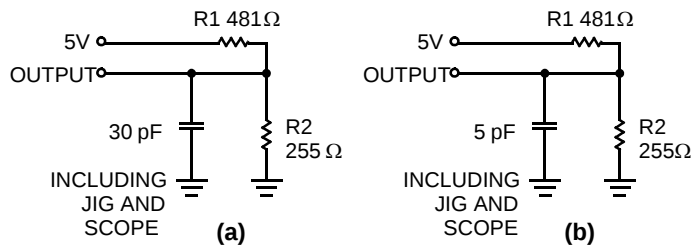
Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	-20		-25		-35		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{CC} , $CE \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	Com'I	30		30		25		25	mA
			L	5		5		5		5	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{CC} , $CE \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$	Com'I	10		10		10		10	mA
			L	0.05		0.05		0.05		0.05	mA
			Mil	15		15		15		15	mA

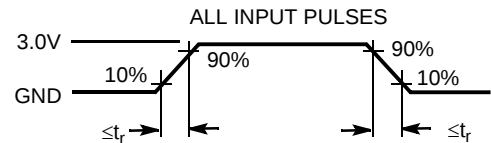
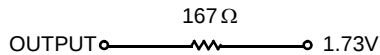
Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1\text{ MHz}$, $V_{CC} = 5.0V$	8	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms^[5]



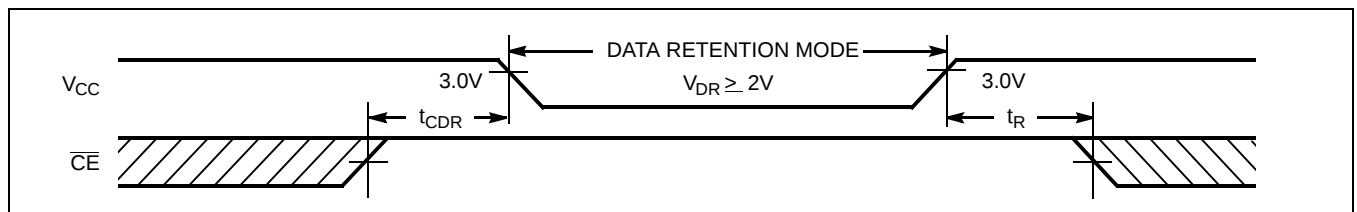
Equivalent to: THÉVENIN EQUIVALENT



Data Retention Characteristics Over the Operating Range (L-version only)

Parameter	Description	Conditions ^[6]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	Com'I			μA
		Com'I L		10	μA
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR} = 2.0V$, $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R^{[5]}$	Operation Recovery Time		200		μs

Data Retention Waveform



Note:

- Tested initially and after any design or process changes that may affect these parameters.
- $t_R \leq 3\text{ ns}$ for the -12 and the -15 speeds. $t_R \leq 5\text{ ns}$ for the -20 and slower speeds
- No input may exceed $V_{CC} + 0.5V$.

Switching Characteristics Over the Operating Range [3, 7]

Parameter	Description	7C199-12		7C199-15		7C199-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{RC}	Read Cycle Time	12		15		20		ns
t _{AA}	Address to Data Valid		12		15		20	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		5		7		9	ns
t _{LZOE}	$\overline{OE}$ LOW to Low-Z ^[8]	0		0		0		ns
t _{HZOE}	$\overline{OE}$ HIGH to High-Z ^[8, 9]		5		7		9	ns
t _{LZCE}	$\overline{CE}$ LOW to Low-Z ^[8]	3		3		3		ns
t _{HZCE}	$\overline{CE}$ HIGH to High-Z ^[8,9]		5		7		9	ns
t _{PU}	$\overline{CE}$ LOW to Power-up	0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-down		12		15		20	ns
Write Cycle ^[10, 11]								
t _{WC}	Write Cycle Time	12		15		20		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		ns
t _{AW}	Address Set-up to Write End	9		10		15		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	8		9		15		ns
t _{SD}	Data Set-up to Write End	8		9		10		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{HZWE}	$\overline{WE}$ LOW to High-Z ^[9]		7		7		10	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low-Z ^[8]	3		3		3		ns

Switching Characteristics Over the Operating Range [3, 7]

Parameter	Description	7C199-25		7C199-35		7C199-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{RC}	Read Cycle Time	25		35		55		ns
t _{AA}	Address to Data Valid		25		35		55	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		55	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		10		16		16	ns
t _{LZOE}	$\overline{OE}$ LOW to Low-Z ^[8]	0		0		0		ns
t _{HZOE}	$\overline{OE}$ HIGH to High-Z ^[8, 9]		11		15		15	ns
t _{LZCE}	$\overline{CE}$ LOW to Low-Z ^[8]	3		3		3		ns

Notes:

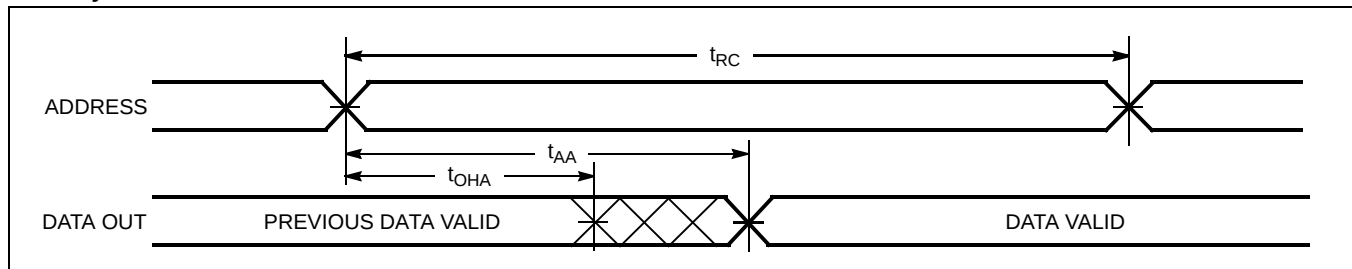
- Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Characteristics Over the Operating Range [3, 7]

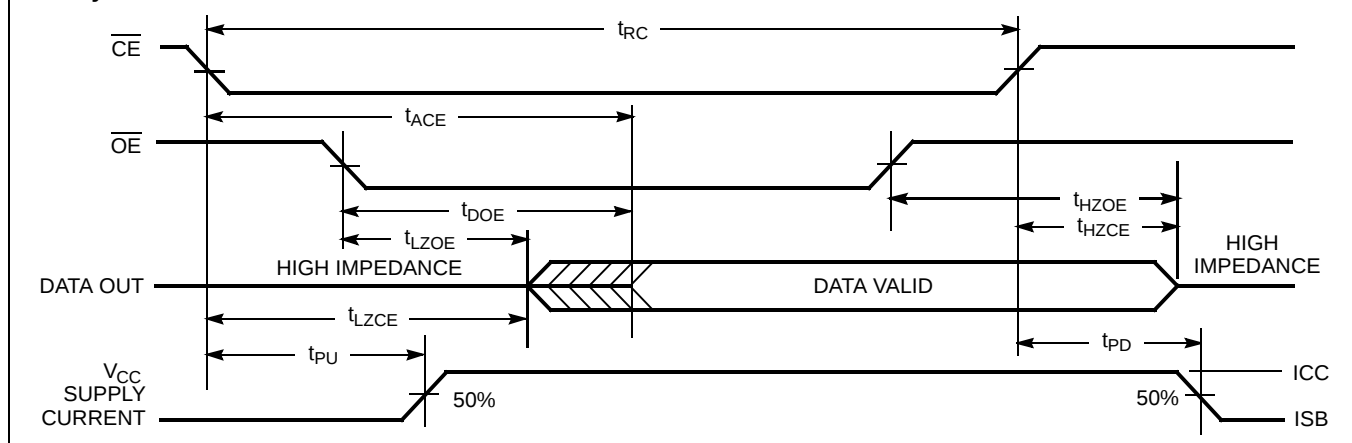
Parameter	Description	7C199-25		7C199-35		7C199-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HZCE}	$\overline{CE}$ HIGH to High-Z ^[8, 9]		11		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		20		20		25	ns
Write Cycle^[10,11]								
t_{WC}	Write Cycle Time	25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	18		22		22		ns
t_{AW}	Address Set-up to Write End	20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	18		22		22		ns
t_{SD}	Data Set-up to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z ^[9]		11		15		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z ^[8]	3		3		3		ns

Switching Waveforms

Read Cycle No. 1^[12, 13]



Read Cycle No. 2^[13, 14]

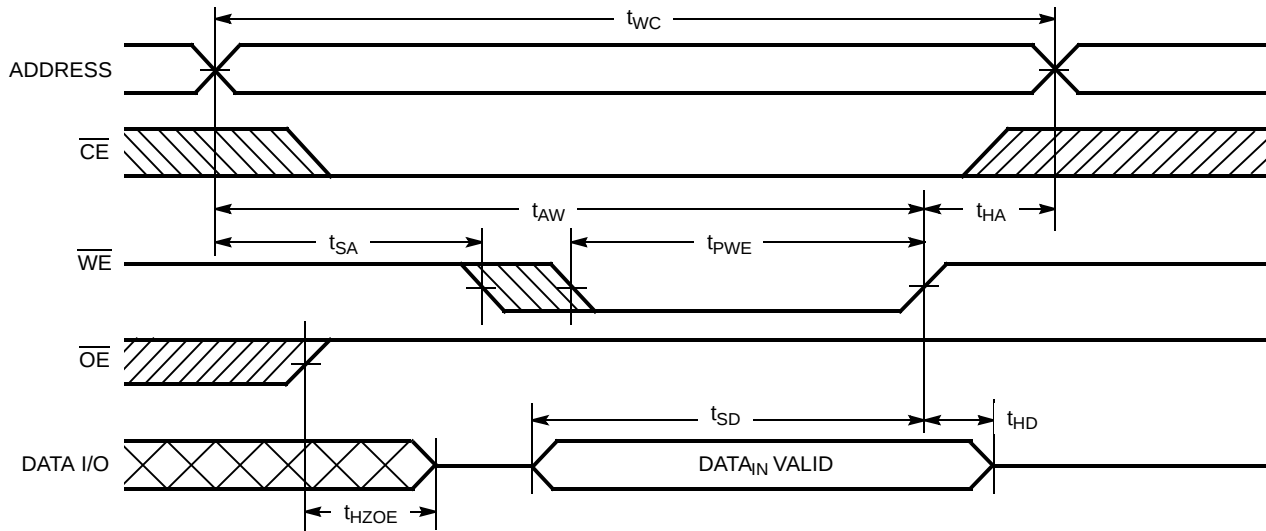


Notes:

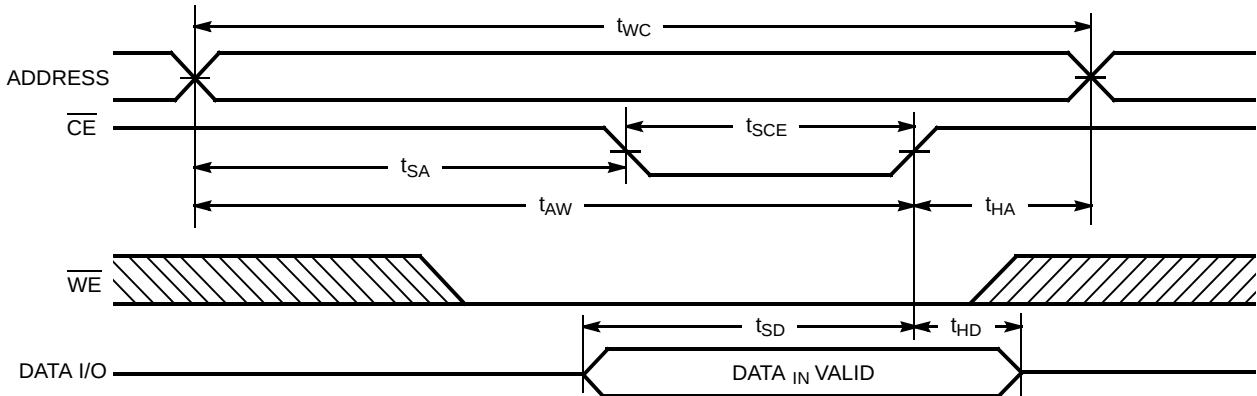
12. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

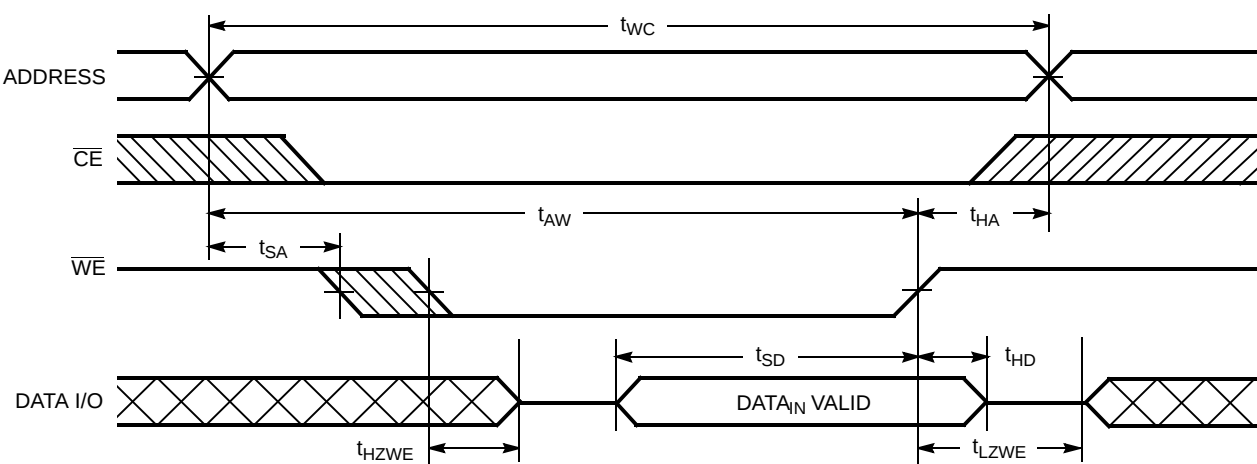
Write Cycle No. 1 (WE Controlled)^[10, 15, 16]



Write Cycle No. 2 (CE Controlled)^[9, 15, 16]



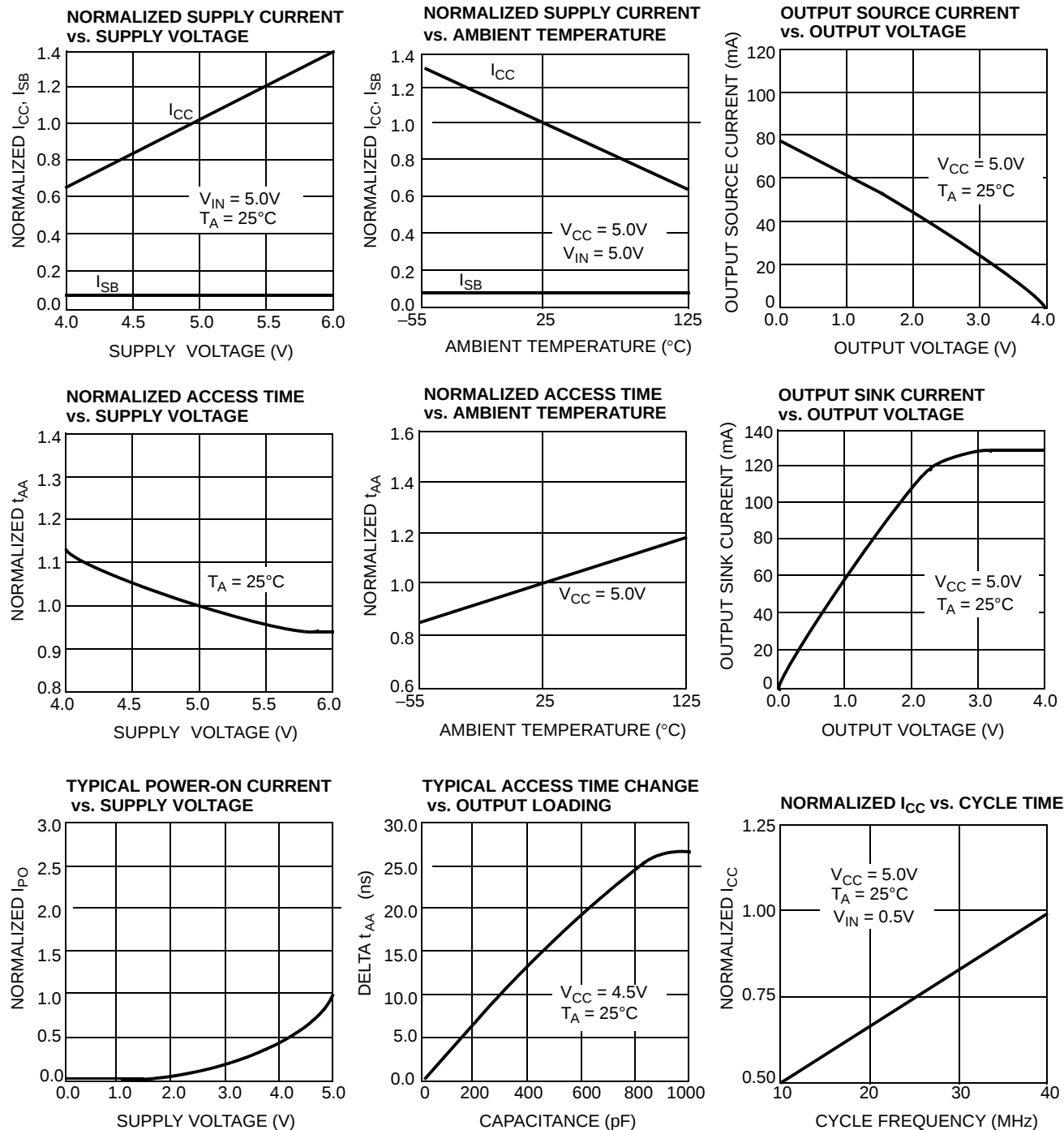
Write Cycle No. 3 (WE Controlled OE LOW)^[11, 16]



Notes:

15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
16. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



Truth Table

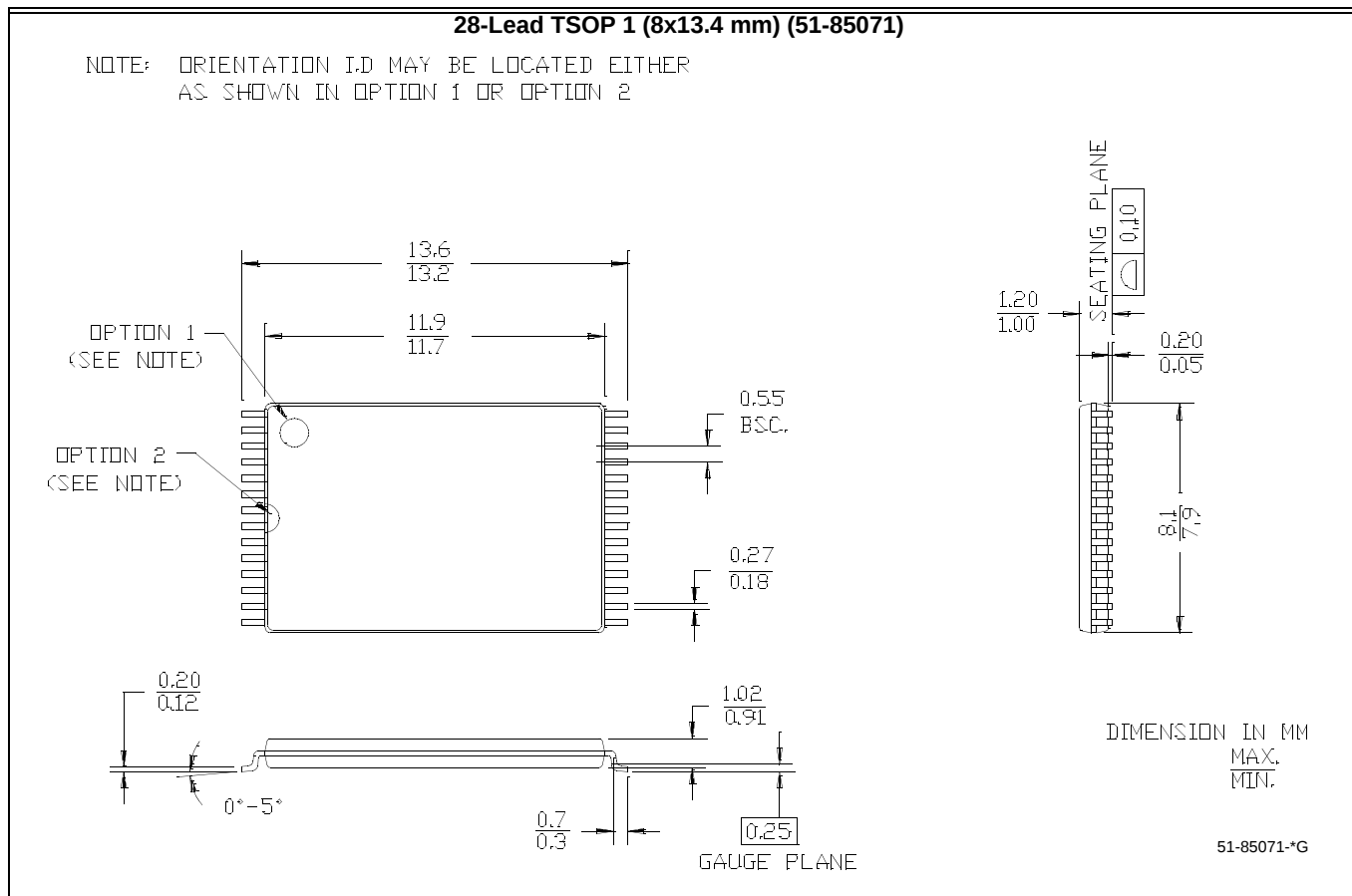
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Output disabled	Active (I_{CC})

Ordering Information

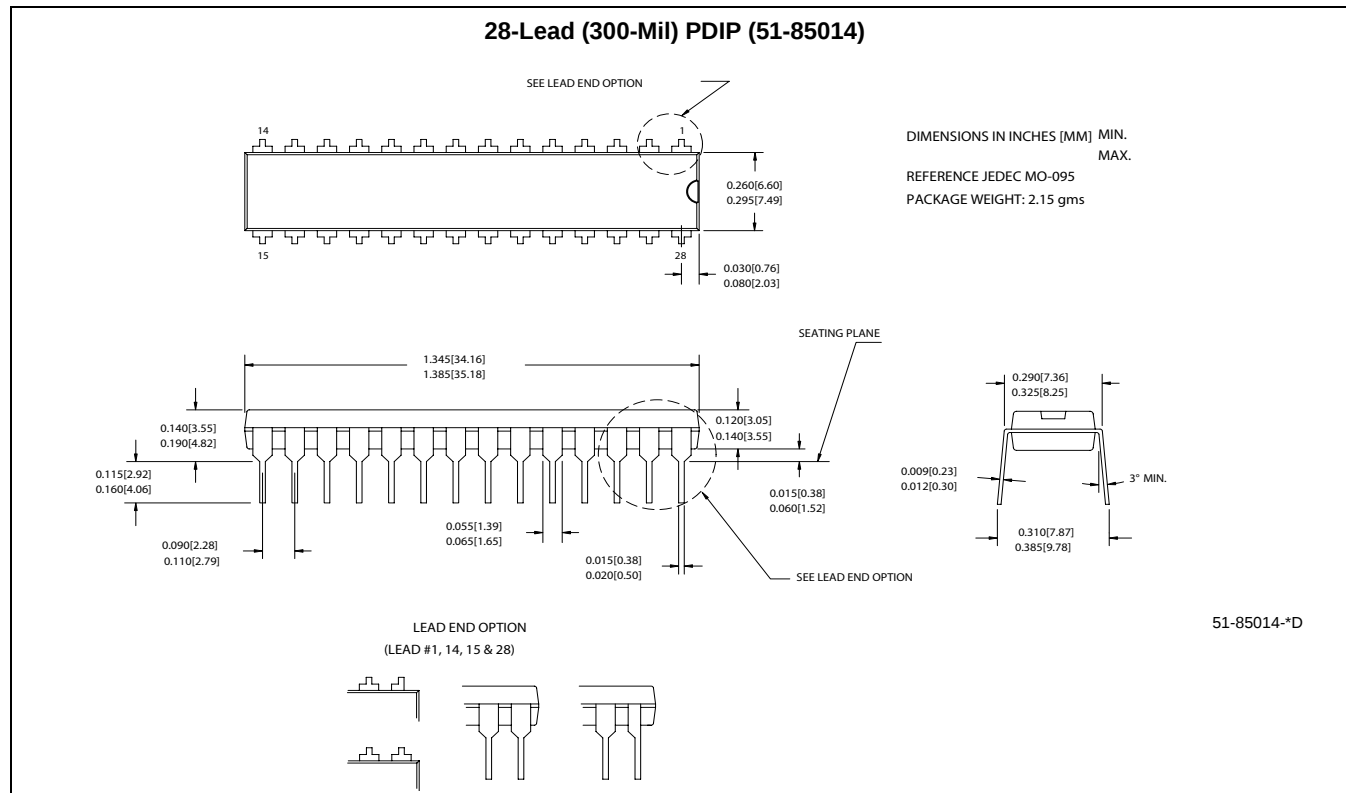
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C199N-12ZXC	51-85071	28-Lead TSOP 1 (Pb-free)	Commercial
15	CY7C199N-15ZXC	51-85071	28-Lead TSOP 1 (Pb-free)	Commercial
	CY7C199NL-15ZXC	51-85071	28-Lead TSOP 1 (Pb-free)	
20	CY7C199N-20PXC	51-85014	28-Lead (300-Mil) Molded DIP (Pb-free)	Commercial
	CY7C199N-20ZXC	51-85071	28-Lead TSOP 1 (Pb-free)	
25	CY7C199N-25PXC	51-85014	28-Lead (300-Mil) Molded DIP (Pb-free)	Commercial
35	CY7C199N-35PXC	51-85014	28-Lead (300-Mil) Molded DIP (Pb-free)	
55	CY7C199N-55PXC	51-85014	28-Lead (300-Mil) Molded DIP (Pb-free)	

Contact your Local Cypress sales representative for availability of these parts

Package Diagrams



Package Diagrams (continued)



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Document History Page

Document Title: CY7C199N 32K x 8 Static RAM Document Number: 001-06493				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	423877	See ECN	NXR	New Data Sheet