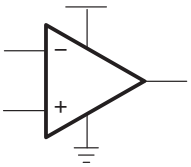
- **Rail-To-Rail Input/Output**
- **Wide Bandwidth . . . 3 MHz**
- **High Slew Rate . . . 2.4 V/μs**
- **Supply Voltage Range . . . 2.7 V to 16 V**
- **Supply Current . . . 550 μA/Channel**
- **Low Power Shutdown Mode**
  $I_{DD(SHDN)}$ . . . 25 μA/Channel
- **Input Noise Voltage . . . 39 nV/$\sqrt{Hz}$**
- **Input Bias Current . . . 1 pA**
- **Specified Temperature Range**
  −40°C to 125°C . . . Industrial Grade
- **Ultrasmall Packaging**
  5 or 6 Pin SOT-23 (TLV2370/1)
  8 or 10 Pin MSOP (TLV2372/3)

Operational Amplifier



description

The TLV237x single supply operational amplifiers provide rail-to-rail input and output capability. The TLV237x takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range while adding the rail-to-rail output swing feature. The TLV237x also provides 3-MHz bandwidth from only 550 μA. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from (±8 V supplies down to ±1.35 V) a variety of rechargeable cells.

The CMOS inputs enable use in high-impedance sensor interfaces, with the lower voltage operation making an ideal alternative for the TLC227x in battery-powered applications. The rail-to-rail input stage further increases its versatility. The TLV237x is the seventh member of a rapidly growing number of RRIO products available from TI, and it is the first to allow operation up to 16-V rails with good ac performance.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

The 2.7-V operation makes the TLV237x compatible with Li-Ion powered systems and the operating supply voltage range of many micro-power microcontrollers available today including TI's MSP430.

SELECTION OF SIGNAL AMPLIFIER PRODUCTS†

DEVICE	V_{DD} (V)	V_{IO} (μV)	Iq/Ch (μA)	I_{IB} (pA)	GBW (MHz)	SR (V/μs)	SHUTDOWN	RAIL-TO-RAIL	SINGLES/DUALS/QUADS
TLV237x	2.7−16	500	550	1	3	2.4	Yes	I/O	S/D/Q
TLC227x	4−16	300	1100	1	2.2	3.6	—	O	D/Q
TLV27x	2.7−16	500	550	1	3	2.4	—	O	S/D/Q
TLC27x	3−16	1100	675	1	1.7	3.6	—	—	S/D/Q
TLV246x	2.7−6	150	550	1300	6.4	1.6	Yes	I/O	S/D/Q
TLV247x	2.7−6	250	600	2	2.8	1.5	Yes	I/O	S/D/Q
TLV244x	2.7−10	300	725	1	1.8	1.4	—	O	D/Q

† Typical values measured at 5 V, 25°C

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FAMILY PACKAGE TABLE(1)

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES					SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	SOIC	SOT-23	TSSOP	MSOP		
TLV2370	1	8	8	6	—	—	Yes	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2371	1	8	8	5	—	—	—	
TLV2372	2	8	8	—	—	8	—	
TLV2373	2	14	14	—	—	10	Yes	
TLV2374	4	14	14	—	14	—	—	
TLV2375	4	16	16	—	16	—	Yes	

TLV2370 and TLV2371 AVAILABLE OPTIONS(1)

T_A	V_{IO}MAX AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE (D)†	SOT-23		PLASTIC DIP (P)
			(DBV)‡	SYMBOL	
−40°C to 125°C	4.5 mV	TLV2370ID TLV2371ID	TLV2370IDBV TLV2371IDBV	VBFI VBGI	TLV2370IP TLV2371IP

† This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2370IDR).
‡ This package is only available taped and reeled. For standard quantities (3,000 pieces per reel), add an **R** suffix (e.g., TLV2370IDBVR). For smaller quantities (250 pieces per mini-reel), add a **T** suffix to the part number (e.g., TLV2370IDBVT).

TLV2372 AND TLV2373 AVAILABLE OPTIONS(1)

T_A	V_{IO}MAX AT 25°C	PACKAGED DEVICES						
		SMALL OUTLINE (D)§	MSOP				PLASTIC DIP (N)	PLASTIC DIP (P)
			(DGK)§	SYMBOL	(DGS)§	SYMBOL		
−40°C to 125°C	4.5 mV	TLV2372ID TLV2373ID	TLV2372IDGK —	APG —	— TLV2373IDGS	— API	— TLV2373IN	TLV2372IP —

§ This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2372IDR).

TLV2374 and TLV2375 AVAILABLE OPTIONS(1)

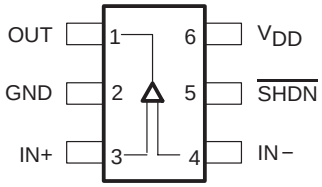
T_A	V_{IO}MAX AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D)¶	PLASTIC DIP (N)	TSSOP (PW)¶
−40°C to 125°C	4.5 mV	TLV2374ID TLV2375ID	TLV2374IN TLV2375IN	TLV2374IPW TLV2375IPW

¶ This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2374IDR).

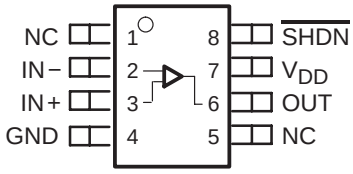
1. For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

TLV237x PACKAGE PINOUTS(1)

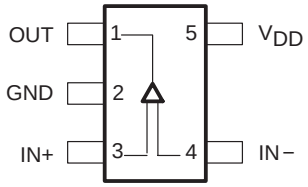
TLV2370
DBV PACKAGE
(TOP VIEW)



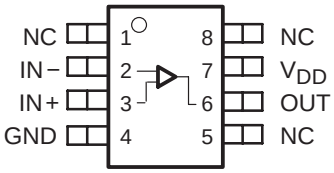
TLV2370
D OR P PACKAGE
(TOP VIEW)



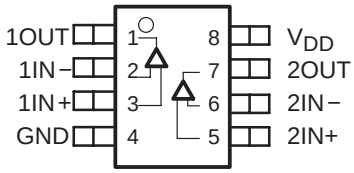
TLV2371
DBV PACKAGE
(TOP VIEW)



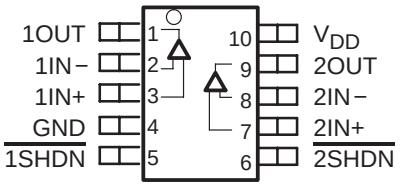
TLV2371
D OR P PACKAGE
(TOP VIEW)



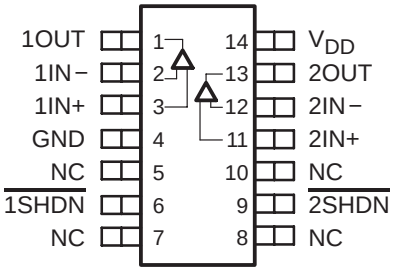
TLV2372
D, DGK, OR P PACKAGE
(TOP VIEW)



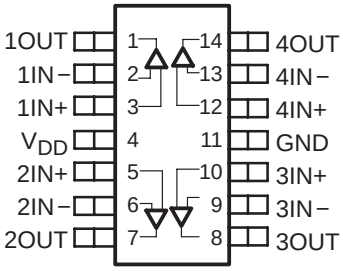
TLV2373
DGS PACKAGE
(TOP VIEW)



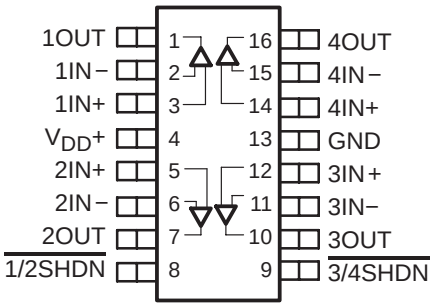
TLV2373
D OR N PACKAGE
(TOP VIEW)



TLV2374
D, N, OR PW PACKAGE
(TOP VIEW)

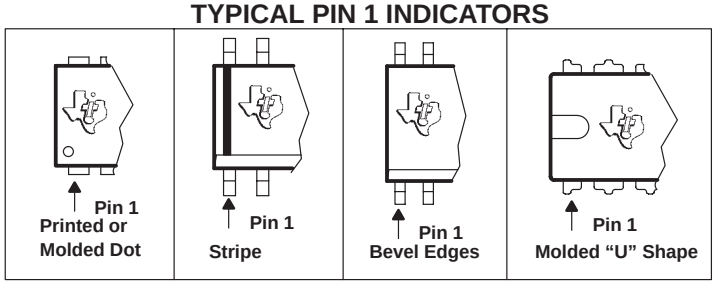


TLV2375
D, N, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

TYPICAL PIN 1 INDICATORS



NOTE: (1) If there is not a Pin 1 indicator, turn device to enable reading the symbol from the left to right. Pin 1 is at the lower left corner of the device.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 16.5 V
Differential input voltage, V_{ID} . . . . . $\pm V_{DD}$
Input voltage range, V_I (see Note 1) . . . . . −0.2 V to V_{DD} + 0.2 V
Input current range, I_I . . . . . ±10 mA
Output current range, I_O . . . . . ±100 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: I-suffix . . . . . −40°C to 125°C
Maximum junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \le 25°C$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
D (16)	25.7	114.7	1090 mW
DBV (5)	55	324.1	385 mW
DBV (6)	55	294.3	425 mW
DGK (8)	54.23	259.96	481 mW
DGS (10)	54.1	257.71	485 mW
N (14, 16)	32	78	1600 mW
P (8)	41	104	1200 mW
PW (14)	29.3	173.6	720 mW
PW (16)	28.7	161.4	774 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	16	V
	Split supply	±1.35	±8	
Common-mode input voltage range, V_{ICR}		0	V_{DD}	V
Operating free-air temperature, T_A	I-suffix	−40	125	°C
Turnon voltage level, $V_{(ON)}$, relative to GND pin voltage			2	V
Turnoff voltage level, $V_{(OFF)}$, relative to GND pin voltage		0.8		V

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V, 5 V, and 15 V (unless otherwise noted)

dc performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_S = 50\ \Omega$		25°C		2	4.5	mV
				Full range			6	
α_{VIO}	Offset voltage drift			25°C		2		μV/°C
CMRR	Common-mode rejection ratio	V_{IC} = 0 to V_{DD}, $R_S = 50\ \Omega$	V_{DD} = 2.7 V	25°C	50	68		dB
				Full range	49			
		V_{IC} = 0 to V_{DD}−1.35V, $R_S = 50\ \Omega$		25°C	56	70		
				Full range	54			
		V_{IC} = 0 to V_{DD}, $R_S = 50\ \Omega$,	V_{DD} = 5 V	25°C	55	72		
				Full range	54			
		V_{IC} = 0 to V_{DD}−1.35V, $R_S = 50\ \Omega$,		25°C	67	80		
				Full range	64			
		V_{IC} = 0 to V_{DD}, $R_S = 50\ \Omega$,	V_{DD} = 15 V	25°C	64	82		
				Full range	63			
		V_{IC} = 0 to V_{DD}−1.35V, $R_S = 50\ \Omega$,		25°C	67	84		
				Full range	66			
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)} = V_{DD}/2$, $R_L = 10\ k\Omega$	V_{DD} = 2.7 V	25°C	98	106		dB
				Full range	76			
			V_{DD} = 5 V	25°C	100	110		
				Full range	86			
			V_{DD} = 15 V	25°C	81	83		
				Full range	79			

input characteristics

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{IO}	Input offset current	V_{DD} = 15 V, $V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$	25°C		1	60	pA
			70°C			100	
			125°C			1000	
I_{IB}	Input bias current		25°C		1	60	pA
			70°C			100	
			125°C			1000	
$r_{i(d)}$	Differential input resistance		25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 21 kHz	25°C		8		pF

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V, 5 V, and 15 V (unless otherwise noted) (continued)

output characteristics

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_{IC} = V_{DD}/2$, $I_{OH} = -1$ mA	V_{DD} = 2.7 V	25°C	2.55	2.58		V
				Full range	2.48			
			V_{DD} = 5 V	25°C	4.9	4.93		
				Full range	4.85			
			V_{DD} = 15 V	25°C	14.92	14.96		
				Full range	14.9			
		$V_{IC} = V_{DD}/2$, $I_{OH} = -5$ mA	V_{DD} = 2.7 V	25°C	1.9	2		
				Full range	1.6			
			V_{DD} = 5 V	25°C	4.6	4.68		
				Full range	4.5			
			V_{DD} = 15 V	25°C	14.7	14.8		
				Full range	14.6			
V_{OL}	Low-level output voltage	$V_{IC} = V_{DD}/2$, I_{OL} = 1 mA	V_{DD} = 2.7 V	25°C		0.1	0.15	V
				Full range			0.22	
			V_{DD} = 5 V	25°C		0.05	0.1	
				Full range			0.15	
			V_{DD} = 15 V	25°C		0.05	0.08	
				Full range			0.1	
		$V_{IC} = V_{DD}/2$, I_{OL} = 5 mA	V_{DD} = 2.7 V	25°C		0.52	0.7	
				Full range			1.1	
			V_{DD} = 5 V	25°C		0.28	0.4	
				Full range			0.5	
			V_{DD} = 15 V	25°C		0.19	0.3	
				Full range			0.35	
I_O	Output current	V_{DD} = 2.7 V, V_O = 0.5 V from rail	Positive rail	25°C		4		mA
			Negative rail	25°C		5		
		V_{DD} = 5 V, V_O = 0.5 V from rail	Positive rail	25°C		7		
			Negative rail	25°C		8		
		V_{DD} = 15 V, V_O = 0.5 V from rail	Positive rail	25°C		16		
			Negative rail	25°C		15		

power supply

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
I_{DD}	Supply current (per channel)	$V_O = V_{DD}/2$,	V_{DD} = 2.7 V	25°C		470	560	μA
			V_{DD} = 5 V	25°C		550	660	
			V_{DD} = 15 V	25°C		750	900	
				Full range			1200	
PSRR	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 15 V, No load	$V_{IC} = V_{DD}/2$,	25°C	70	80		dB
				Full range	65			

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V, 5 V, and 15 V (unless otherwise noted) (continued)

dynamic performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	R_L = 2 kΩ, C_L = 10 pF	V_{DD} = 2.7 V	25°C		2.4		MHz
			V_{DD} = 5 V to 15 V	25°C		3		
SR	Slew rate at unity gain	$V_{O(PP)} = V_{DD}/2$, C_L = 50 pF, R_L = 10 kΩ	V_{DD} = 2.7 V	25°C	1.4	2		V/μs
				Full range	1			
			V_{DD} = 5 V	25°C	1.6	2.4		V/μs
				Full range	1.2			
			V_{DD} = 15 V	25°C	1.9	2.1		V/μs
				Full range	1.4			
ϕ_m	Phase margin	R_L = 2 kΩ,	C_L = 100 pF	25°C		65°		
	Gain margin	R_L = 2 kΩ,	C_L = 10 pF	25°C		18		dB
t_s	Settling time	V_{DD} = 2.7 V, $V_{(STEP)PP}$ = 1 V, A_V = −1, C_L = 10 pF, R_L = 2 kΩ	0.1%	25°C		2.9		μs
		V_{DD} = 5 V, 15 V, $V_{(STEP)PP}$ = 1 V, A_V = −1, C_L = 47 pF, R_L = 2 kΩ	0.1%			2		

noise/distortion performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion plus noise	V_{DD} = 2.7 V, $V_{O(PP)} = V_{DD}/2$ V, R_L = 2 kΩ, f = 10 kHz	A_V = 1	25°C		0.02%		
			A_V = 10			0.05%		
			A_V = 100			0.18%		
		V_{DD} = 5 V, 15 V, $V_{O(PP)} = V_{DD}/2$ V, R_L = 2 kΩ, f = 10 kHz	A_V = 1	25°C		0.02%		
			A_V = 10			0.09%		
			A_V = 100			0.5%		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		39		nV/√Hz
		f = 10 kHz				35		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.6		fA/√Hz

shutdown characteristics

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLV2370, TLV2373, TLV2375) (per channel)	V_{DD} = 2.7 V, 5 V, $\overline{SHDN}$ = 0 V	25°C		25	30	μA
			Full range			35	
		V_{DD} = 15 V, $\overline{SHDN}$ = 0 V	25°C		40	45	μA
			Full range			50	
$t_{(on)}$	Amplifier turnon time (see Note 2)	R_L = 2 kΩ	25°C		0.8		μs
$t_{(off)}$	Amplifier turnoff time (see Note 2)		25°C		1		μs

NOTE: Disable time and enable time are defined as the interval between application of the logic signal to the $\overline{SHDN}$ terminal and the point at which the supply current has reached one half of its final value.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2, 3
CMRR	Common-mode rejection ratio	vs Frequency	4
	Input bias and offset current	vs Free-air temperature	5
V_{OL}	Low-level output voltage	vs Low-level output current	6, 8, 10
V_{OH}	High-level output voltage	vs High-level output current	7, 9, 11
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	12
I_{DD}	Supply current	vs Supply voltage	13
PSRR	Power supply rejection ratio	vs Frequency	14
A_{VD}	Differential voltage gain & phase	vs Frequency	15
	Gain-bandwidth product	vs Free-air temperature	16
SR	Slew rate	vs Supply voltage	17
		vs Free-air temperature	18
ϕ_m	Phase margin	vs Capacitive load	19
V_n	Equivalent input noise voltage	vs Frequency	20
	Voltage-follower large-signal pulse response		21, 22
	Voltage-follower small-signal pulse response		23
	Inverting large-signal response		24, 25
	Inverting small-signal response		26
	Crosstalk	vs Frequency	27
	Shutdown forward & reverse isolation	vs Frequency	28
$I_{DD(SHDN)}$	Shutdown supply current	vs Supply voltage	29
$I_{DD(SHDN)}$	Shutdown pin leakage current	vs Shutdown pin voltage	30
$I_{DD(SHDN)}$	Shutdown supply current/output voltage	vs Time	31, 32

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

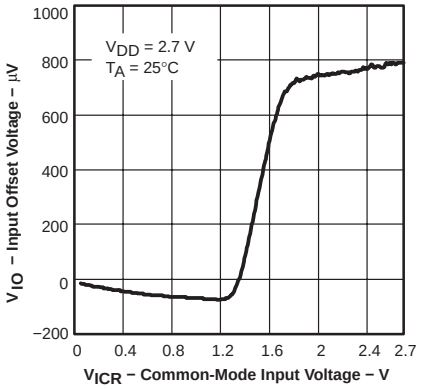


Figure 1

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

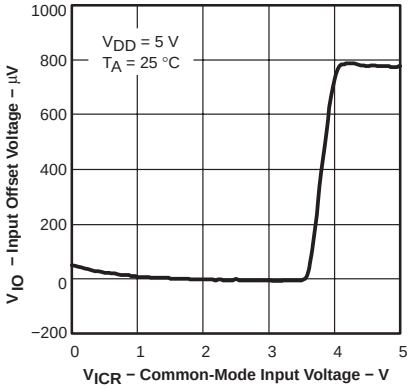


Figure 2

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

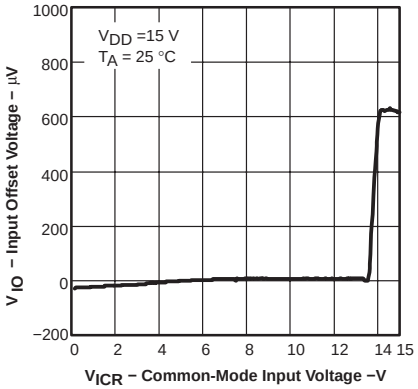


Figure 3

COMMON-MODE REJECTION RATIO vs FREQUENCY

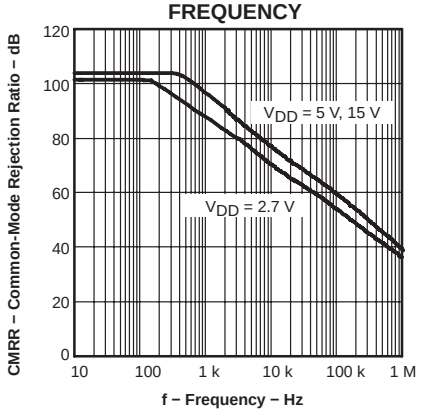


Figure 4

INPUT BIAS/OFFSET CURRENT vs FREE-AIR TEMPERATURE

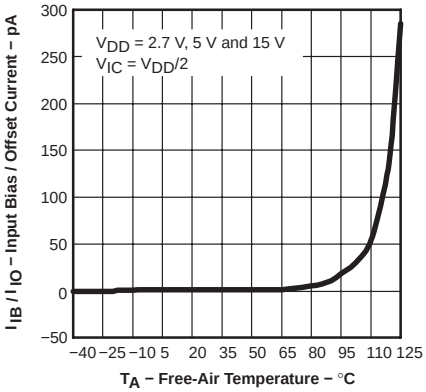


Figure 5

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

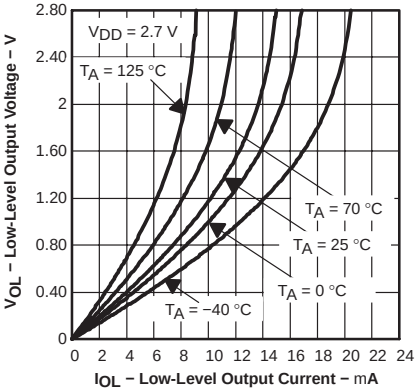


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

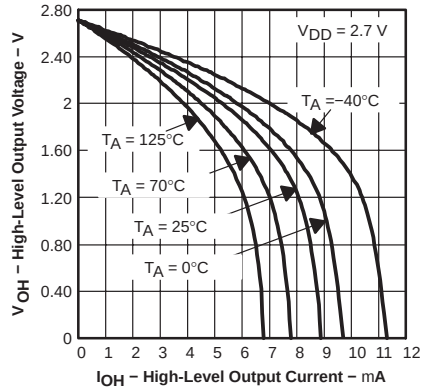


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

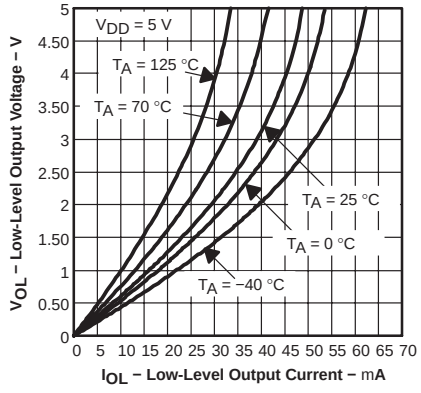


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

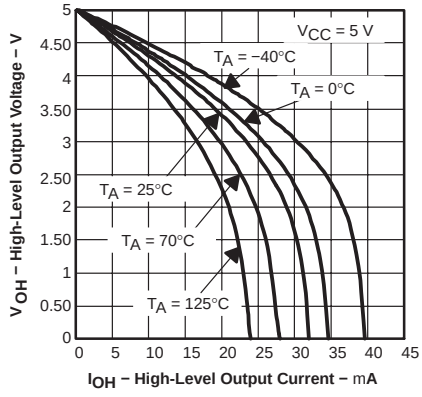


Figure 9

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

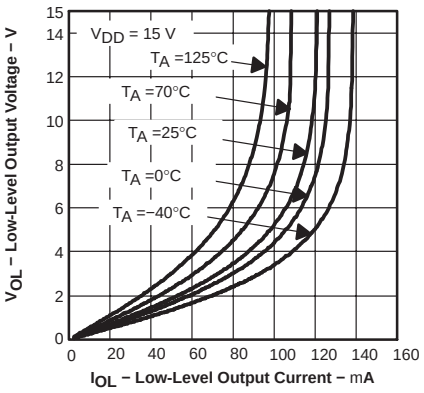


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

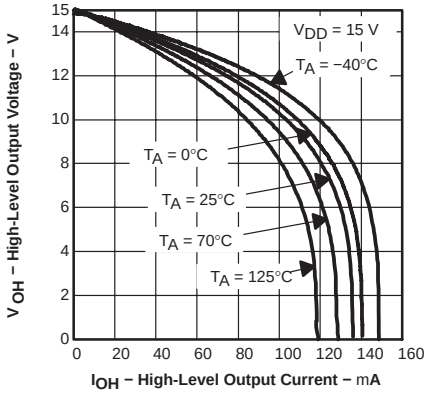


Figure 11

PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

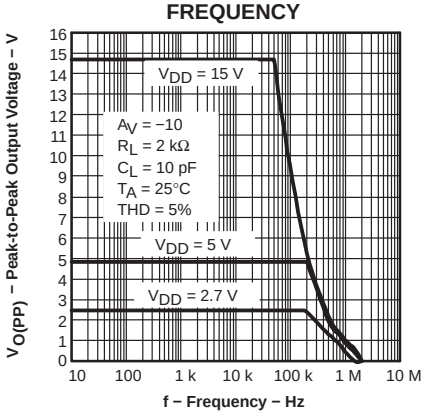


Figure 12

SUPPLY CURRENT vs SUPPLY VOLTAGE

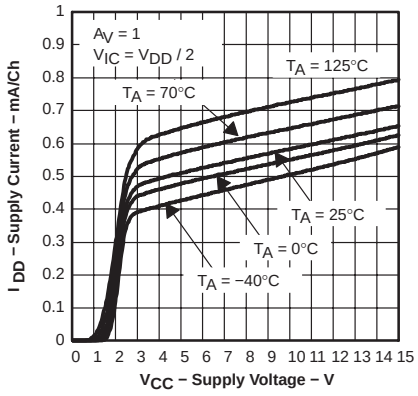


Figure 13

POWER SUPPLY REJECTION RATIO vs FREQUENCY

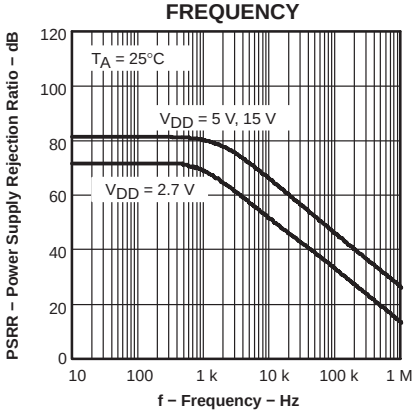


Figure 14

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

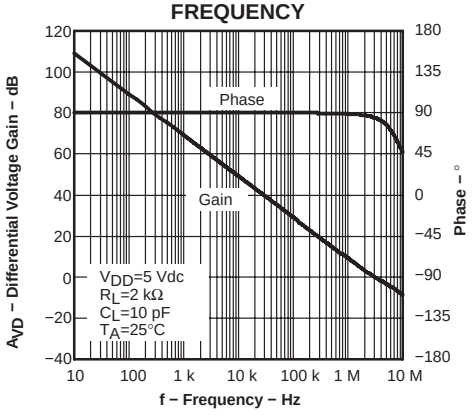


Figure 15

GAIN BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

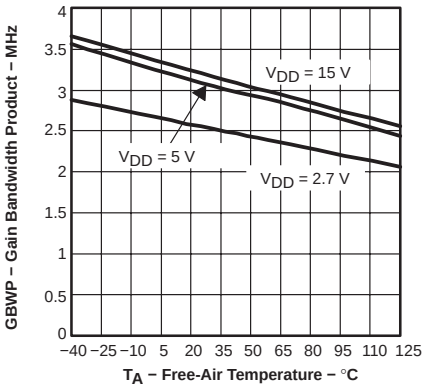


Figure 16

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TYPICAL CHARACTERISTICS

SLEW RATE vs SUPPLY VOLTAGE

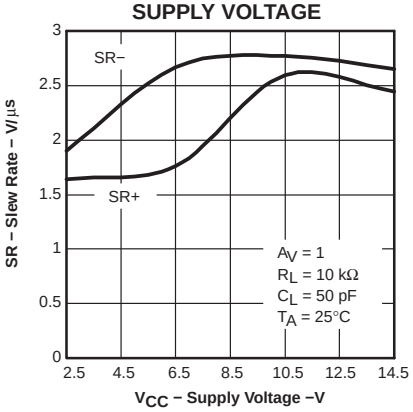

Figure 17

SLEW RATE vs FREE-AIR TEMPERATURE

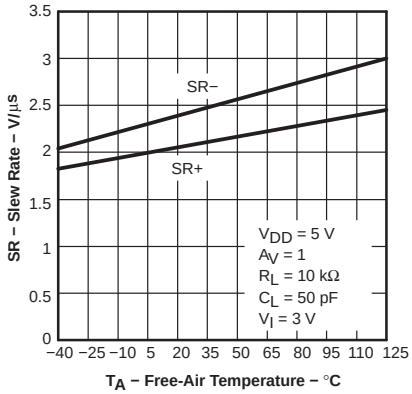

Figure 18

PHASE MARGIN vs CAPACITIVE LOAD

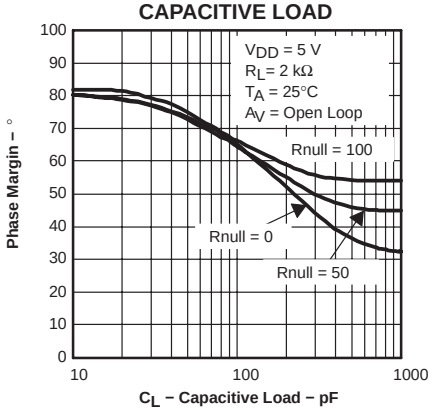

Figure 19

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

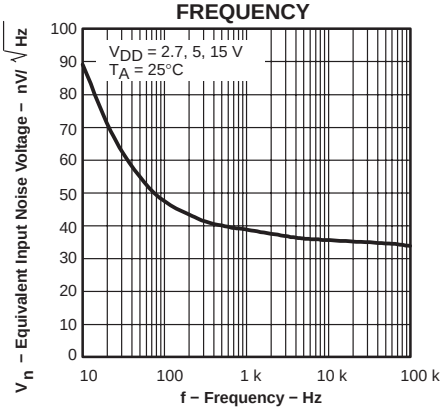

Figure 20

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

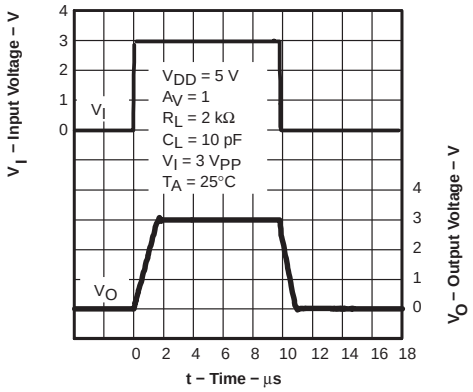

Figure 21

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

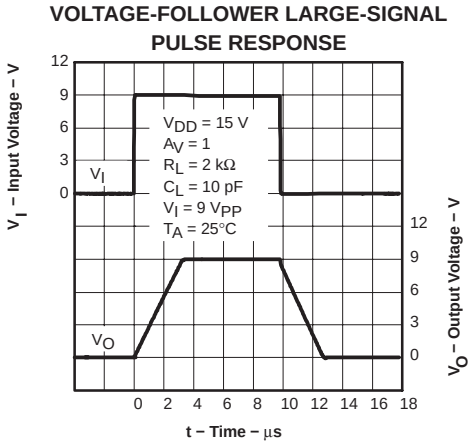

Figure 22

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

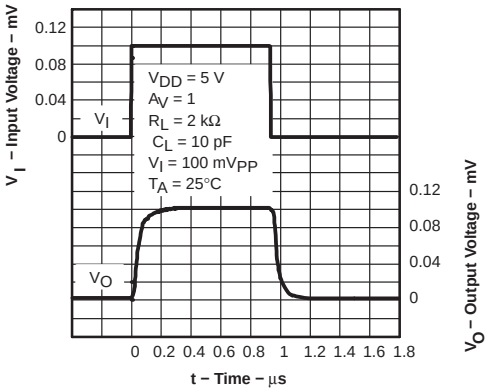

Figure 23

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL RESPONSE

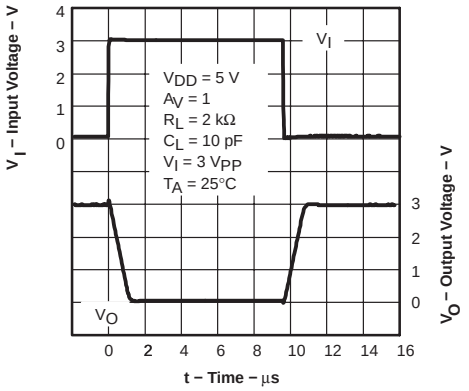

Figure 24

INVERTING LARGE-SIGNAL RESPONSE

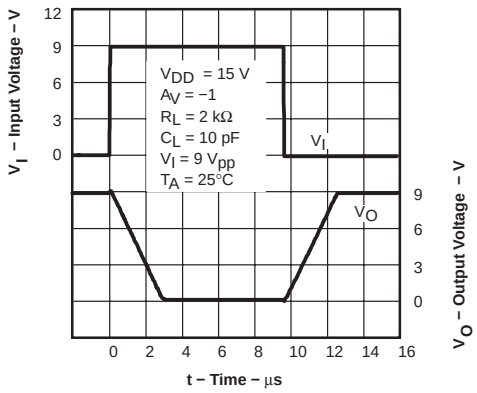

Figure 25

INVERTING SMALL-SIGNAL RESPONSE

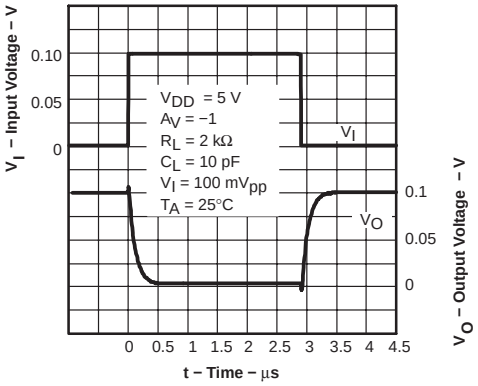

Figure 26

CROSSTALK vs FREQUENCY

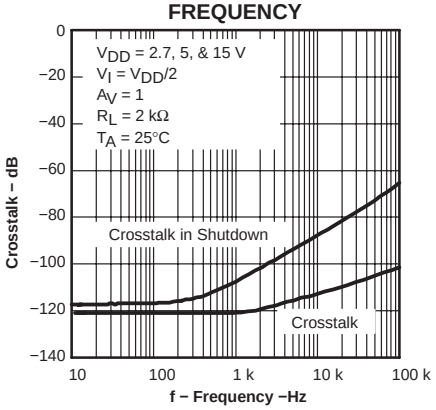

Figure 27

SHUTDOWN FORWARD AND REVERSE ISOLATION vs FREQUENCY

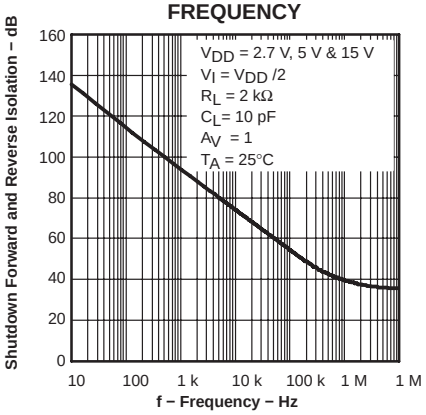

Figure 28

SHUTDOWN SUPPLY CURRENT vs SUPPLY VOLTAGE

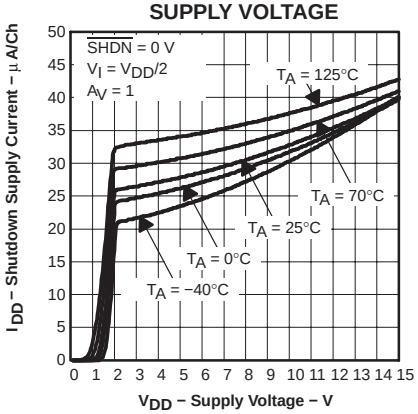

Figure 29

SHUTDOWN PIN LEAKAGE CURRENT vs SHUTDOWN PIN VOLTAGE

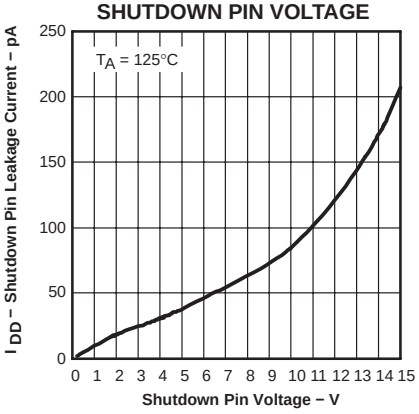

Figure 30

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TYPICAL CHARACTERISTICS

SHUTDOWN SUPPLY CURRENT/OUTPUT VOLTAGE vs TIME

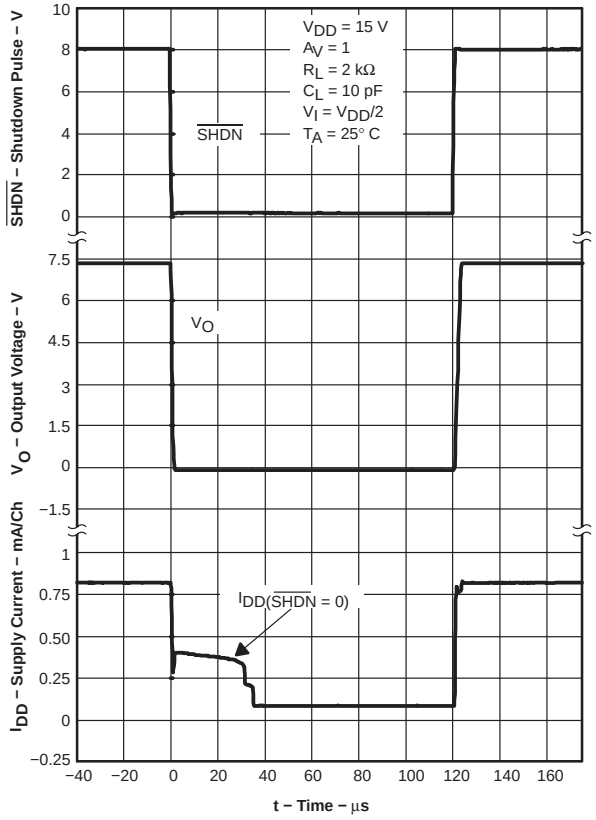


Figure 31

SHUTDOWN SUPPLY CURRENT/OUTPUT VOLTAGE vs TIME

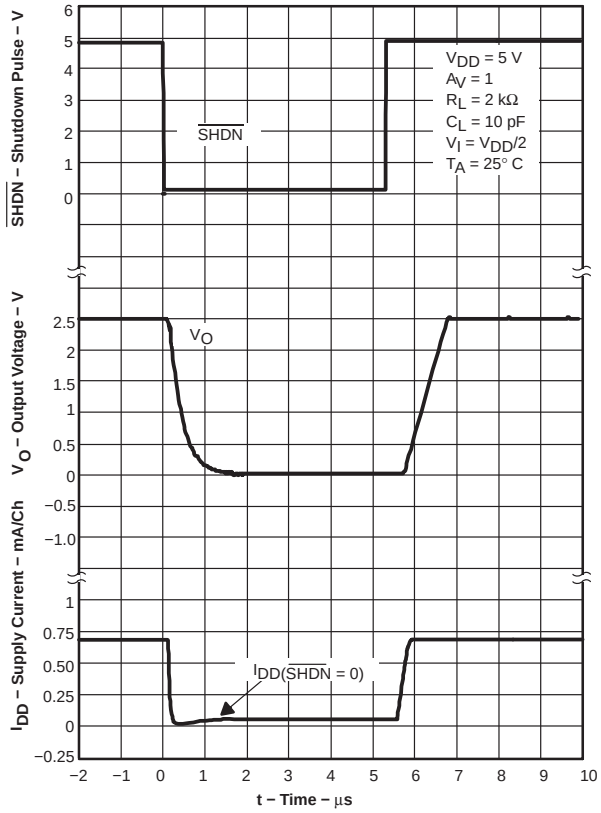


Figure 32

APPLICATION INFORMATION

rail-to-rail input operation

The TLV237x input stage consists of two differential transistor pairs, NMOS and PMOS, that operate together to achieve rail-to-rail input operation. The transition point between these two pairs can be seen in Figure 1, Figure 2, and Figure 3 for a 2.7-V, 5-V, and 15-V supply. As the common-mode input voltage approaches the positive supply rail, the input pair switches from the PMOS differential pair to the NMOS differential pair. This transition occurs approximately 1.35 V from the positive rail and results in a change in offset voltage due to different device characteristics between the NMOS and PMOS pairs. If the input signal to the device is large enough to swing between both rails, this transition results in a reduction in common-mode rejection ratio (CMRR). If the input signal does not swing between both rails, it is best to bias the signal in the region where only one input pair is active. This is the region in Figure 1 through Figure 3 where the offset voltage varies slightly across the input range and optimal CMRR can be achieved. This has the greatest impact when operating from a 2.7-V supply voltage.

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 33. A minimum value of 20 Ω should work well for most applications.

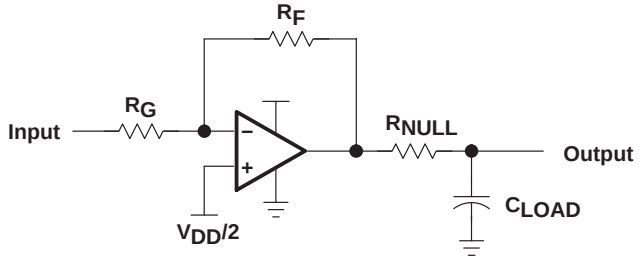
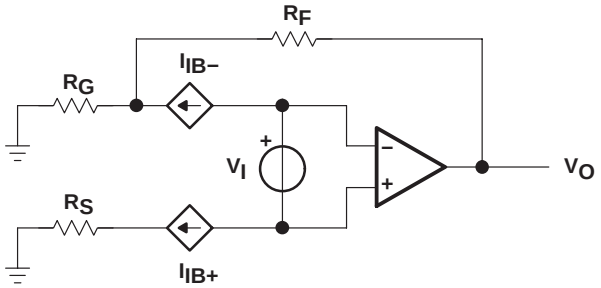


Figure 33. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+} R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-} R_F$$

Figure 34. Output Offset Voltage Model

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APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 35).

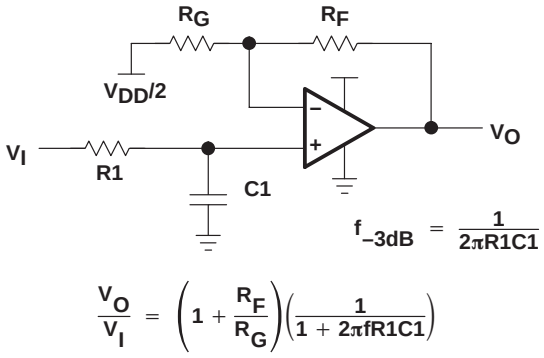


Figure 35. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

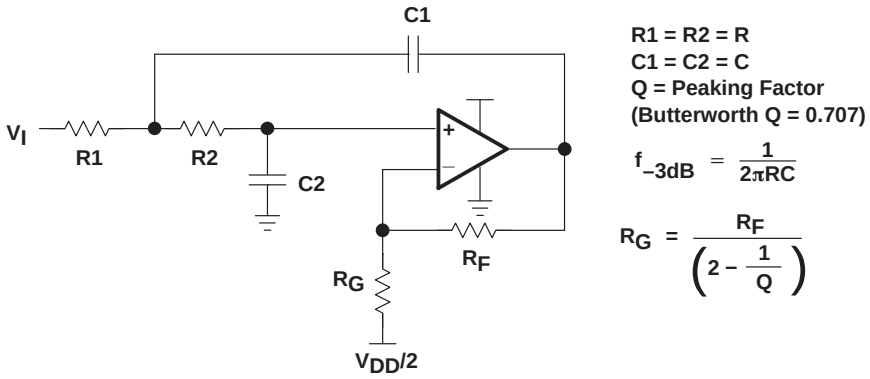


Figure 36. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV237x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

shutdown function

Three members of the TLV237x family (TLV2370/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 25 μA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown.

APPLICATION INFORMATION

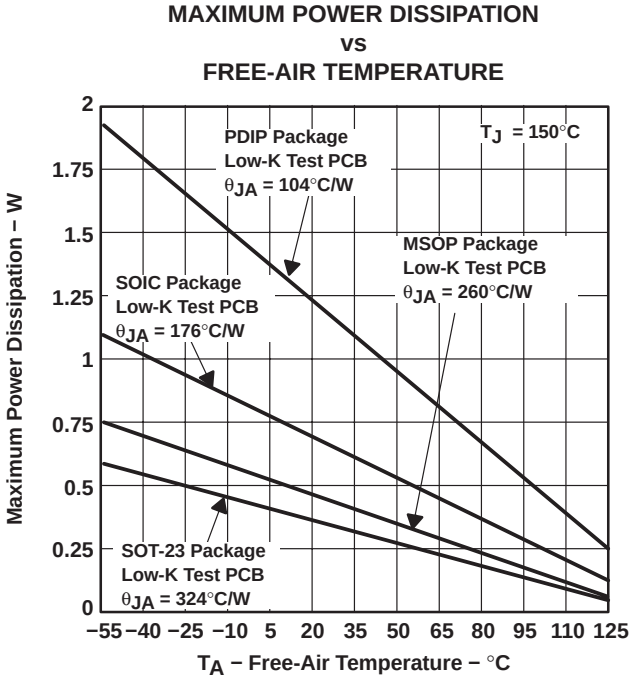
general power dissipation considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 37 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of TLV237x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 37. Maximum Power Dissipation vs Free-Air Temperature

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2370ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2370I	Samples
TLV2370IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBFI	Samples
TLV2370IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBFI	Samples
TLV2370IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBFI	Samples
TLV2370IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBFI	Samples
TLV2370IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2370I	Samples
TLV2370IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2370I	Samples
TLV2370IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	2370I	Samples
TLV2370IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	2370I	Samples
TLV2371ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2371I	Samples
TLV2371IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBGI	Samples
TLV2371IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBGI	Samples
TLV2371IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBGI	Samples
TLV2371IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBGI	Samples
TLV2371IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2371I	Samples
TLV2371IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2371I	Samples
TLV2371IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2371I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2371IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	2371I	Samples
TLV2371IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	2371I	Samples
TLV2372ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2372I	Samples
TLV2372IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2372I	Samples
TLV2372IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	APG	Samples
TLV2372IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	APG	Samples
TLV2372IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	APG	Samples
TLV2372IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	APG	Samples
TLV2372IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2372I	Samples
TLV2372IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2372I	Samples
TLV2372IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	2372I	Samples
TLV2372IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	2372I	Samples
TLV2373ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2373I	Samples
TLV2373IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2373I	Samples
TLV2373IDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	API	Samples
TLV2373IDGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	API	Samples
TLV2373IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	API	Samples
TLV2373IDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	API	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2373IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2373I	Samples
TLV2373IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2373I	Samples
TLV2373IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2373I	Samples
TLV2374-W	ACTIVE	WAFERSALE	YS	0		TBD	Call TI	Call TI			Samples
TLV2374ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374I	Samples
TLV2374IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374I	Samples
TLV2374IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374I	Samples
TLV2374IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374I	Samples
TLV2374IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	2374I	Samples
TLV2374INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	2374I	Samples
TLV2374IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374I	Samples
TLV2374IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374I	Samples
TLV2374IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374I	Samples
TLV2374IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374I	Samples
TLV2375ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2375I	Samples
TLV2375IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2375I	Samples
TLV2375IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2375I	Samples
TLV2375IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2375I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2375IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	2375I	Samples
TLV2375IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2375I	Samples
TLV2375IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2375I	Samples
TLV2375IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2375I	Samples
TLV2375IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2375I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV2371, TLV2372, TLV2374 :

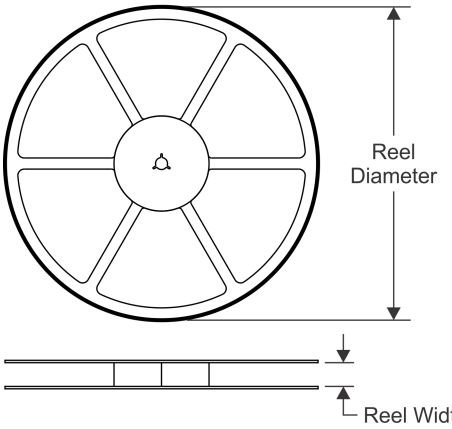
- Automotive: TLV2371-Q1, TLV2372-Q1, TLV2374-Q1
- Enhanced Product: TLV2371-EP, TLV2374-EP

NOTE: Qualified Version Definitions:

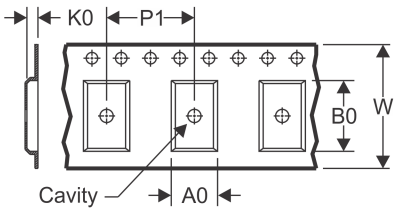
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

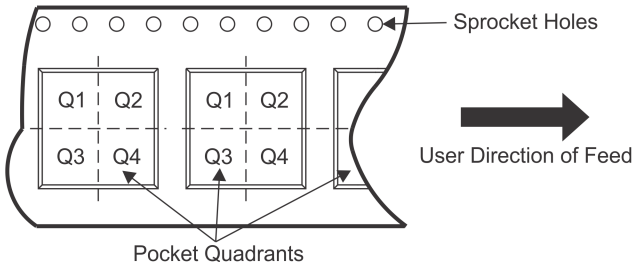


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

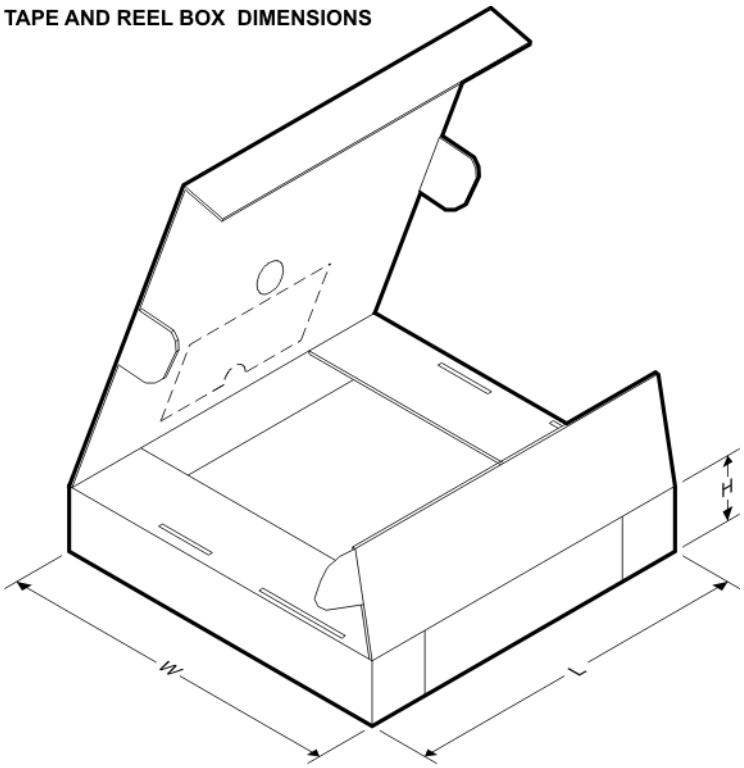
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2370IDBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2370IDBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2370IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2371IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2371IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2371IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2372IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2372IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2372IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2373IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2373IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2373IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2374IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2374IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2375IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLV2375IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

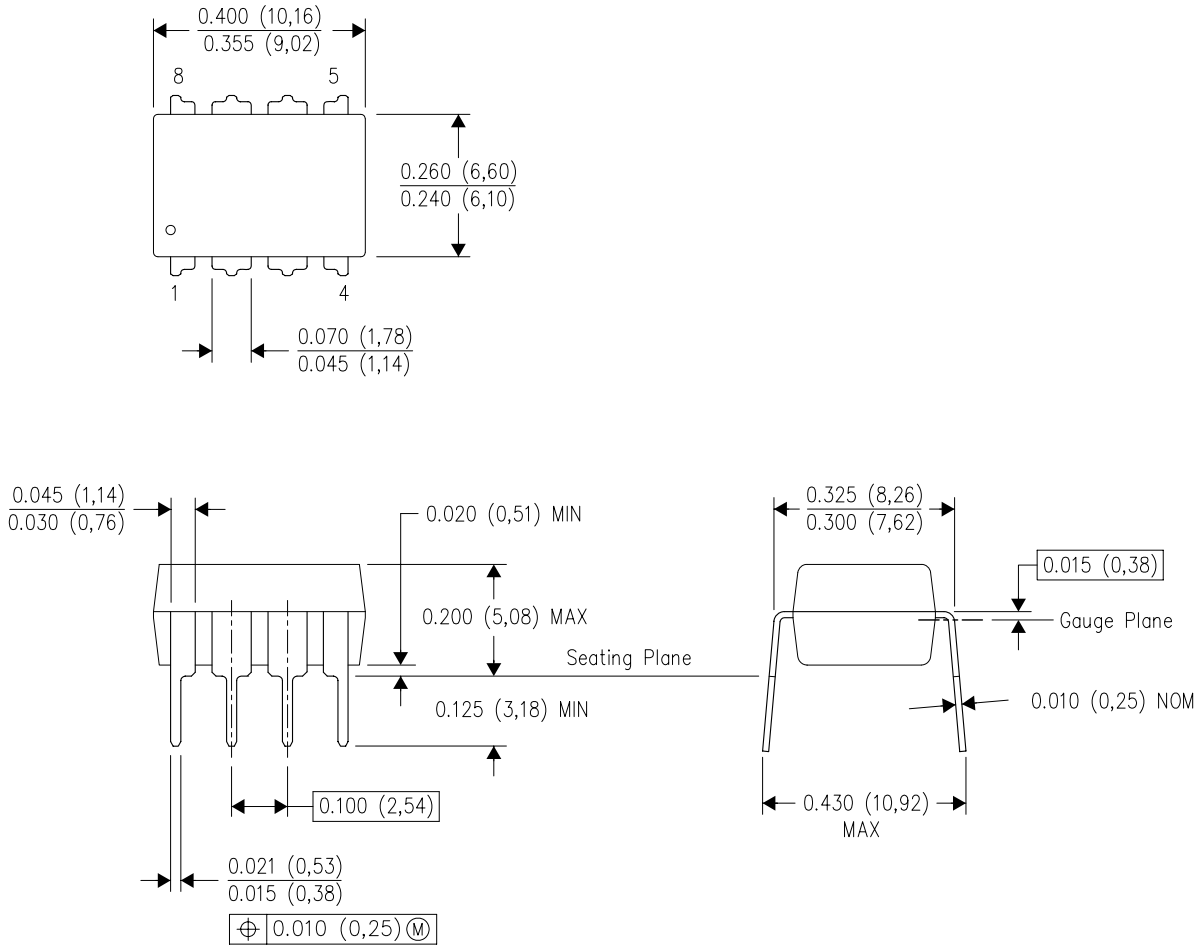
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

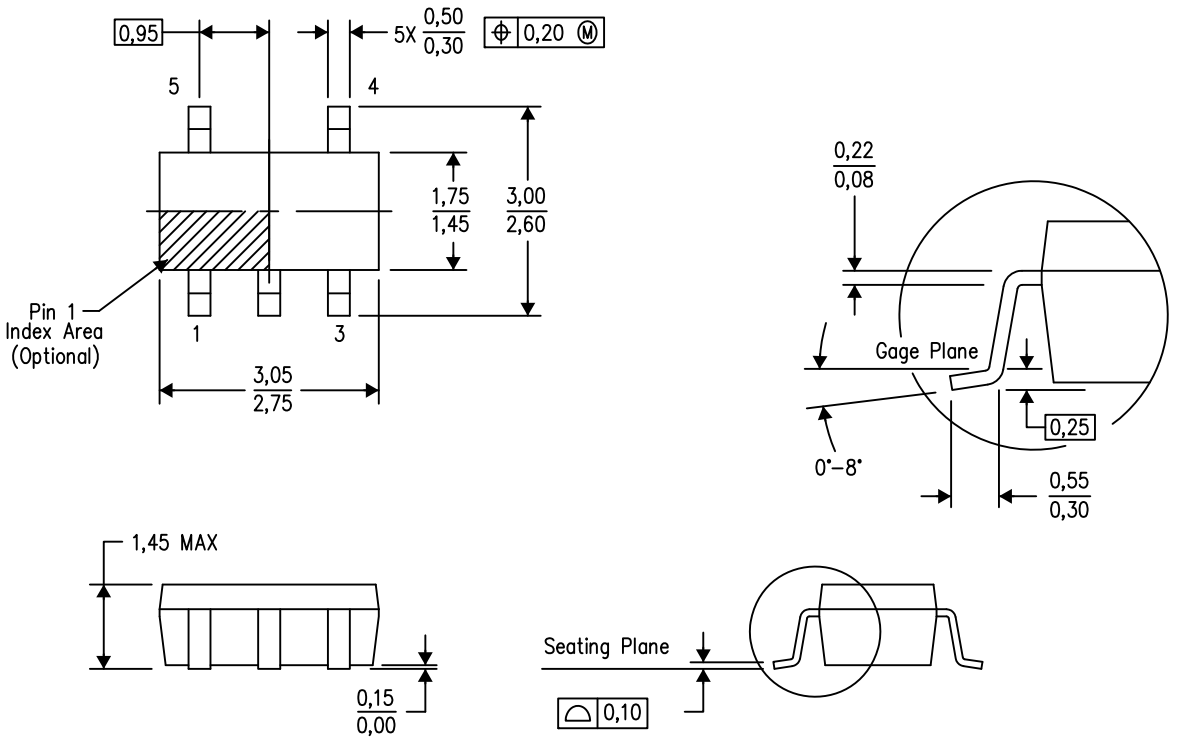
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2370IDBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TLV2370IDBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TLV2370IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2371IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV2371IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV2371IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2372IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2372IDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2372IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2373IDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TLV2373IDGSR	VSSOP	DGS	10	2500	364.0	364.0	27.0
TLV2373IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV2374IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV2374IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2375IDR	SOIC	D	16	2500	333.2	345.9	28.6
TLV2375IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

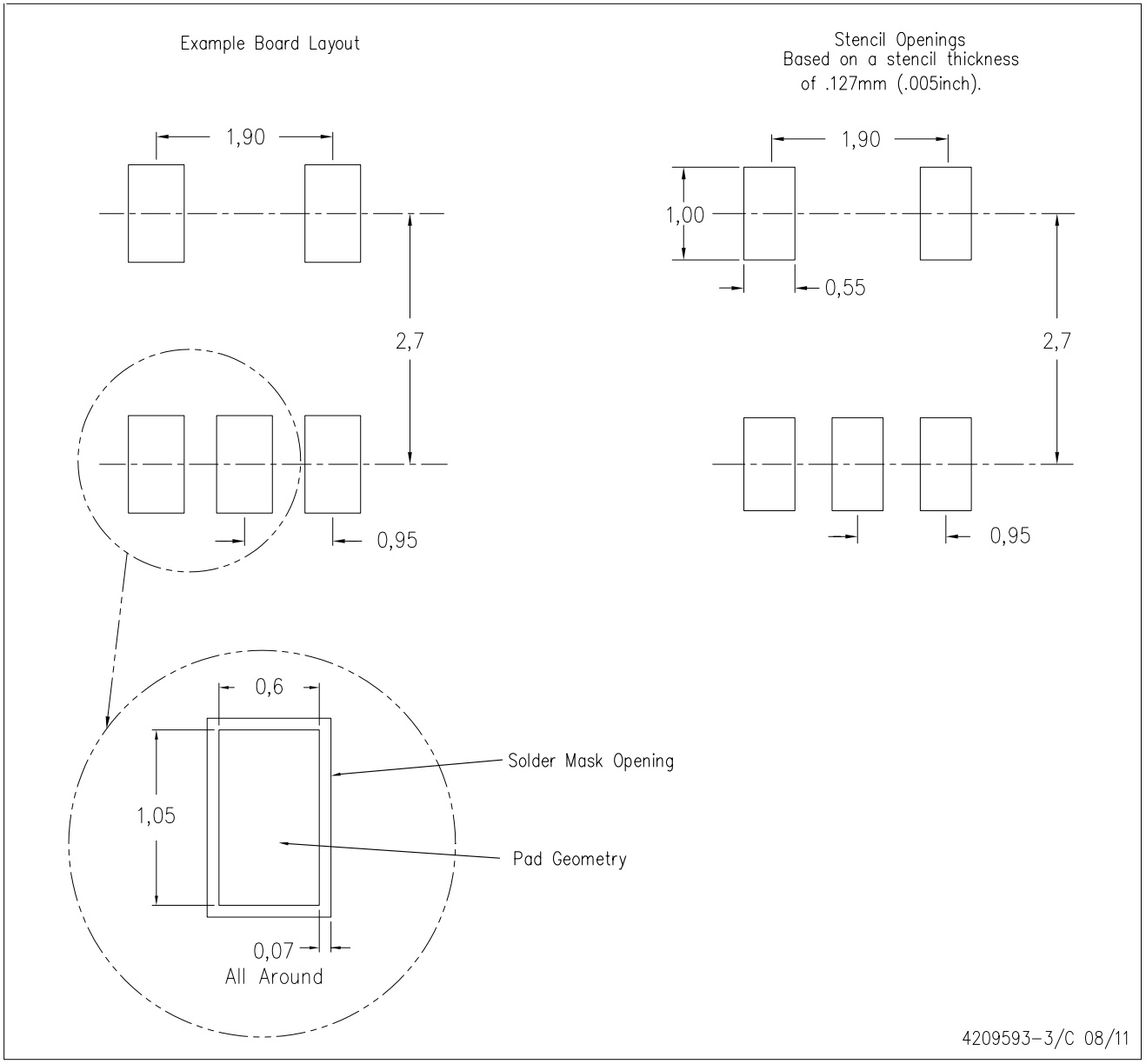
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

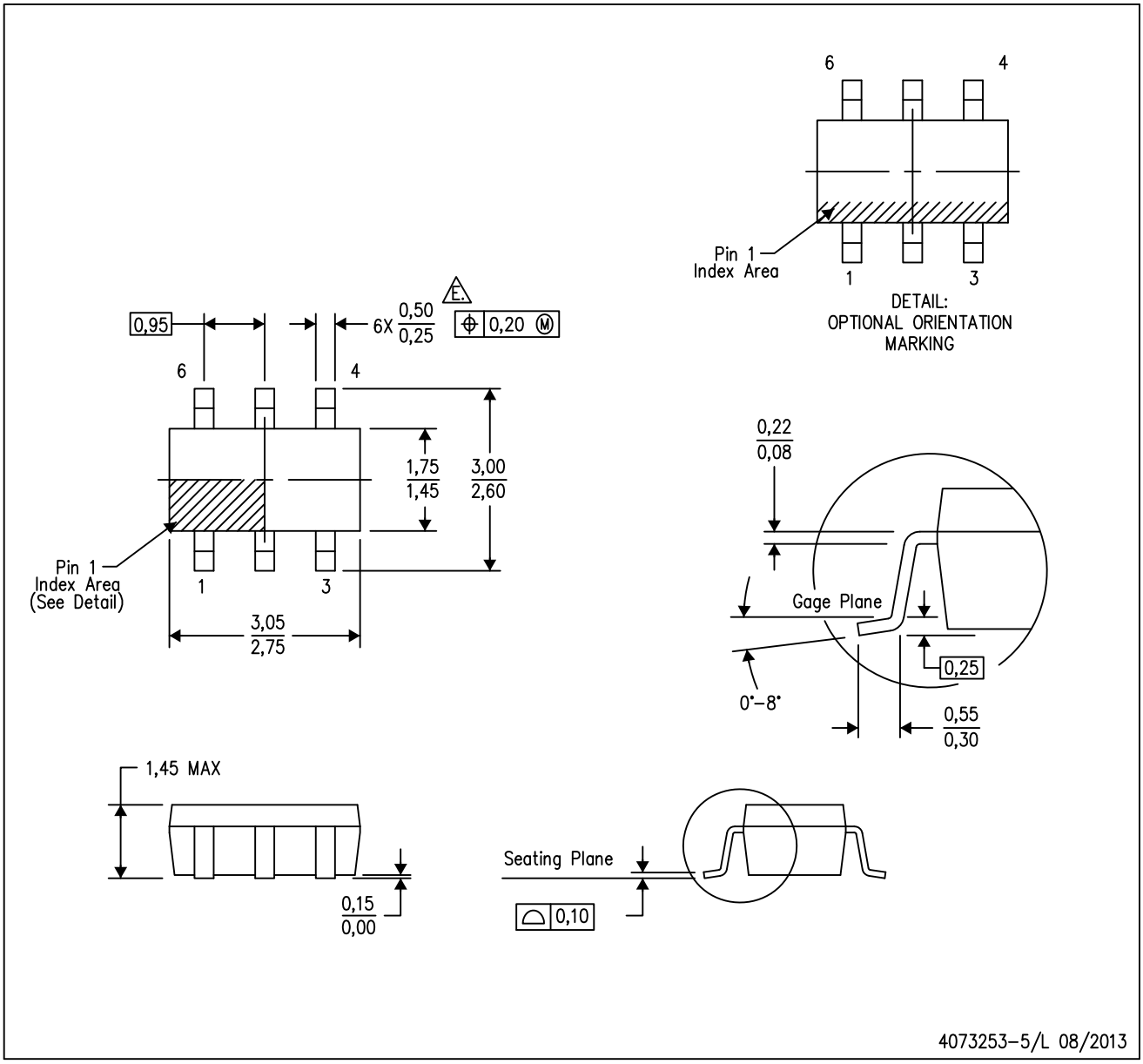
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



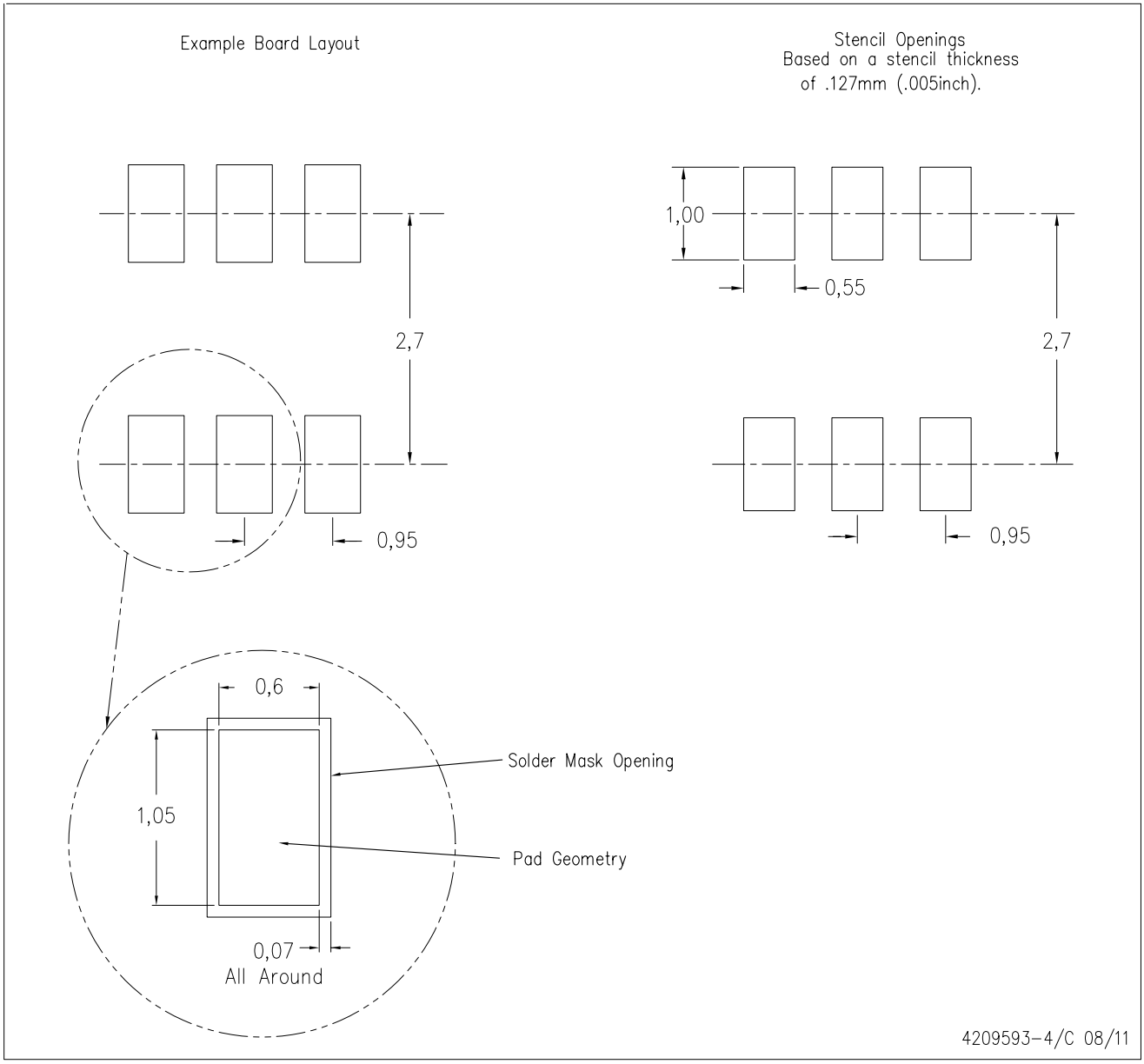
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



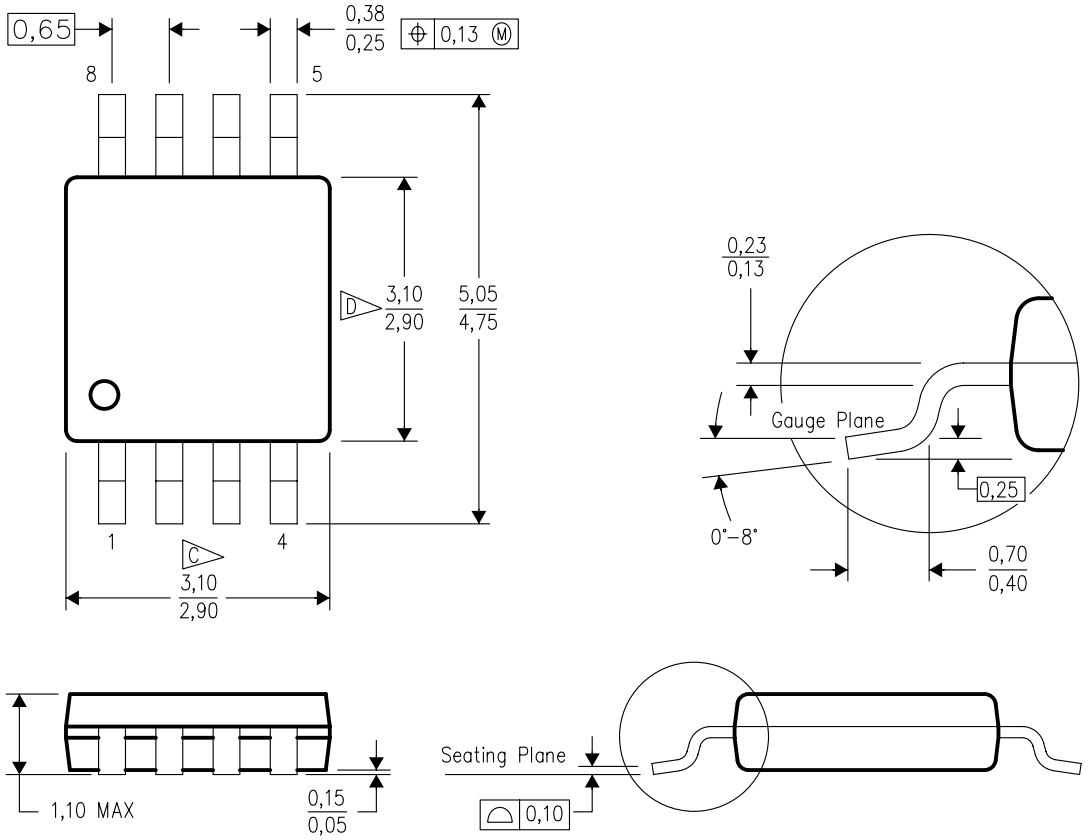
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

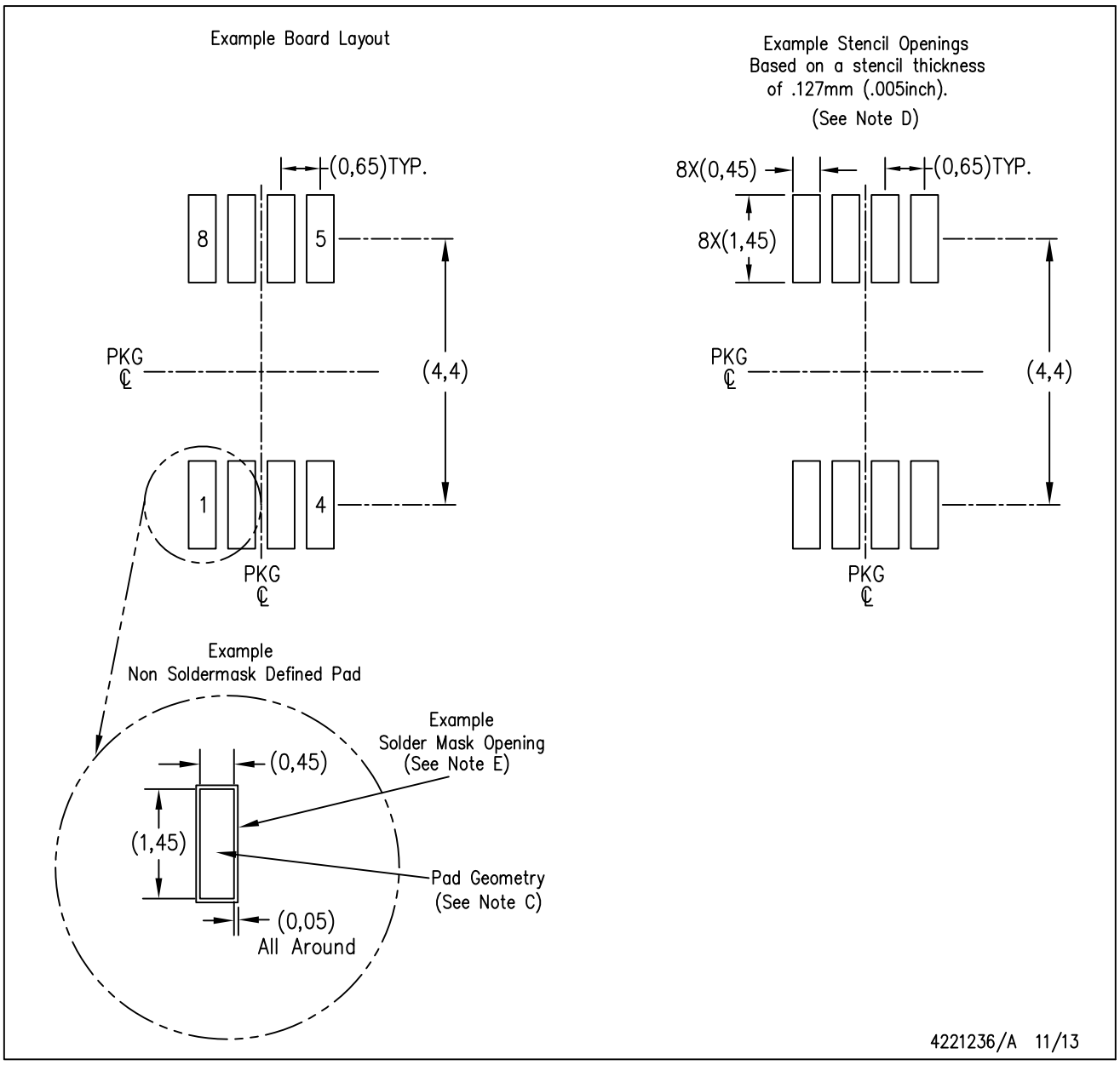
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

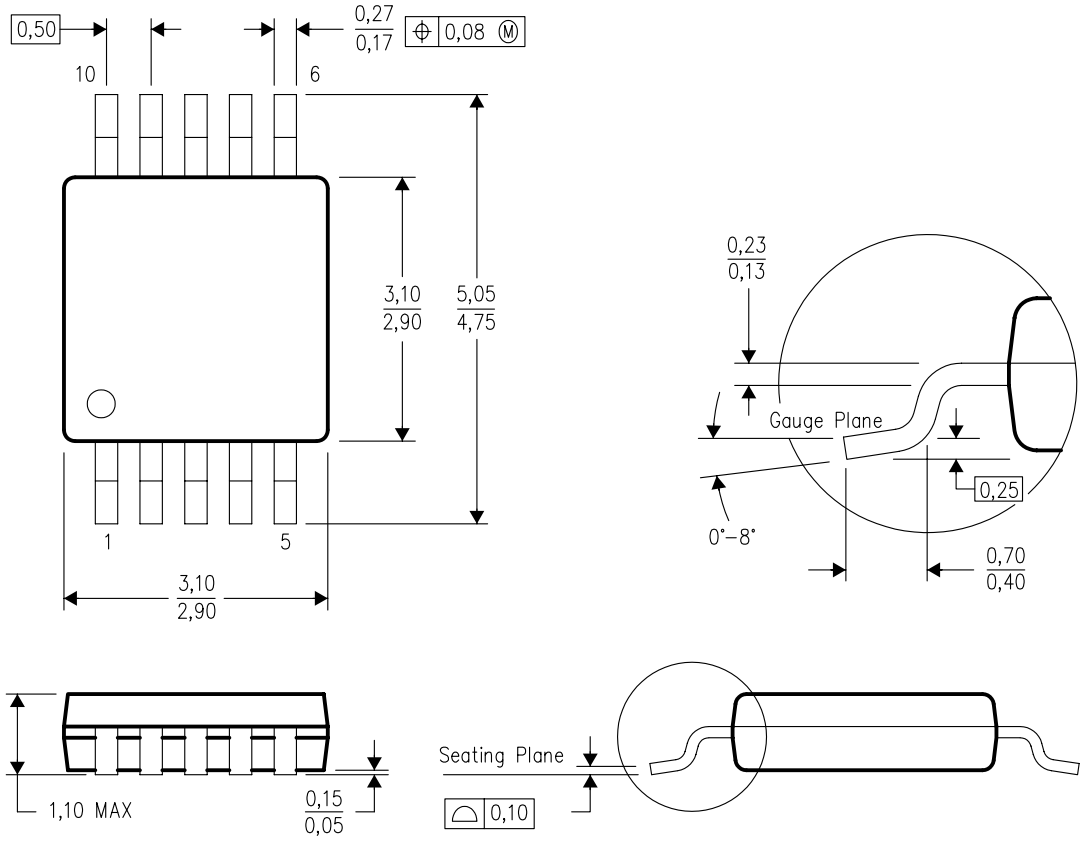
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

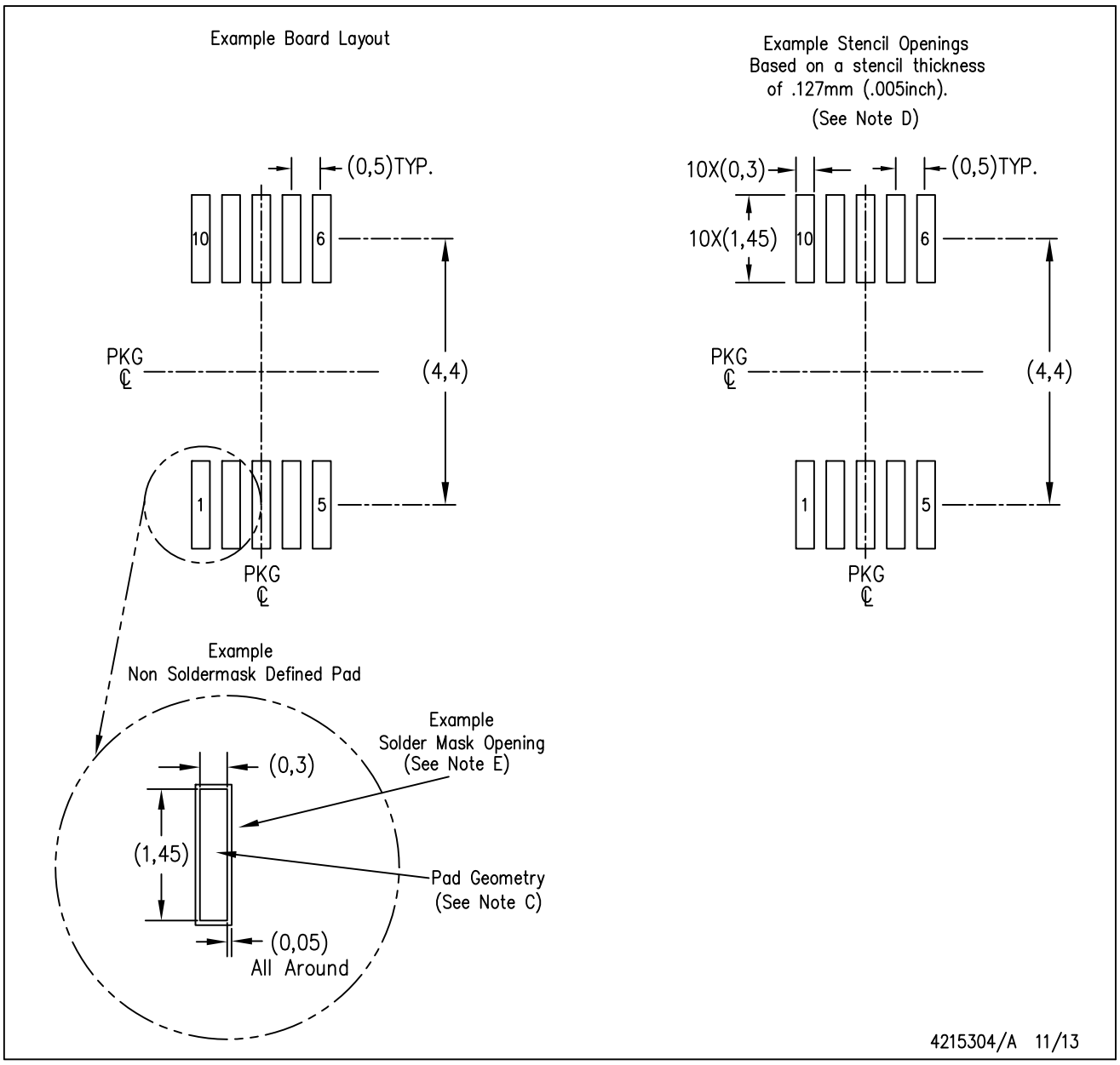
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

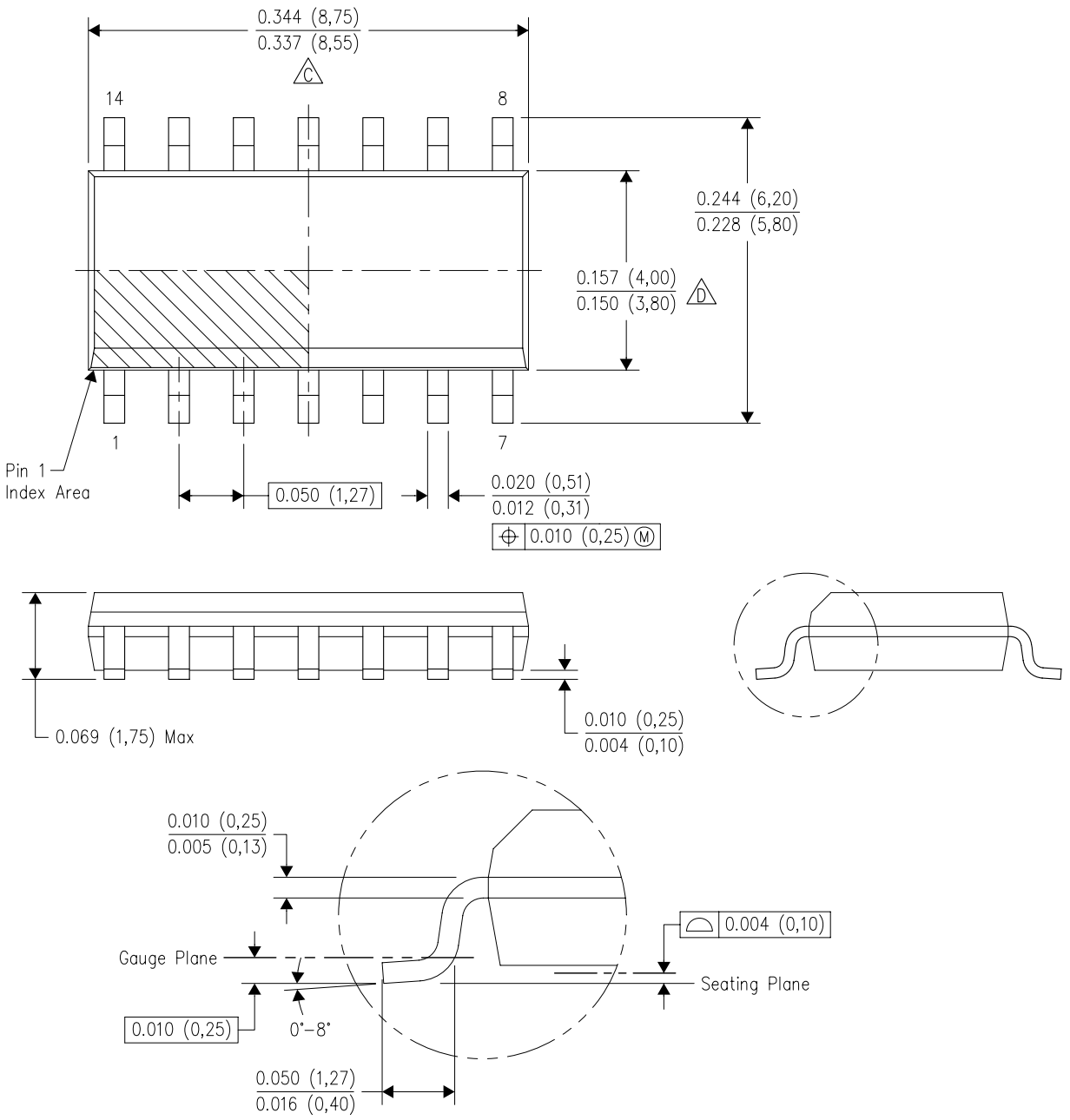
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

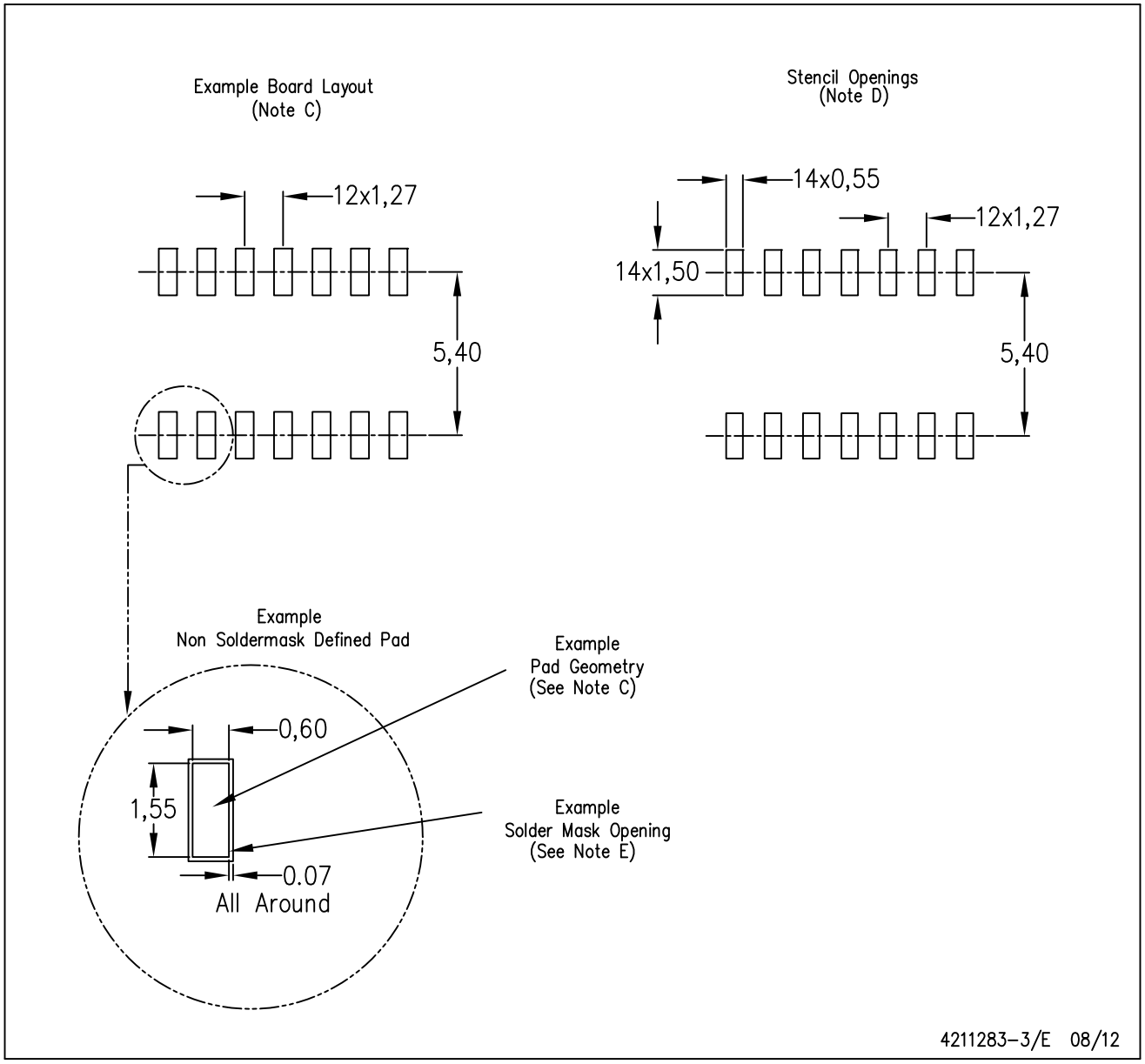
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

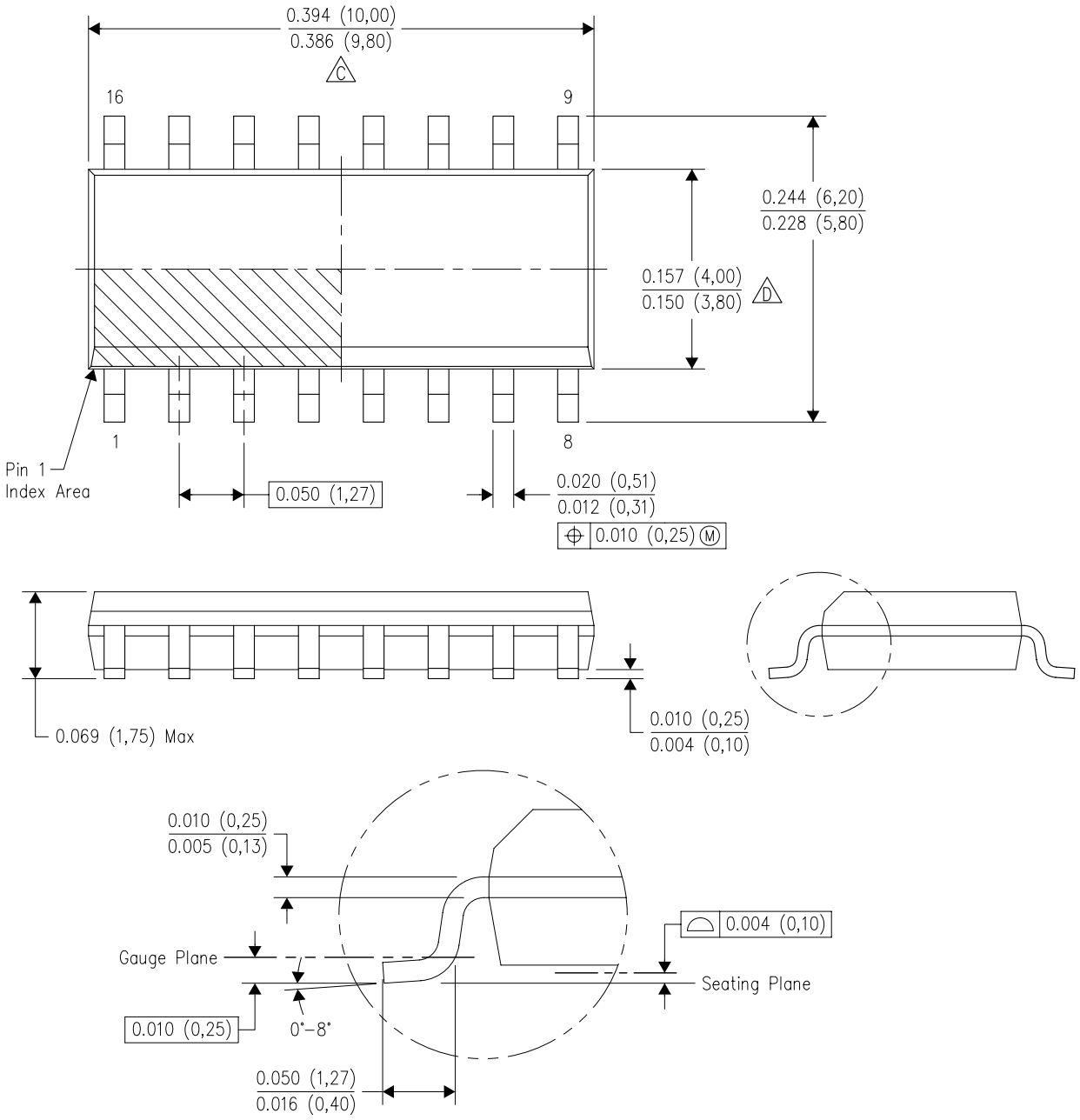
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



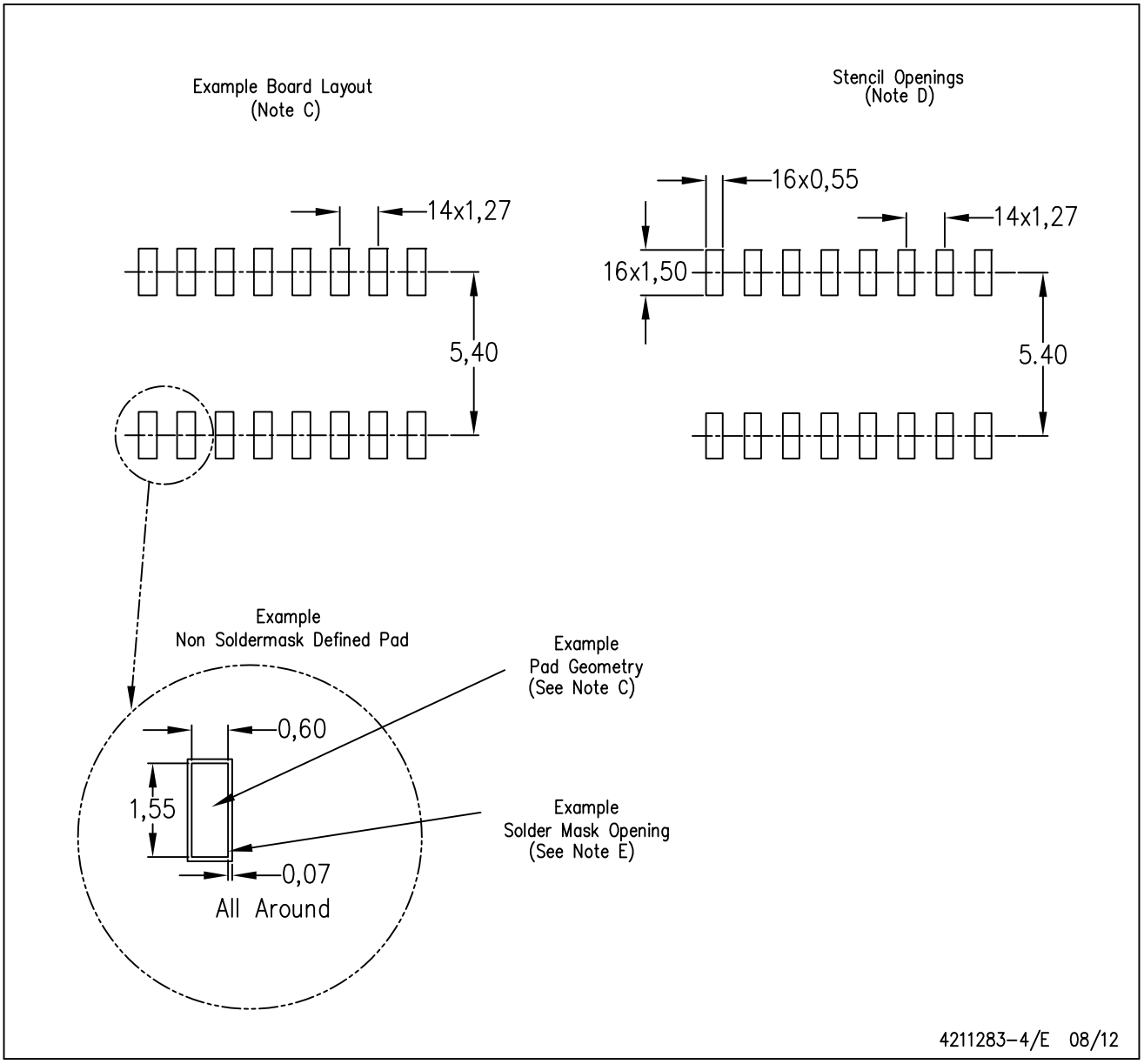
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



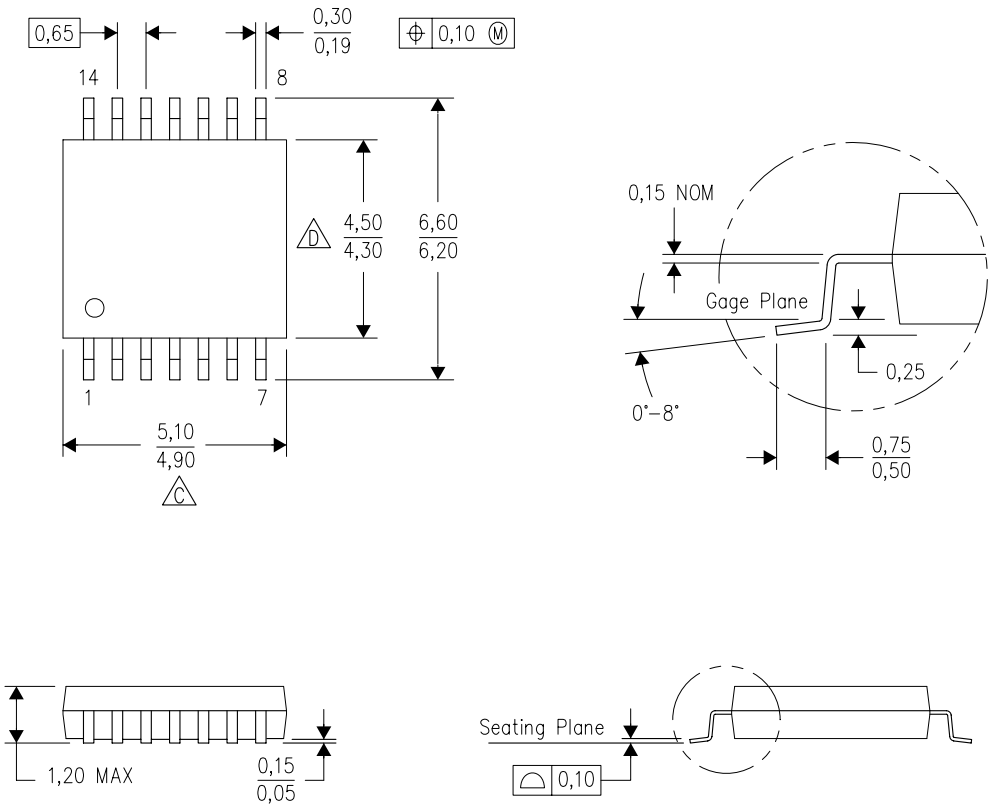
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

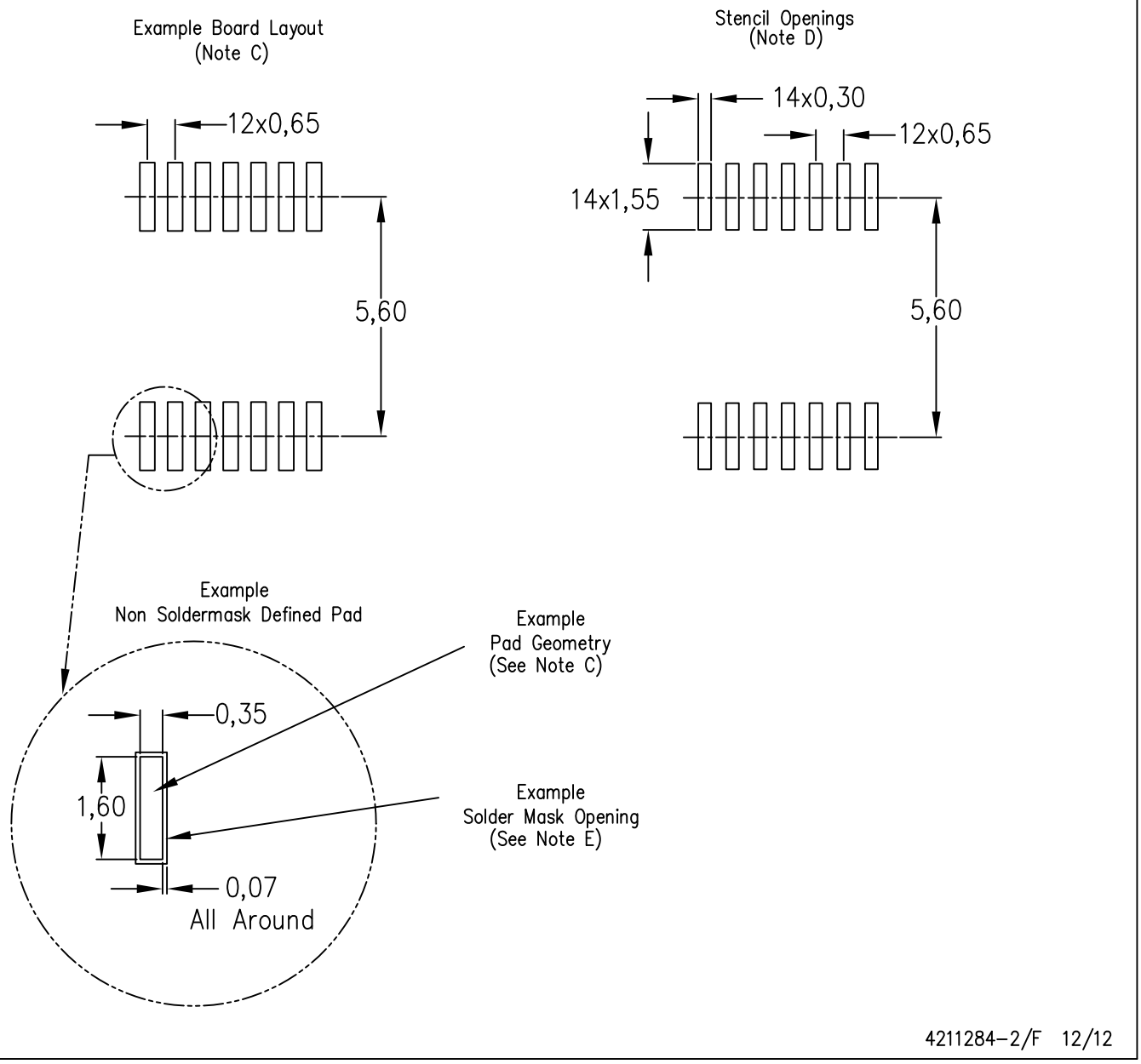
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

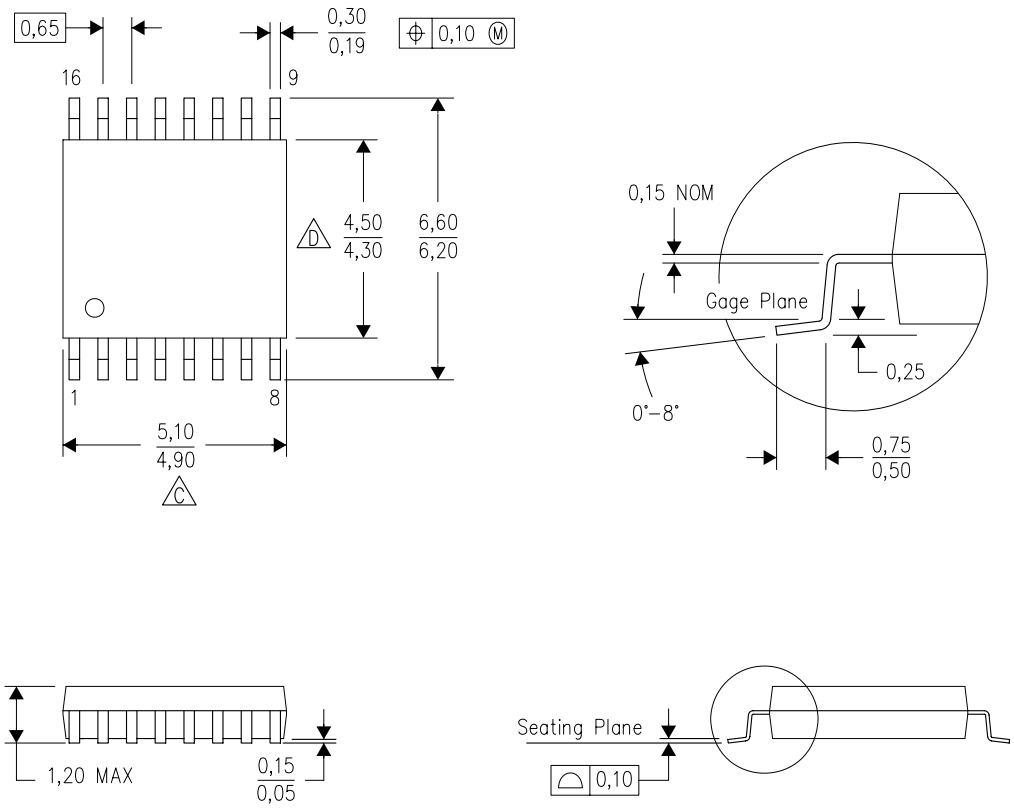
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

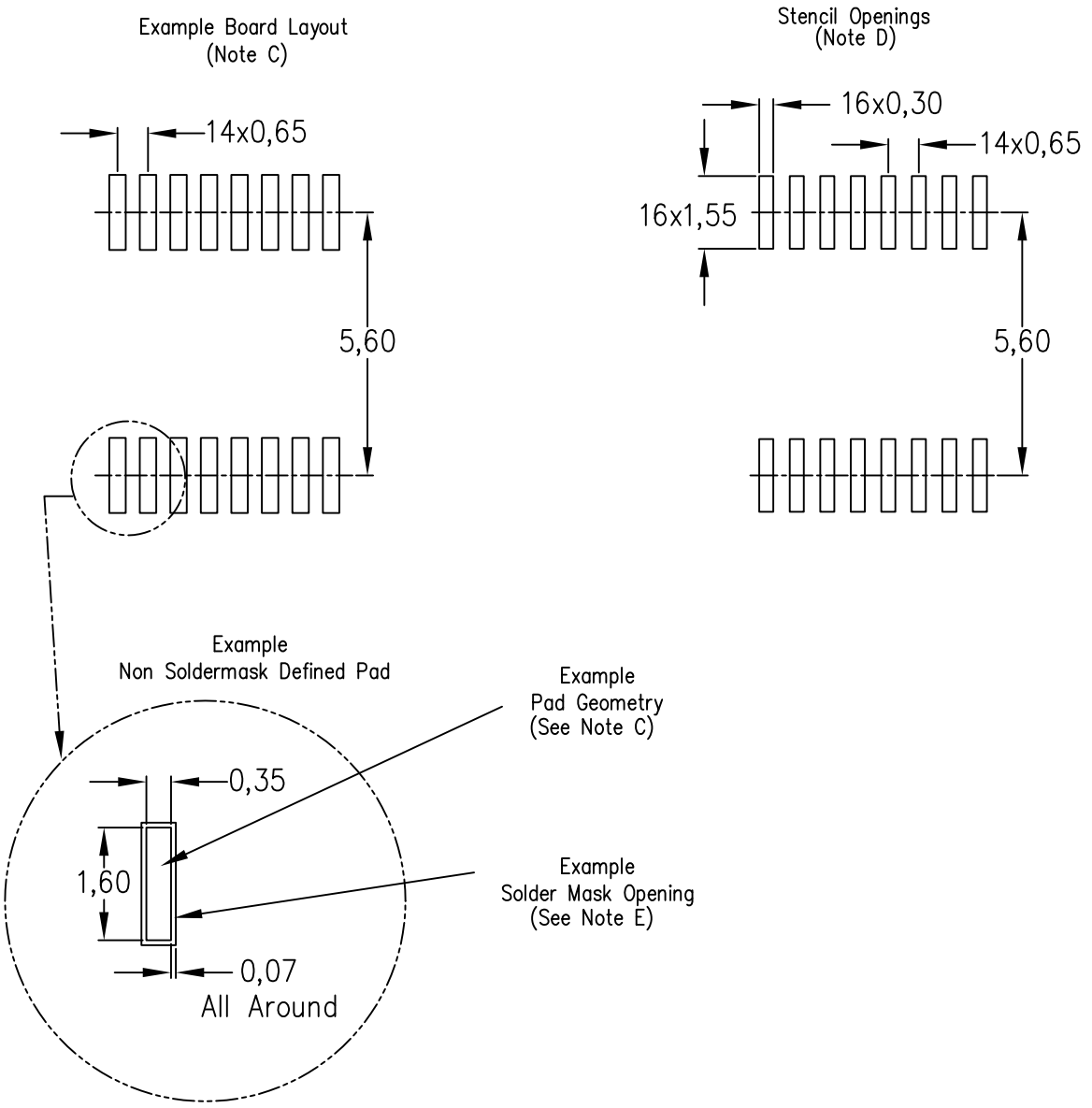
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

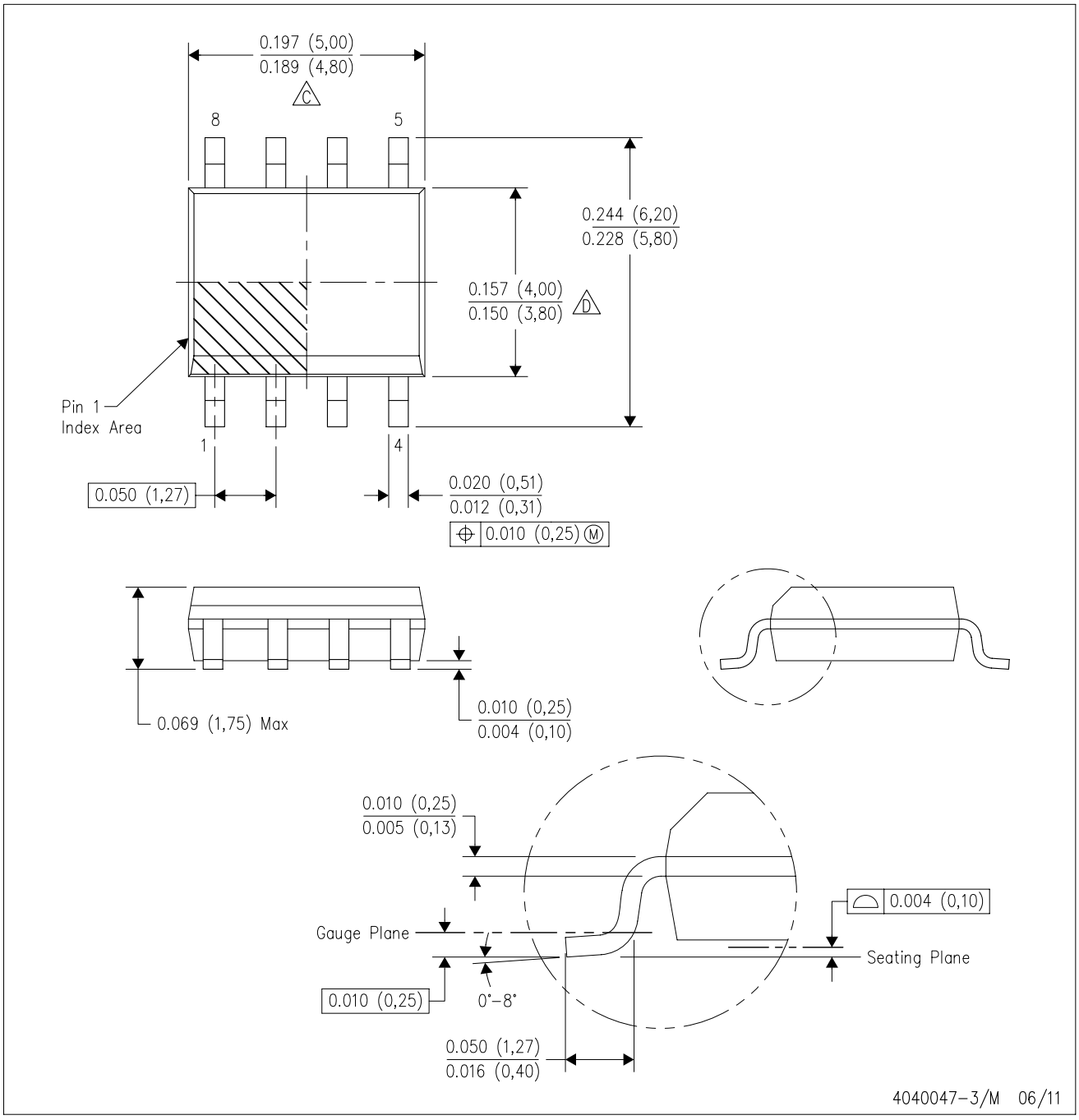
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



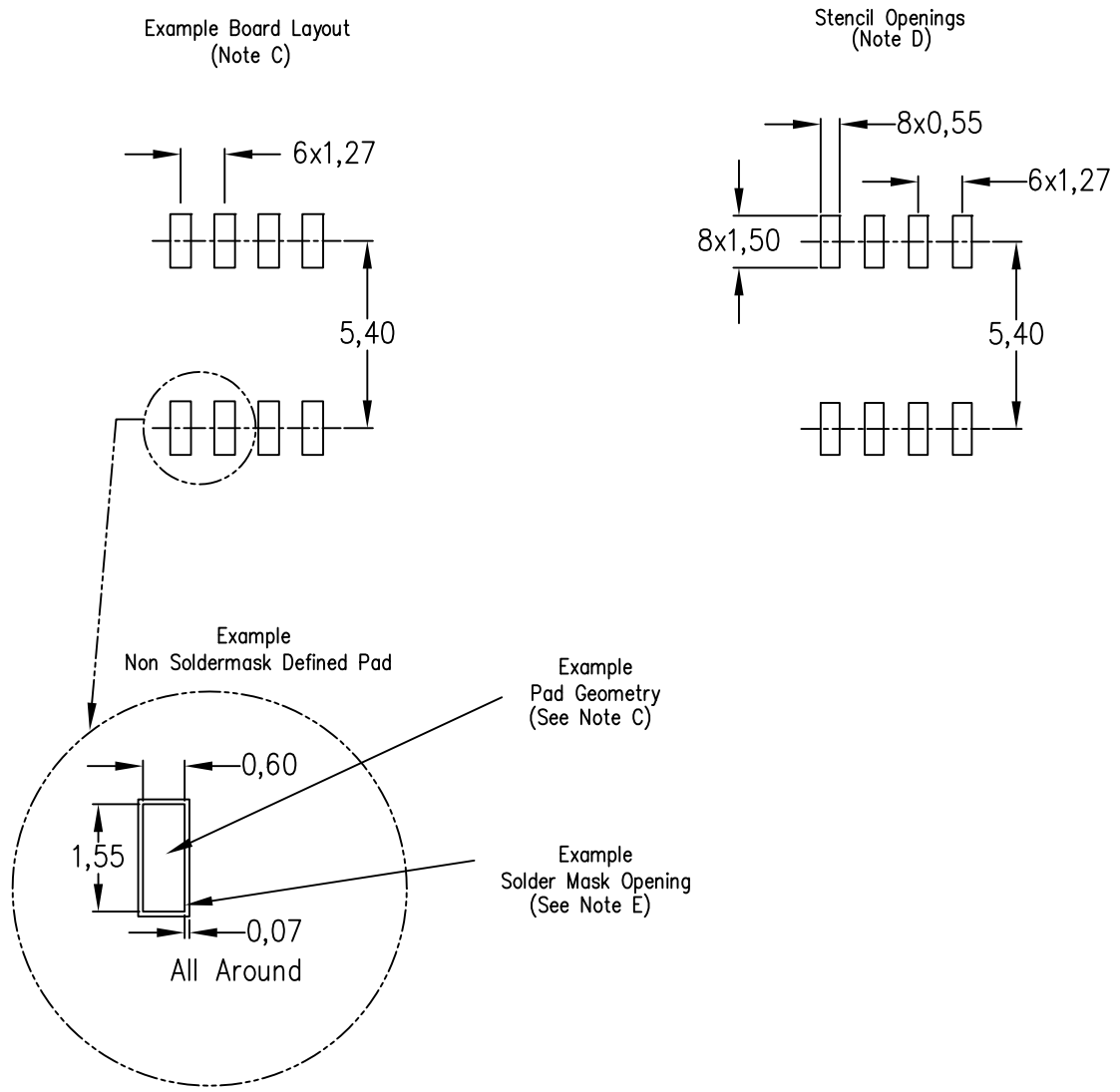
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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