19-2555; Rev 1; 12/02

EVALUATION KIT AVAILABLE

Digitally Controlled, 0.5% Accurate, Safest APD Bias Supply

General Description

The MAX1932 generates a low-noise, high-voltage output to bias avalanche photodiodes (APDs) in optical receivers. Very low output ripple and noise is achieved by a constant-frequency, pulse-width modulated (PWM) boost topology combined with a unique architecture that maintains regulation with an optional RC or LC post filter inside its feedback loop. A precision reference and error amplifier maintain 0.5% output voltage accuracy.

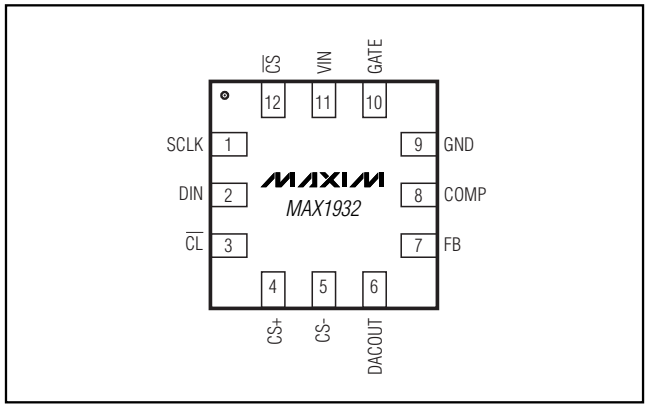
The MAX1932 protects expensive APDs against adverse operating conditions while providing optimal bias. Traditional boost converters measure switch current for protection, whereas the MAX1932 integrates accurate high-side current limiting to protect APDs under avalanche conditions. A current-limit flag allows easy calibration of the APD operating point by indicating the precise point of avalanche breakdown. The MAX1932 control scheme prevents output overshoot and undershoot to provide safe APD operation without data loss.

The output voltage can be accurately set with either external resistors, an internal 8-bit DAC, an external DAC, or other voltage source. Output span and offset are independently settable with external resistors. This optimizes the utilization of DAC resolution for applications that may require limited output voltage range, such as 4.5V to 15V, 4.5V to 45V, 20V to 60V, or 40V to 90V.

Applications

Optical Receivers and Modules
Fiber Optic Network Equipment
Telecom Equipment
Laser Range Finders
PIN Diode Bias Supply

Pin Configuration



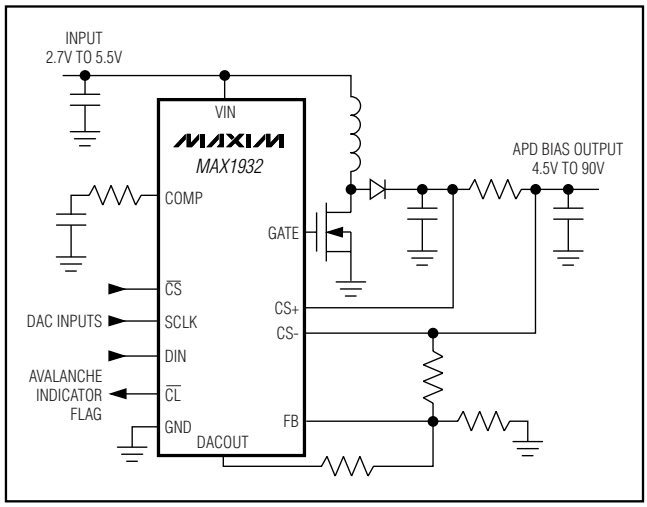
Features

- ♦ **Small Circuit Footprint**
- ♦ **Circuit Height < 2mm**
- ♦ **2.7V to 5.5V Input**
- ♦ **4.5V to 90V Output**
- ♦ **No Overshoot**
- ♦ **Accurate High-Side Current Limit**
- ♦ **Avalanche Indicator Flag**
- ♦ **8-Bit SPI-Compatible DAC**
- ♦ **Compatible with External DAC**
- ♦ **0.5% Accurate Output**
- ♦ **Low Ripple Output (< 1mV)**
- ♦ **Small 12-Pin, 4mm × 4mm Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1932ETC	-40°C to +85°C	12 Thin QFN

Typical Application Circuit



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ABSOLUTE MAXIMUM RATINGS

VIN to GND .....-0.3V to +6V
DIN, SCLK, $\overline{CS}$, FB to GND .....-0.3V to +6V
COMP, DACOUT, GATE, $\overline{CL}$ to GND .....-0.3V to (V_{IN} +0.3V)
CS+, CS- to GND .....-0.3V to +110V
Continuous Power Dissipation (T_A = +70°C)
12-Pin Thin QFN (derate 16.9mW/°C above +70°C) .1349mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, $\overline{CS}$ = SCLK = D_{IN} = 3.3V, CS+ = CS- = 45V, Circuit of Figure 2, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Input Supply Range	V_{IN}		2.7		5.5	V
V_{IN} Undervoltage Lockout	UVLO	Both rise/fall, hysteresis = 100mV	2.1		2.6	V
Operating Supply Current	I_{IN}			0.5	1	mA
V_{IN} Shutdown Supply Current	I_{SHDN}	00 hex loaded to DAC		25	65	µA
Input Resistance for CS+/CS-		Resistance from either pin to ground	0.5	1	2.0	MΩ
Current-Limit Threshold for CS+/CS-			1.80	2.00	2.20	V
Common-Mode Rejection of Current Threshold		CS+ = 3V to 100V		±0.005		%/V
Gate-Driver Resistance		Gate high or low, I_{GATE} = ±50mA		5	10	Ω
FB Input Bias Current			-25		+25	nA
FB Voltage	V_{FB}	T_A = +25°C	1.24375	1.2500	1.25625	V
		T_A = 0°C to +85°C	1.24250	1.2500	1.25750	
FB Voltage Temperature Coefficient	TCV_{FB}			0.0007		%/°C
FB to COMP Transconductance		COMP = 1.5V	50	110	200	µS
COMP Pulldown Resistance in Shutdown		DAC code = 00 hex			100	Ω
DACOUT to FB Voltage Difference		DAC code = FF hex	-3		+3	mV
DACOUT Differential Nonlinearity (Note 1)		DAC Code = 01 to FF hex, DAC guaranteed monotonic	-1		+1	LSB
DACOUT Voltage Temperature Coefficient	TCV_{DACOUT}			0.0007		%/°C
DACOUT Load Regulation		DAC code = 0F to FF hex, source or sink 50µA	-1		+1	mV
Switching Frequency	f_{OSC}		250	300	340	kHz
GATE Maximum On-Time	t_{ON}			3		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, $\overline{CS}$ = SCLK = D_{IN} = 3.3V, CS+ = CS- = 45V, Circuit of Figure 2, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$)						
Input Low Voltage					0.6	V
Input High Voltage			1.4			V
Input Hysteresis				200		mV
Input Leakage Current		T_A = +25°C	-1		+1	µA
		T_A = 0°C to +85°C		10		nA
Input Capacitance				5		pF
DIGITAL OUTPUT ($\overline{CL}$)						
Output Low Voltage		I_{SINK} = 1mA			0.1	V
Output High Voltage		I_{SOURCE} = 0.5mA	V_{IN} - 0.5			V
SPI TIMING (FIGURE 5)						
SCLK Clock Frequency	f_{SCLK}				2	MHz
SCLK Low Period	t_{CL}		125			ns
SCLK High Period	t_{CH}		125			ns
Data Hold Time	t_{DH}		0			ns
Data Setup Time	t_{DS}		125			ns
$\overline{CS}$ Assertion to SCLK Rising Edge Setup Time	t_{CSS0}		200			ns
$\overline{CS}$ Deassertion to SCLK Rising Edge Setup Time	t_{CSS1}		200			ns
SCLK Rising Edge to $\overline{CS}$ Deassertion	t_{CSH1}		200			ns
SCLK Rising Edge to $\overline{CS}$ Assertion	t_{CSH0}		200			ns
$\overline{CS}$ High Period	t_{CSW}		300			ns

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, $\overline{CS}$ = SCLK = D_{IN} = 3.3V, CS+ = CS- = 45V, Circuit of Figure 2, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Input Supply Range	V_{IN}		2.7		5.5	V
V_{IN} Undervoltage Lockout	UVLO	Both rise/fall, hysteresis = 100mV	2.1		2.6	V
Operating Supply Current	I_{IN}				1	mA
V_{IN} Shutdown Supply Current	I_{SHDN}	00 hex loaded to DAC			65	µA
Input Resistance for CS+/CS-		Resistance from either pin to ground	0.5		2	MΩ
Current-Limit Threshold for CS+/CS-			1.80		2.20	V
Gate-Driver Resistance		Gate high or low, I_{GATE} = ±50mA			10	Ω
FB Input Bias Current			-30		+30	nA

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, $\overline{CS}$ = SCLK = D_{IN} = 3.3V, CS+ = CS- = 45V, Circuit of Figure 2, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB Voltage	V_{FB}		1.23875		1.26125	V
FB to COMP Transconductance		COMP = 1.5V	50		200	µS
COMP Pulldown Resistance in Shutdown		DAC code = 00 hex			100	Ω
DACOUT to FB Voltage Difference		DAC code = FF hex	-4		+4	mV
DACOUT Differential Nonlinearity (Note 1)		DAC Code = 01 to FF hex, DAC guaranteed monotonic	-1		+1	LSB
DACOUT Load Regulation		DAC code = 0F to FF hex, source or sink 50µA	-1		+1	mV
Switching Frequency	f_{OSC}		240		360	kHz
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$)						
Input Low Voltage					0.6	V
Input High Voltage			1.4			V
DIGITAL OUTPUT ($\overline{CL}$)						
Output Low Voltage		I_{SINK} = 1mA			0.1	V
Output High Voltage		I_{SOURCE} = 0.5mA	V_{IN} - 0.5			V
SPI TIMING (FIGURE 5)						
SCLK Clock Frequency	f_{SCLK}				2	MHz
SCLK Low Period	t_{CL}		125			ns
SCLK High Period	t_{CH}		125			ns
Data Hold Time	t_{DH}		0			ns
Data Setup Time	t_{DS}		125			ns
$\overline{CS}$ Assertion to SCLK Rising Edge Setup Time	t_{CSS0}		200			ns
$\overline{CS}$ Deassertion to SCLK Rising Edge Setup Time	t_{CSS1}		200			ns
SCLK Rising Edge to $\overline{CS}$ Deassertion	t_{CSH1}		200			ns
SCLK Rising Edge to $\overline{CS}$ Assertion	t_{CSH0}		200			ns
$\overline{CS}$ High Period	t_{CSW}		300			ns

Note 1: DACOUT = DAC code x (1.25V/256) + 1.25V/256.
Note 2: Specifications to -40°C are guaranteed by design and not production tested.

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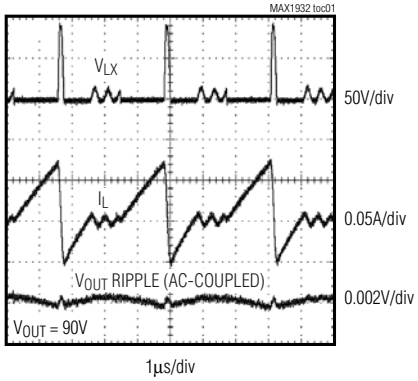
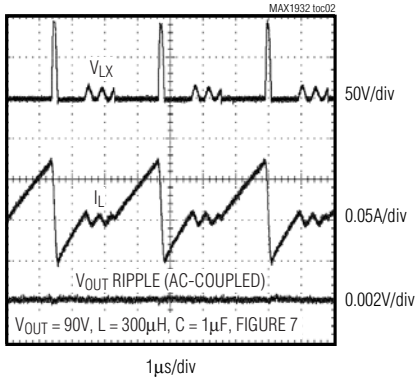
Typical Operating Characteristics

(V_{IN} = 5V, Circuit of Figure 2, T_A =+25°C, unless otherwise noted)

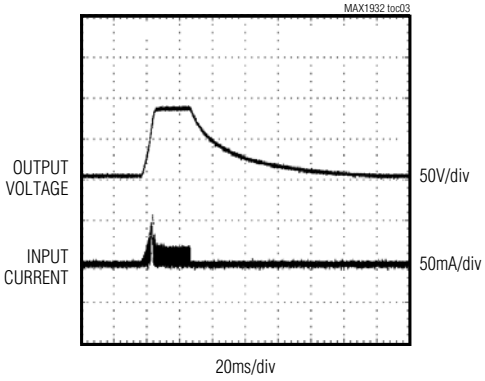
SWITCHING WAVEFORMS



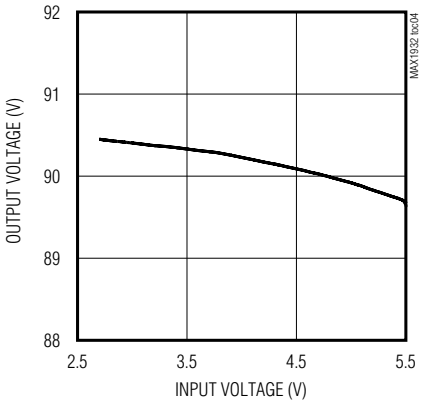
SWITCHING WAVEFORM WITH LC FILTER



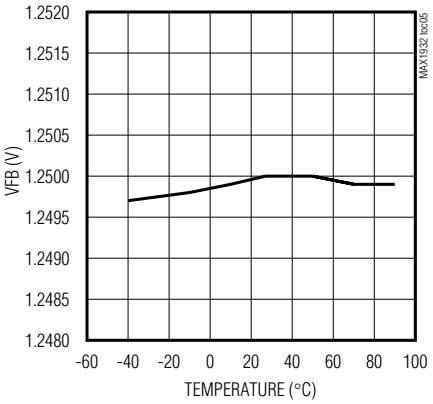
STARTUP AND SHUTDOWN WAVEFORMS



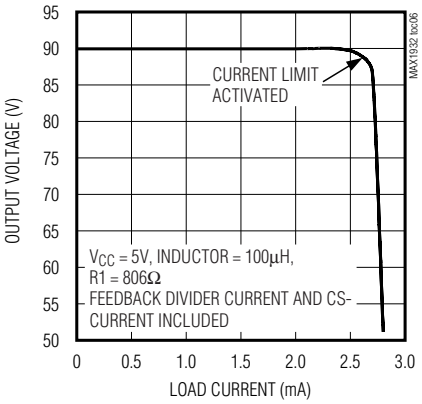
OUTPUT VOLTAGE vs. INPUT VOLTAGE



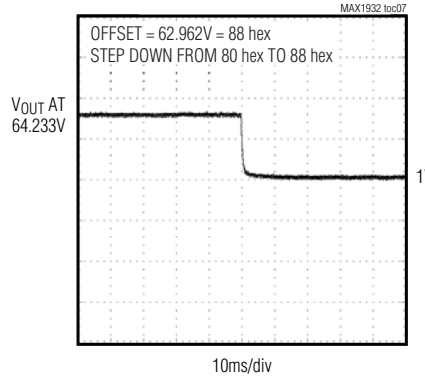
VFB vs. TEMPERATURE



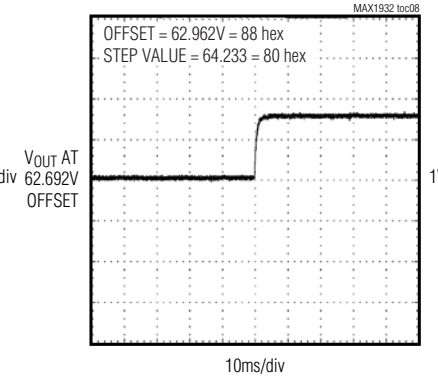
OUTPUT VOLTAGE vs. LOAD CURRENT



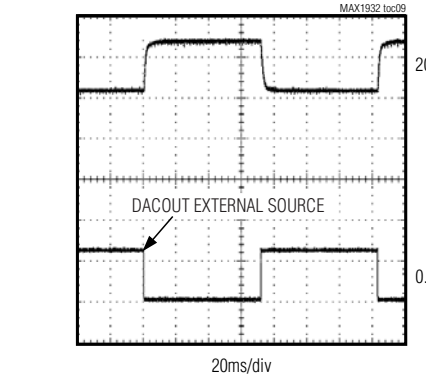
OUTPUT VOLTAGE STEP-DOWN DUE TO DAC CHANGE



OUTPUT VOLTAGE STEP-UP DUE TO DAC CHANGE



OUTPUT VOLTAGE STEP DUE TO DACOUT CHANGE



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Pin Description

PIN	NAME	FUNCTION
1	SCLK	DAC Serial Clock Input
2	DIN	DAC Serial Data Input
3	$\overline{CL}$	Current-Limit Indicator Flag. $\overline{CL}$ = 0 indicates that the part is in current limit. Logic high level = VIN.
4	CS+	Current-Limit Plus Sense Input. Connect a resistor from CS+ to CS- in series with the output. The differential threshold is 2V. CS+ has typically 1MΩ resistance to ground.
5	CS-	Current-Limit Minus Sense Input. CS- has typically 1MΩ resistance to ground.
6	DACOUT	Internal DAC Output. Generates a control voltage for adjustable output operation. DACOUT can source or sink 50µA.
7	FB	Feedback input. Connect to a resistive voltage-divider between the output voltage (V_{OUT}) and FB to set the output voltage. The feedback set point is 1.25V.
8	COMP	Compensation Pin. Compensates the DC-DC converter control loop with a series RC to GND. COMP is actively discharged to ground during shutdown or undervoltage conditions.
9	GND	Ground
10	GATE	Gate-Driver Output for External N-FET
11	VIN	IC Supply Voltage (2.7V to 5.5V). Bypass VIN with a 1µF or greater ceramic capacitor.
12	$\overline{CS}$	DAC Chip-Select Input

Detailed Description

Fixed Frequency PWM

The MAX1932 uses a constant frequency, PWM, controller architecture. This controller sets the switch on-time and drives an external N-channel MOSFET (see Figure 1). As the load varies, the error amplifier sets the inductor peak current necessary to supply the load and regulate the output voltage.

Output Current Limit

The MAX1932 uses an external resistor at CS+ and CS- to sense the output current (see Figure 2). The typical current-limit threshold is 2V. $\overline{CL}$ is designed to help find the optimum APD bias point by going low to indicate when the APD reaches avalanche and that current limit has been activated. To minimize noise, $\overline{CL}$ only changes state on an internal oscillator edge.

Output Control DAC

An internal digital-to-analog converter can be used to control the output voltage of the DC-DC converter (Figure 2). The DAC output is changed through an SPI™ serial interface using an 8-bit control byte. On power-up, the DAC defaults to FF hex (1.25V), which corresponds to a minimum boost converter output voltage.

Alternately, the output voltage can be set with external resistors, an external DAC, or a voltage source. Output span and offset are independently settable with external resistors. See the *Applications Information* section for output control equations.

SPI Interface/Shutdown

Use an SPI-compatible 3-wire serial interface with the MAX1932 to control the DAC output voltage and to shut down the MAX1932. Figures 4 and 5 show timing diagrams for the SPI protocol. The MAX1932 is a write-only device and uses $\overline{CS}$ along with SCLK and DIN to communicate. The serial port is always operational when the device is powered. To shut down the DC-DC converter portion only, update the DAC registers to 00 hex.

Applications Information

Voltage Feedback Sense Point

Feedback can be taken from in front of, or after, the current-limit sense resistor. The current-limit sense resistor forms a lowpass filter with the output capacitor. Taking feedback after the current-limit sense resistor (see Figure 2), optimizes the output voltage accuracy, but requires overcompensation, which slows down the control loop response. For faster response, the feedback can be taken from in front of the current-sense resistor (see Figure 3). This configuration however, makes the output voltage more sensitive to load variation and degrades output accuracy by an amount equal to the load current times the current-sense resistor value.

SPI is a trademark of Motorola, Inc.

Output and DAC Adjustments Range

Many biasing applications require an adjustable output voltage, which is easily obtained using the MAX1932's DAC output (Figure 2).

The DAC output voltage is given by the following equation:

$$V_{DACOUT} = CODE \times \left(\frac{1.25V}{256}\right) + \left(\frac{1.25V}{256}\right)$$

On power-up, DACOUT defaults to FF hex or 1.25V, which corresponds to the minimum V_{OUT} output voltage.

The voltage generated at DACOUT is coupled to FB through R6. DACOUT can sink only 50µA so:

$$R6 \geq \frac{1.25V}{50\mu A}$$

Select the minimum output voltage (V_{OUTFF}), and the maximum output voltage (V_{OUT01}) for the desired adjustment range. R5 sets the adjustment span using the following equation:

$$R5 = (V_{OUTFF} - V_{OUT01})\ (R6/1.25V)$$

R8 sets the minimum output of the adjustment range with the following equation:

$$R8 = (1.25V \times R5)/(V_{OUTFF})$$

Setting the Output Voltage without the DAC

Adjust the output voltage by connecting a voltage-divider from the output (V_{OUT}) to FB (Figure 2 with R6 omitted). Select R8 between 10kΩ to 50kΩ. Calculate R5 with the following equation:

$$R5 = R8\left(\frac{VOUT}{1.25V} - 1\right)$$

Inductor Selection

Optimum inductor selection depends on input voltage, output voltage, maximum output current, switching frequency, and inductor size. Inductors are typically specified by their inductance (L), peak current (I_{PK}), and resistance (L_R).

The inductance value is given by:

$$L = \frac{(V_{IN})^2 \times D^2 \times T \times \eta}{2I_{OUT(MAX)} \times V_{OUT}}$$

where V_{IN} is the input voltage, $I_{OUT(MAX)}$ is the maximum output current delivered, V_{OUT} is the output voltage, and T is the switching period (3.3µs), η is the estimated power conversion efficiency, and D is the maximum duty cycle:

$$D < (V_{OUT} - V_{IN})/V_{OUT} \text{ up to a maximum of } 0.9$$

Since the L equation factors in efficiency, for inductor calculation purposes, an η of 0.5 to 0.75 is usually suitable.

For example, with a maximum DC load current of 2.5mA, a 90V output, V_{IN} = 5V, D = 0.9, T = 3.3µs, and η estimated at 0.75, the above equation yields an L of 111µH, so 100µH would be a suitable value.

The peak inductor current is given by:

$$I_{PK} = \frac{V_{IN} \times D \times T}{L}$$

These are typical calculations. For worst case, refer to the article titled "Choosing the MAX1932 External Indicator, Diode, Current Sense Resistor, and Output Filter Capacitor for Worst Case Conditions" located on the Maxim website in the Application Notes section (visit www.maxim-ic.com/an1805).

External Power-Transistor Selection

An N-FET power switch is required for the MAX1932. The N-FET switch should be selected to have adequate on-resistance with the MOSFET $V_{GS} = V_{IN(MIN)}$. The breakdown voltage of the N-FET must be greater than V_{OUT}.

For higher-current output applications (such as 5mA at 90V), SOT23 high-voltage low-gate-threshold N-FETs may not have adequate current capability. For example, with a 5V input, a 90V, 5mA output requires an inductor peak of 240mA. For such cases it may be necessary to simply parallel two N-FETs to achieve the required current rating. With SOT23 devices this often results in smaller and lower cost than using a larger N-FET device.

Diode Selection

The output diode should be rated to handle the output voltage and the peak switch current. Make sure that the diode's peak current rating is at least I_{PK} and that its breakdown voltage exceeds V_{OUT}. Fast reverse recovery time (t_{rr} < 10ns) and low junction capacitance

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(<10pF) are recommended to minimize losses. A small-signal silicon switching diode is suitable if efficiency is not critical.

Output Filter Capacitor Selection

The output capacitors of the MAX1932 must have high enough voltage rating to operate with the V_{OUT} required. Output capacitor effective series resistance (ESR) determines the amplitude of the high-frequency ripple seen on the output voltage. In the typical application circuit, a second RC formed by R1 and C3 further reduces ripple.

Input Bypass Capacitor Selection

The input bypass capacitor reduces the peak currents drawn from the voltage source and reduces noise caused by the MAX1932's switching action. The input source impedance determines the size of the capacitor required at the input (VIN). A low ESR capacitor is recommended. A 1µF ceramic capacitor is adequate for most applications. Place the bypass capacitor as close as possible to the VIN and GND pins.

Current-Sense Resistor Selection

Current limit is used to set the maximum delivered output current. In the typical application circuit, MAX1932 is designed to current limit at:

$$R1 = \frac{2V}{I_{LIMIT}}$$

Note that I_{LIMIT} must include current drawn by the feedback divider (if sensing feedback after R1) and the input current of CS-.

Stability and Compensation Component Selection

Compensation components, R7 and C4, introduce a pole and a zero necessary to stabilize the MAX1932 (see Figure 6). The dominant pole, POLE1, is formed by the output impedance of the error amplifier (R_{EA}) and C4. The R7/C4 zero, ZERO1, is selected to cancel the pole formed by the output filter cap C3 and output load R_{LD}, POLE2. The additional pole of R1/C3, POLE3, should be at least a decade past the crossover frequency to not affect stability:

POLE1 (dominant pole) = $1 / (2\pi \times R_{EA} \times C4)$

ZERO1 (integrator zero) = $1 / (2\pi \times R7 \times C4)$

POLE2 (output load pole) = $K1 / (2\pi \times R_{LD} \times (C2 + C3))$

POLE3 (output filter pole) = $1 / (2\pi \times R1 \times C3)$

The DC open-loop gain is given by:

$$A_{OL} = K2 \times Gm \times R_{EA}$$

where R_{EA} = 310MΩ,

g_M = 110µS,

R_{LD} is the parallel combination of feedback network and the load resistance.

$$K1 = \frac{2 \times V_{OUT} - V_{IN}}{V_{OUT} - V_{IN}}$$

$$K2 = \frac{V_{FB}\ (Volts)}{0.75\ (Volts)} \times \frac{2 \times V_{IN}}{2 \times V_{OUT} - V_{IN}} \times \left(\sqrt{\left(\frac{V_{OUT}}{V_{OUT} - V_{IN}} \right) \frac{R_{LD} \times T(second)}{2 \times L\ (Henries)}} \right)$$

A properly compensated MAX1932 results in a gain vs. frequency plot that crosses 0dB with a single pole slope (20dB per decade). See Figure 6.

Table 1 lists suggested component values for several typical applications.

Further Noise Reduction

The current-limit sense resistor is typically used as part of an output lowpass filter to reduce noise and ripple. For further reduction of noise, an LC filter can be added as shown in Figure 7. Output ripple and noise with and without the LC filter are shown in the *Typical Operating Characteristics*. If a post LC filter is used, it is best to use a coil with fairly large resistance (or a series resistor) so that ringing at the response peak of the LC filter is damped. For a 330µH and 1µF filter, 22Ω accomplishes this, but a resistor is not needed if the coil resistance is greater than 15Ω.

Output Accuracy and Feedback Resistor Selection

The MAX1932 features 0.5% feedback accuracy. The total voltage accuracy of a complete APD bias circuit is the sum of the FB set-point accuracy, plus resistor ratio error and temperature coefficient. If absolute accuracy is critical, the best resistor choice is an integrated network with specified ratio tolerance and temperature coefficient. If using discrete resistors in high-accuracy applications, pay close attention to resistor tolerance and temperature coefficients.

Temperature Compensation

APDs exhibit a change in gain as a function of temperature. This gain change can be compensated with an appropriate adjustment in bias voltage. For this reason it may be desirable to vary the MAX1932 output voltage as a function of temperature. This can be done in soft-

Table 1. Compensation Components for Typical Circuits (Figure 2)

V_{IN}, V_{OUT}, $I_{OUT(MAX)}$	INDUCTOR L1 (µH)	C_{SNS} C2 (µF)	R_{SNS} R1 (Ω)	C_{OUT} C3 (µF)	R_{COMP} R7 (kΩ)	C_{COMP} C4 (µF)
$5V_{IN}$, 40-90V_{OUT} at 2.5mA	100	0.047	806	0.1	20	0.22
$5V_{IN}$, 20-60V_{OUT} at 2.5mA	150	0.10	806	0.047	15	0.22
$5V_{IN}$, 20-60V_{OUT} at 5mA	82	0.22	392	0.10	10	0.47
$3V_{IN}$, 40-90V_{OUT} at 2.5mA	33	0.047	806	0.1	20	0.22
$3V_{IN}$, 4.5-15V_{OUT} at 2.5mA	220	0.47	806	0.01	7.5	0.47

ware by the system through the on-chip DAC, but can also be accomplished in hardware using an external thermistor or IC temperature sensor. Figure 8 shows how an NTC thermistor can be connected to make the bias voltage increase with temperature.

PC Board Layout and Grounding

Careful PC board layout is important for minimizing ground bounce and noise. In addition, keep all connections to FB as a short as possible. In particular, locate feedback resistors (R5, R6, and R8) as close to FB as possible. Use wide, short traces to interconnect large current paths for N1, D1, L1, C1, C2. Do not share these connections with other signal paths. Refer to the MAX1932 EV kit for a PC board layout example.

Chip Information

TRANSISTOR COUNT: 1592

PROCESS: BICMOS

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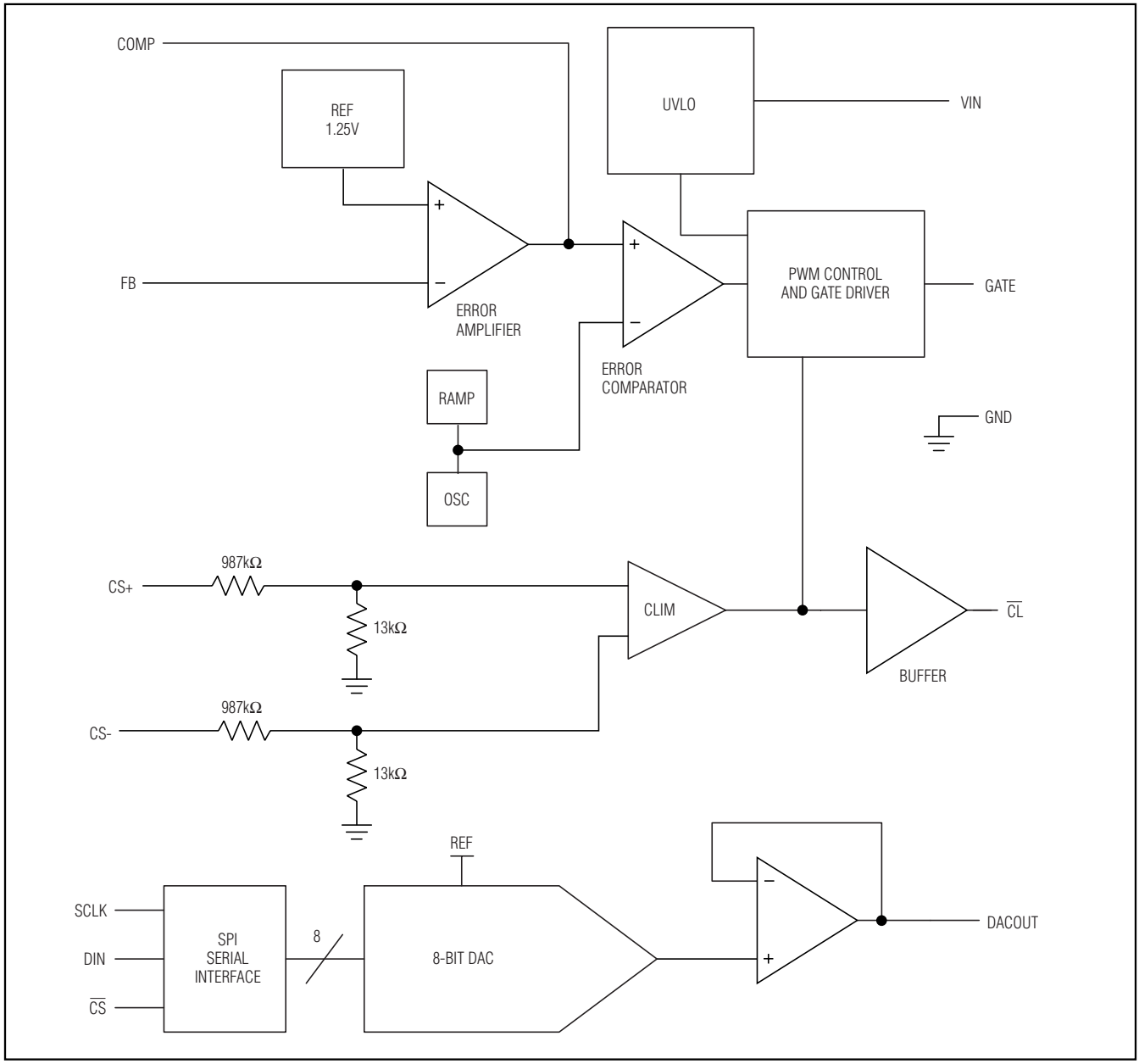

Figure 1. Functional Diagram

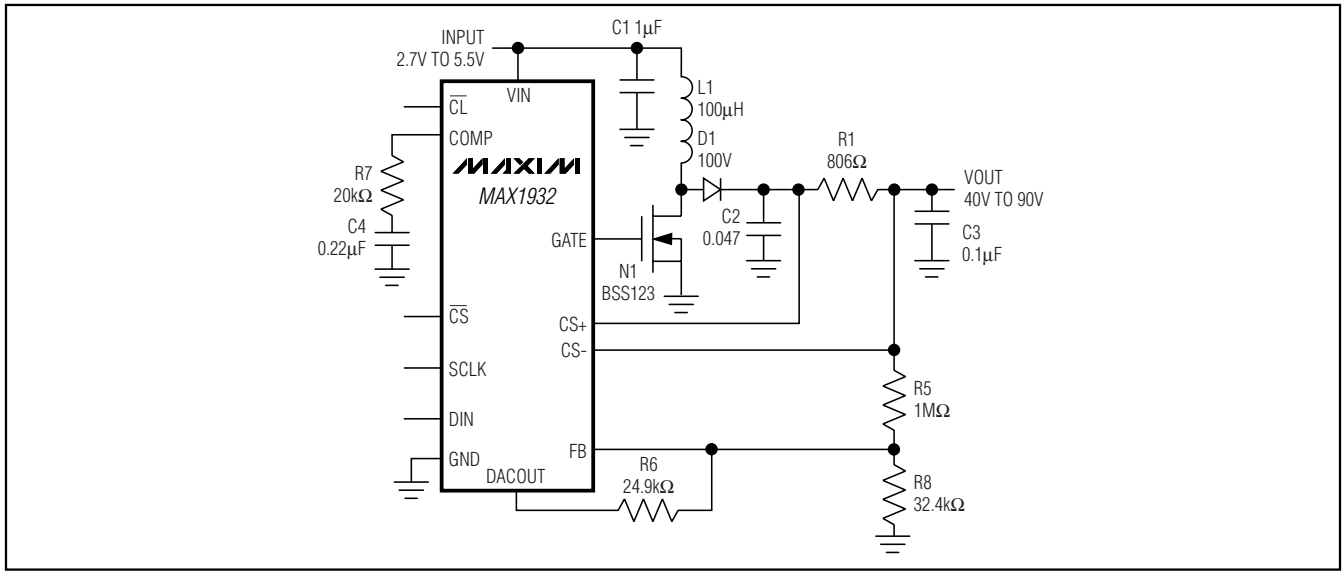

Figure 2. Typical Operating Circuit

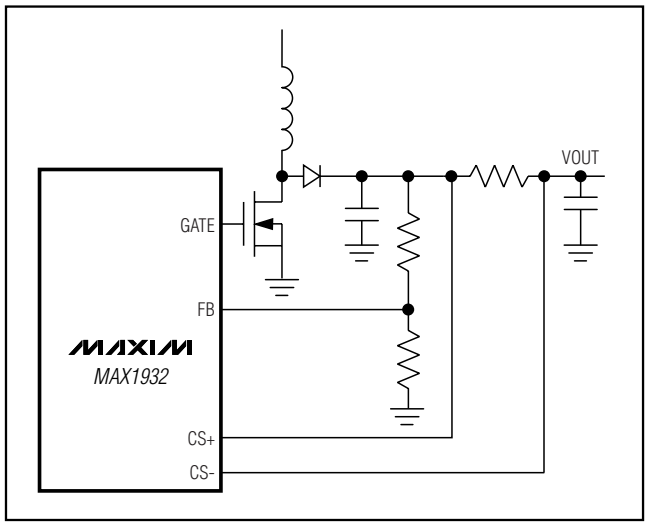

Figure 3. Taking Feedback Ahead of Output Filter

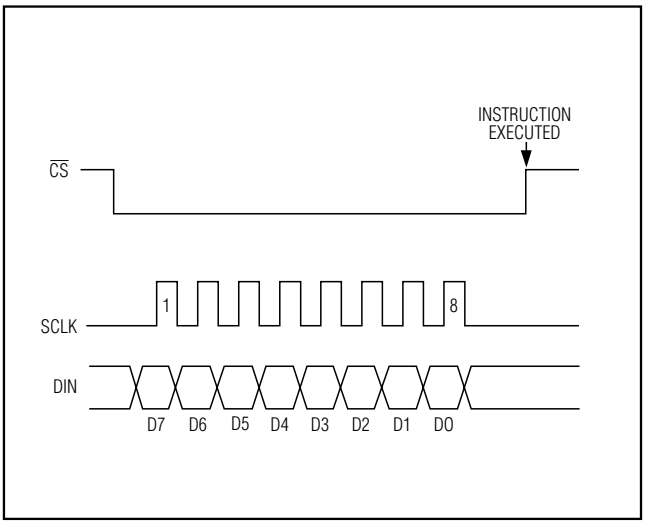

Figure 4. Serial Interface Timing Diagram

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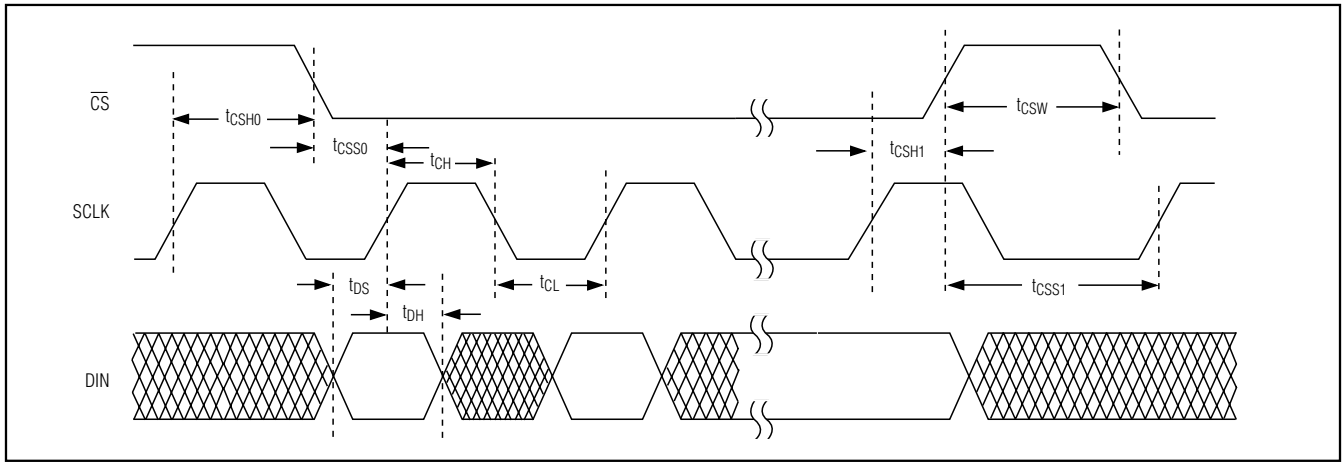
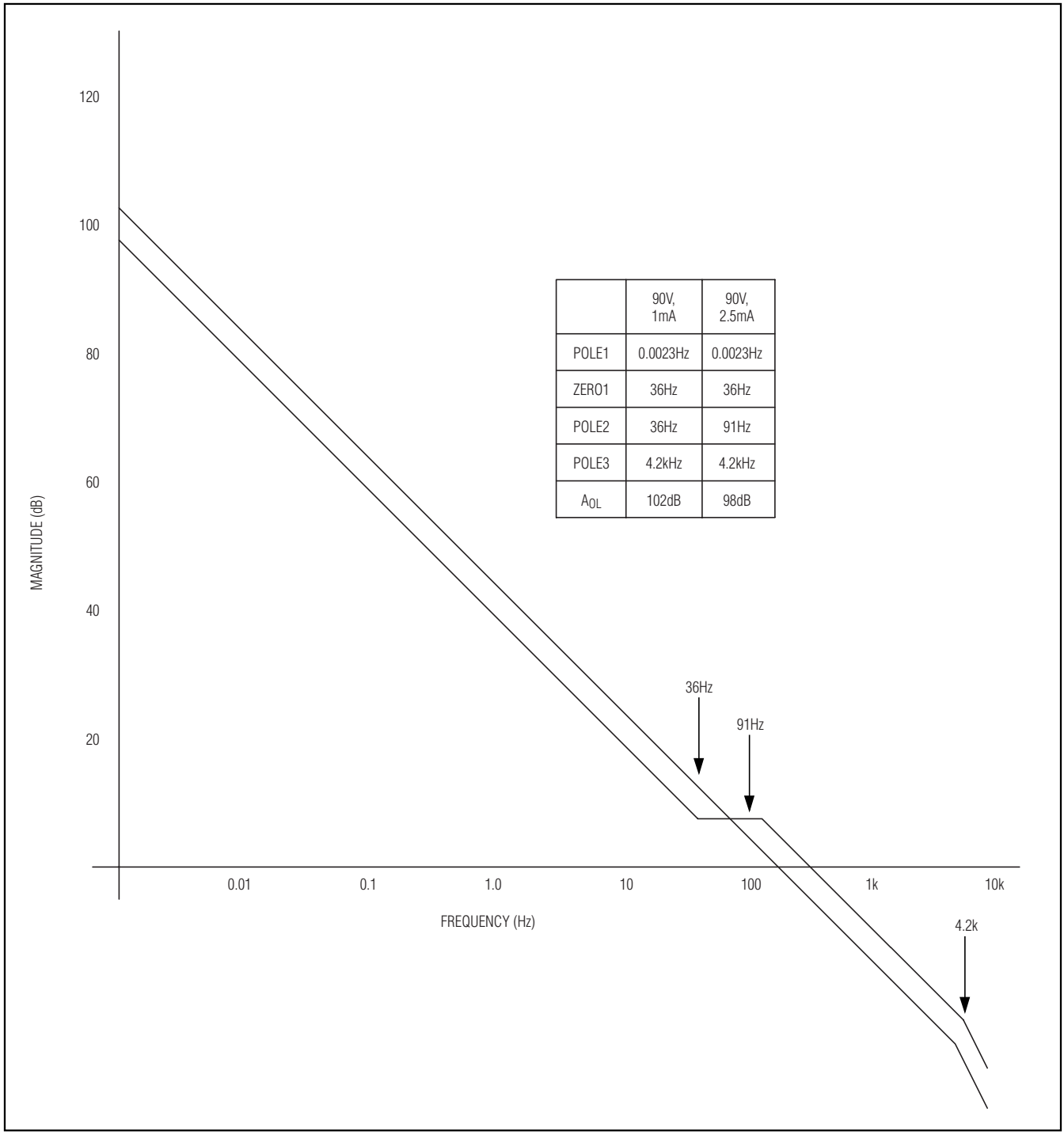


Figure 5. Detailed Serial Interface Timing Diagram



	90V, 1mA	90V, 2.5mA
POLE1	0.0023Hz	0.0023Hz
ZERO1	36Hz	36Hz
POLE2	36Hz	91Hz
POLE3	4.2kHz	4.2kHz
A_{OL}	102dB	98dB

Figure 6. Loop Response

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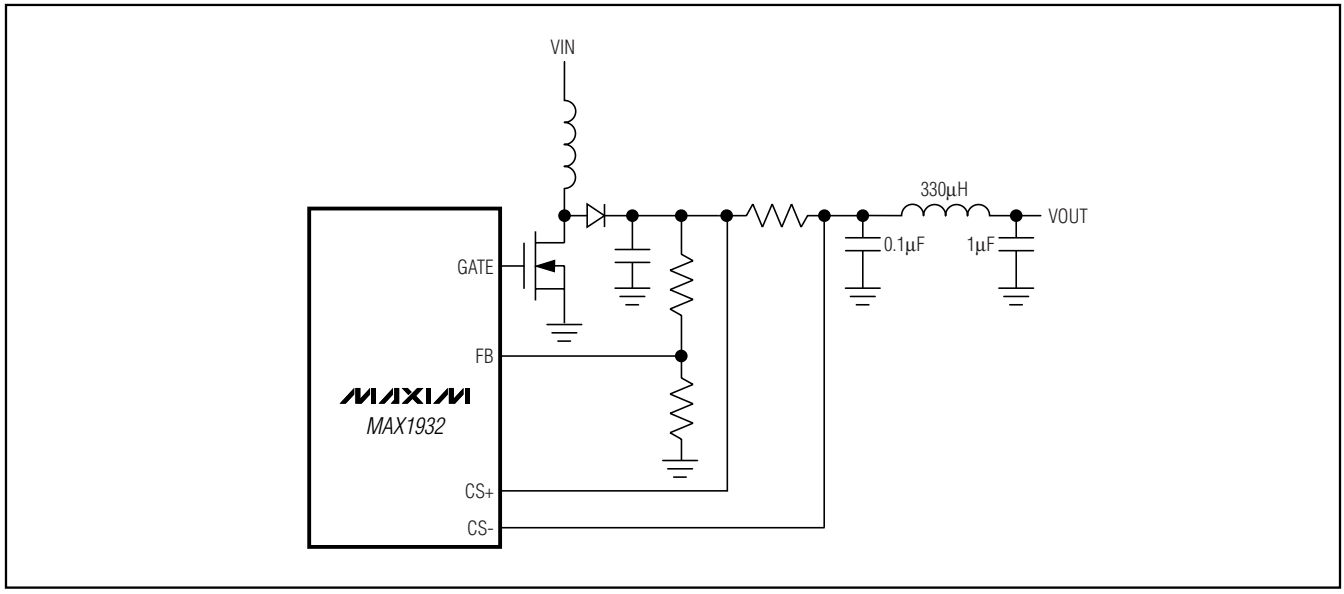

Figure 7. Adding a Post LC Filter

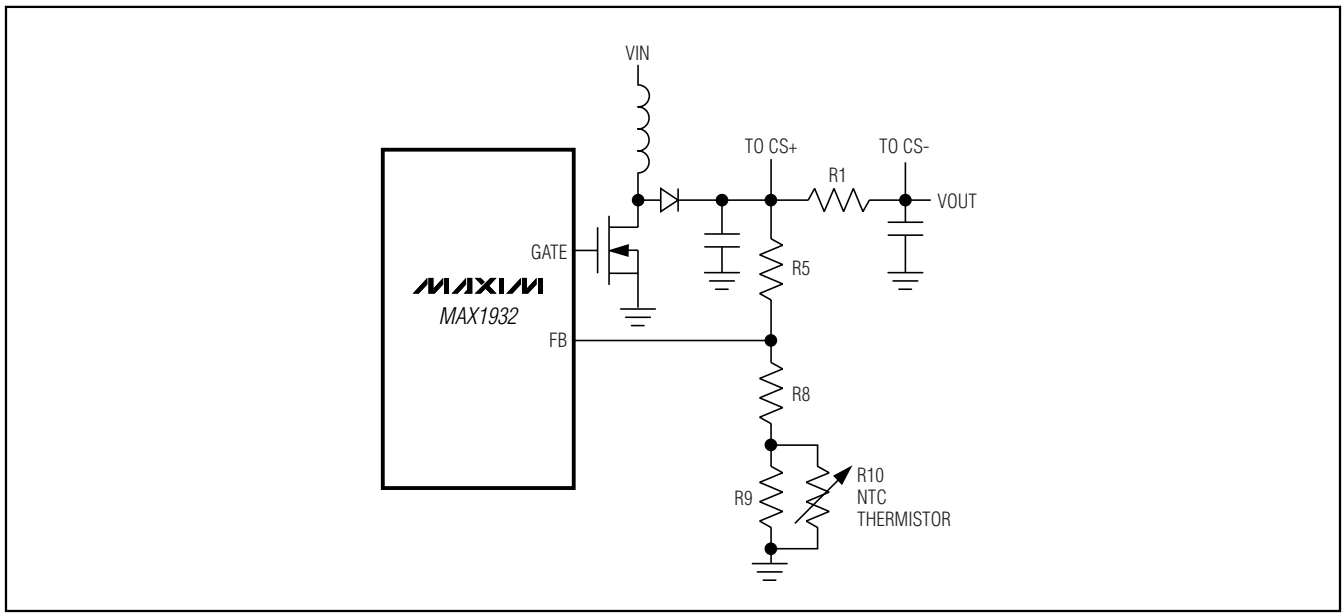

Figure 8. Adding an NTC Thermistor for Hardware Temperature Compensation; Output Voltage Increases with Temperature Rise

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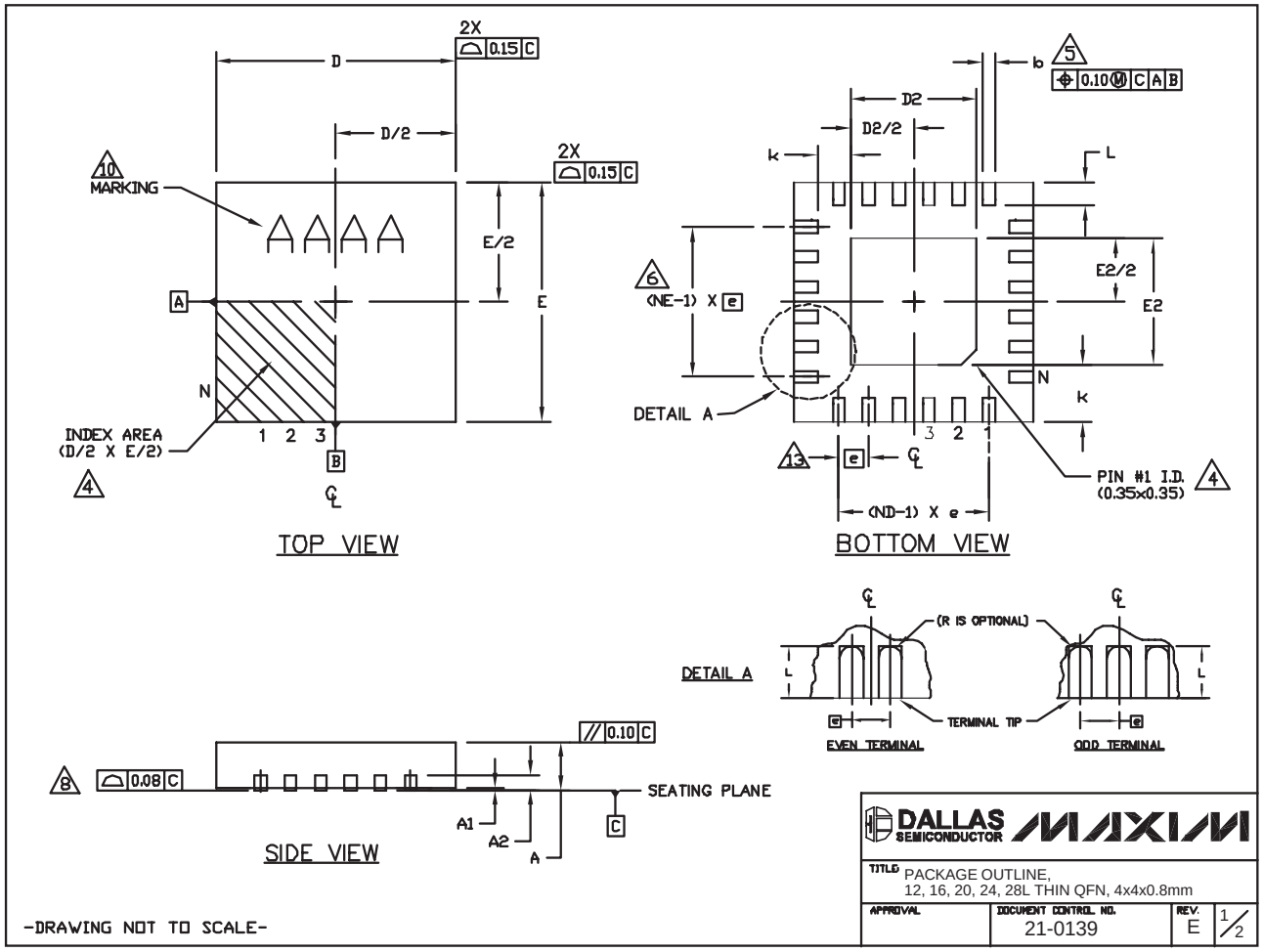
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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