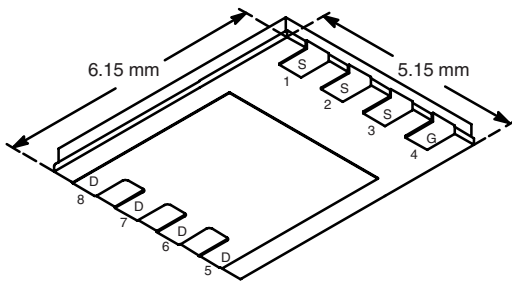


## N-Channel 30-V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ.)
30	0.0040 at $V_{GS} = 10$ V	25	47
	0.0048 at $V_{GS} = 4.5$ V	23	

PowerPAK SO-8



Bottom View

Ordering Information: Si7886ADP-T1-E3 (Lead (Pb)-free)  
Si7886ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

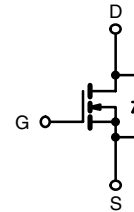
- Halogen-free available
- TrenchFET® Power MOSFET
- Optimized for “Low Side” Synchronous Rectifier Operation
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 %  $R_g$  Tested



**RoHS**  
COMPLIANT

### FEATURES

- DC/DC Converters
- Synchronous Rectifiers



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ , unless otherwise noted

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted					
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	30		V
Gate-Source Voltage		V <sub>GS</sub>	± 12		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	I <sub>D</sub>	25	15	A
	T <sub>A</sub> = 70 °C		20	12	
Pulsed Drain Current (10 μs Pulse Width)		I <sub>DM</sub>	60		
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	4.5	1.6	
Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	50		mJ
Single Pulse Avalanche Energy		E <sub>AS</sub>	125		
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C	P <sub>D</sub>	5.4	1.9	W
	T <sub>A</sub> = 70 °C		3.4	1.2	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>			260		

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	18	23	$^\circ\text{C}/\text{W}$
		50	65	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	1.0	1.5	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

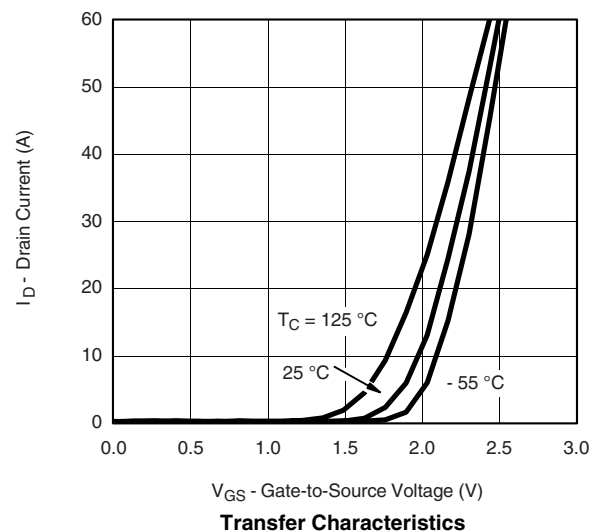
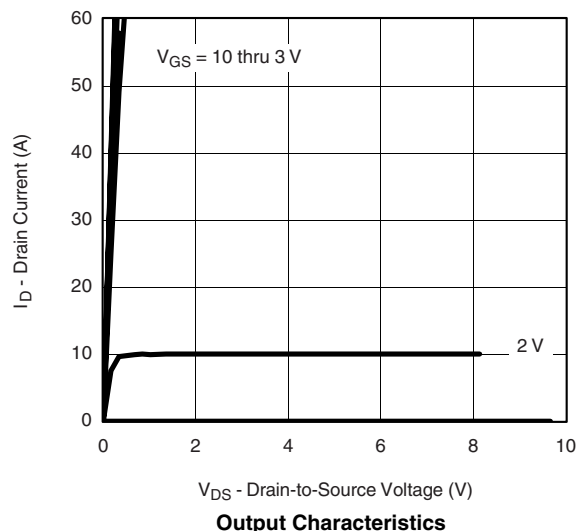
<b>SPECIFICATIONS</b> $T_J = 25^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	0.6	1	1.5	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\ \text{V}$ , $V_{GS} = \pm 12\ \text{V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\ \text{V}$ , $V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
		$V_{DS} = 30\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $T_J = 55^\circ\text{C}$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$ , $V_{GS} = 10\ \text{V}$	30			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}$ , $I_D = 25\ \text{A}$		0.0032	0.0040	$\Omega$
		$V_{GS} = 4.5\ \text{V}$ , $I_D = 23\ \text{A}$		0.0037	0.0048	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\ \text{V}$ , $I_D = 25\ \text{A}$		90		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 2.9\ \text{A}$ , $V_{GS} = 0\ \text{V}$		0.7	1.1	V
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15\ \text{V}$ , $V_{SS} = 0\ \text{V}$ , $f = 1\ \text{kHz}$		6450		pF
Output Capacitance	$C_{oss}$			873		
Reverse Transfer Capacitance	$C_{rss}$			402		
Total Gate Charge	$Q_g$	$V_{DS} = 15\ \text{V}$ , $V_{GS} = 4.5\ \text{V}$ , $I_D = 25\ \text{A}$		47	60	nC
Gate-Source Charge	$Q_{gs}$			12.5		
Gate-Drain Charge	$Q_{gd}$			9.0		
Gate Resistance	$R_g$		0.5	1.0	1.5	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$ , $R_L = 15\ \Omega$ $I_D \cong 1.0\ \text{A}$ , $V_{GEN} = 10\ \text{V}$ , $R_G = 6\ \Omega$		17	30	ns
Rise Time	$t_r$			14	25	
Turn-Off Delay Time	$t_{d(off)}$			158	230	
Fall Time	$t_f$			43	65	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 2.9\ \text{A}$ , $di/dt = 100\ \text{A}/\mu\text{s}$		50	80	

Notes:

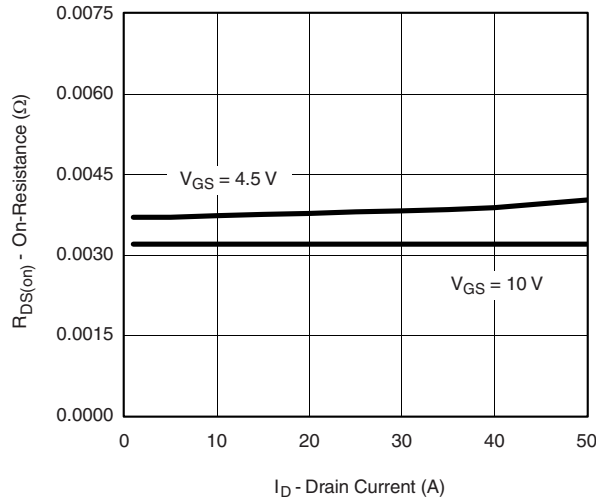
a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

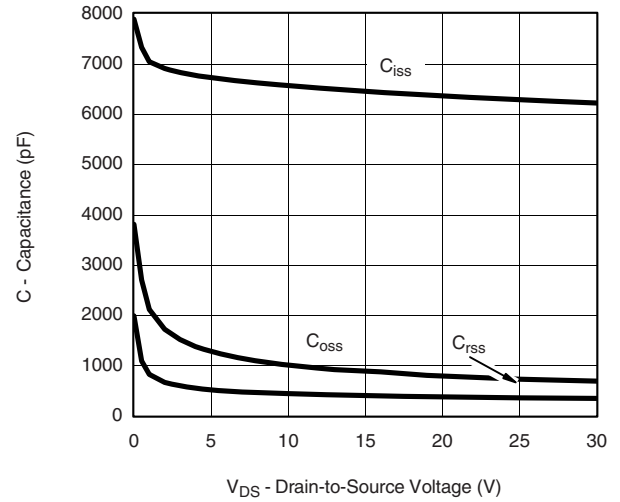
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS**  $25^\circ\text{C}$ , unless otherwise noted

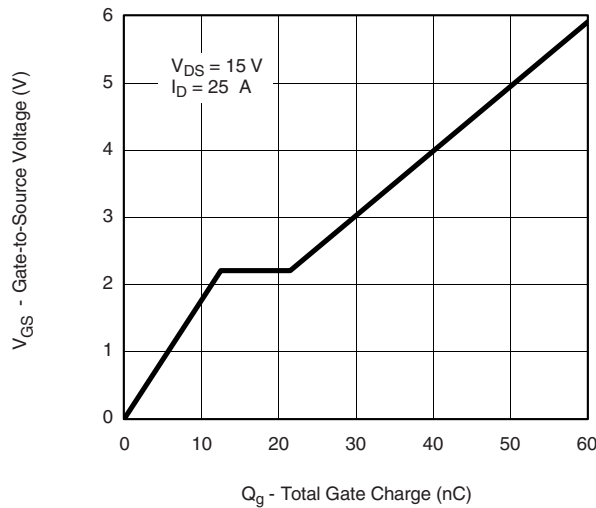
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



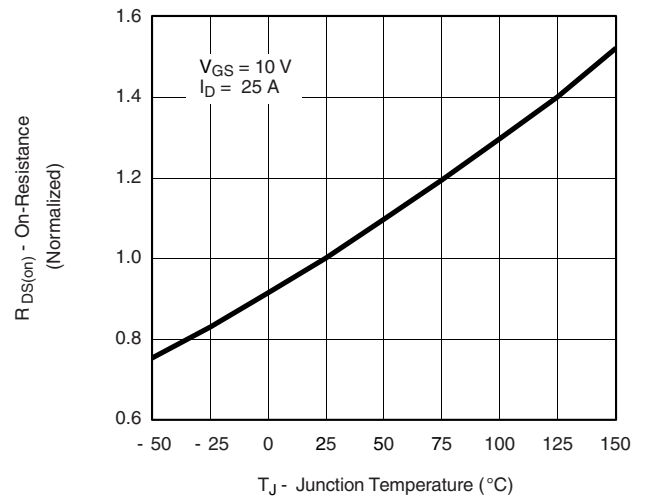
On-Resistance vs. Drain Current



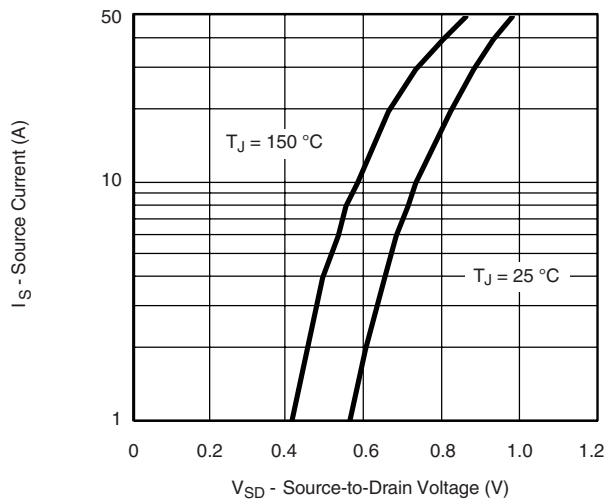
Capacitance



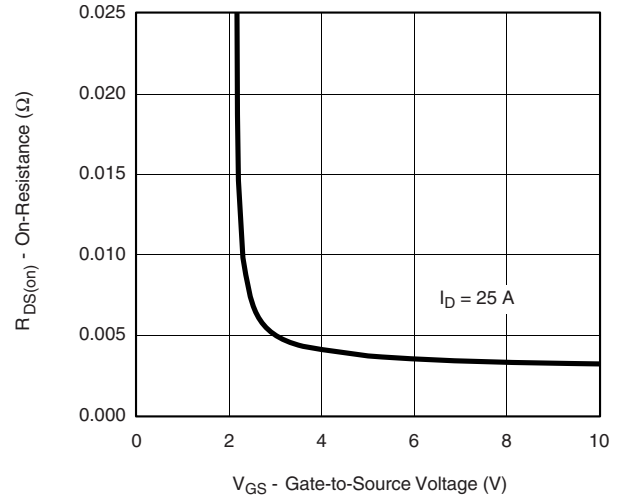
Gate Charge



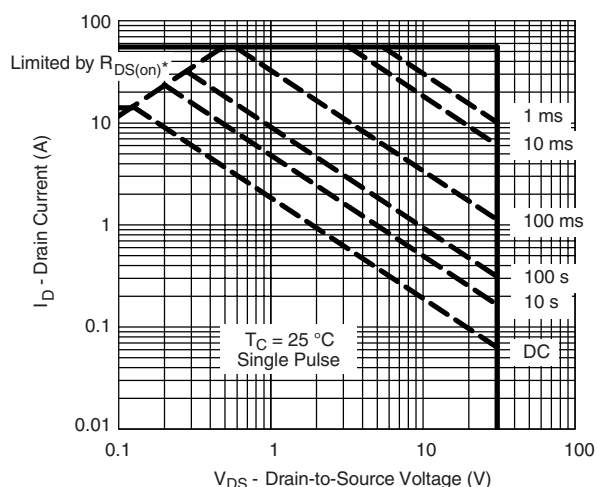
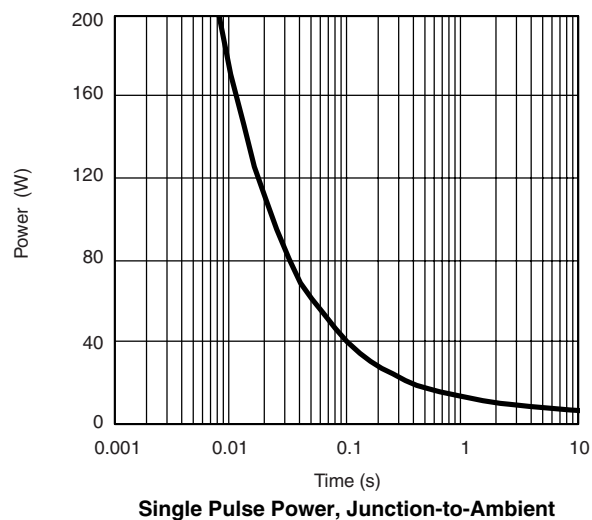
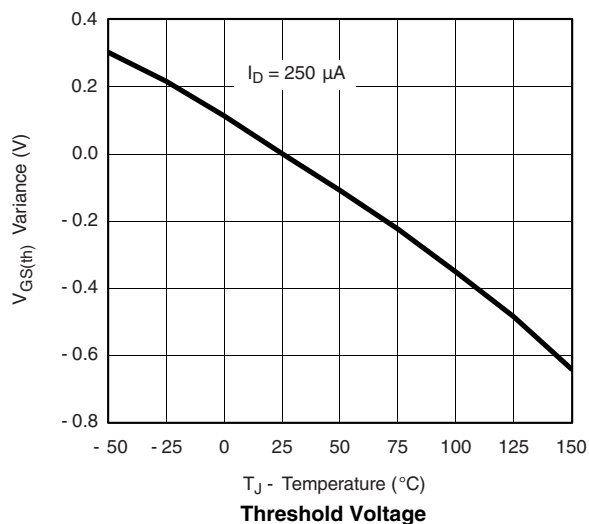
On-Resistance vs. Junction Temperature



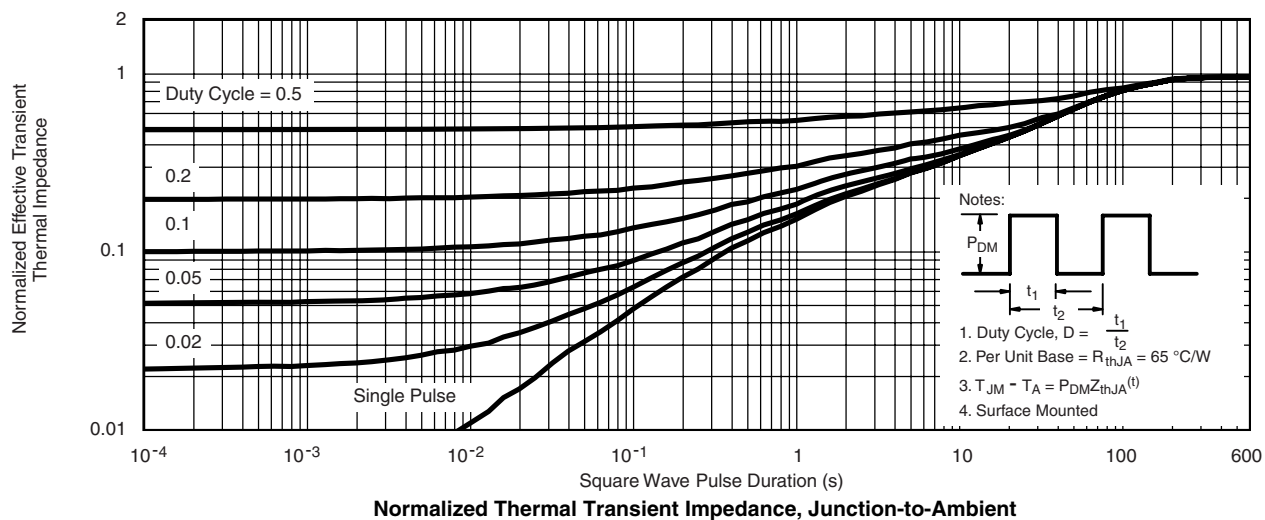
Source-Drain Diode Forward Voltage



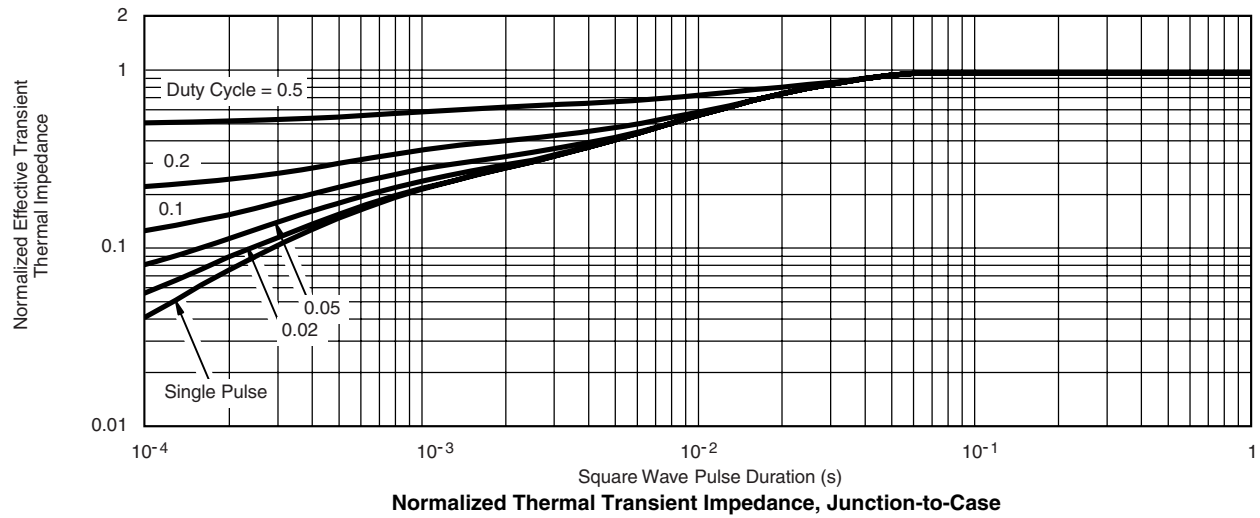
On-Resistance vs. Gate-to-Source Voltage

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Case**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73156>.

## PowerPAK® SO-8, (Single/Dual)



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4 (for AL product)	0.58 typ.			0.023 typ.		
E4 (for other product)	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K (for AL product)	1.45 typ.			0.057 typ.		
K (for other product)	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: C13-0702-Rev. K, 20-May-13						
DWG: 5881						

## RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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