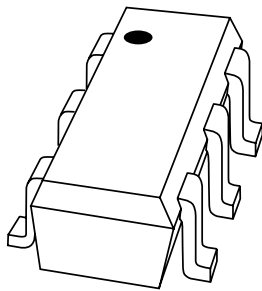


DATA SHEET



PUMB2 PNP resistor-equipped double transistor

Product specification

1999 Aug 03

PNP resistor-equipped double transistor

PUMB2

FEATURES

- Transistors with built-in bias resistors R1 and R2 (typ. 47 kΩ each)
- No mutual interference between the transistors
- Simplification of circuit design
- Reduces number of components and board space.

APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configurations without use of external resistors.

DESCRIPTION

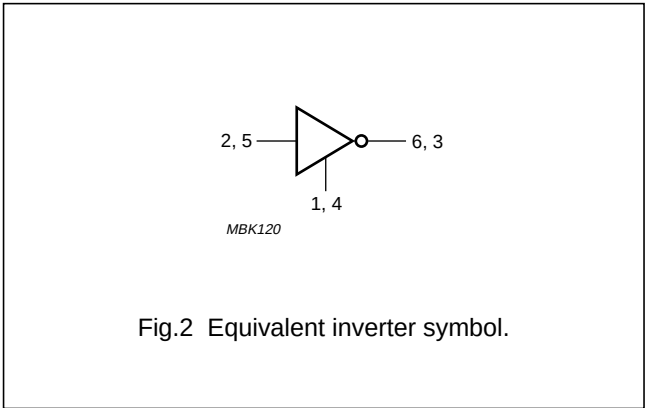
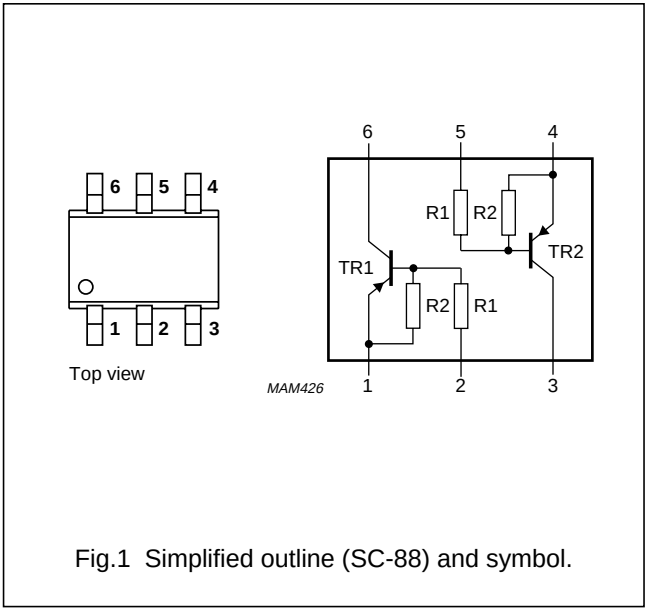
PNP resistor-equipped double transistor in an SC-88 (SOT363) plastic package.

MARKING

TYPE NUMBER	MARKING CODE
PUMB2	Bt2

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



PNP resistor-equipped double transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor					
V_{CBO}	collector-base voltage	open emitter	–	–50	V
V_{CEO}	collector-emitter voltage	open base	–	–50	V
V_{EBO}	emitter-base voltage	open collector	–	–10	V
V_I	input voltage				
	positive		–	+10	V
	negative		–	–40	V
I_O	output current (DC)		–	–100	mA
I_{CM}	peak collector current		–	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	300	mW

Note

1. Refer to SC-88 standard mounting conditions.

PNP resistor-equipped double transistor

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	416	K/W

Note

1. Refer to SC-88 standard mounting conditions.

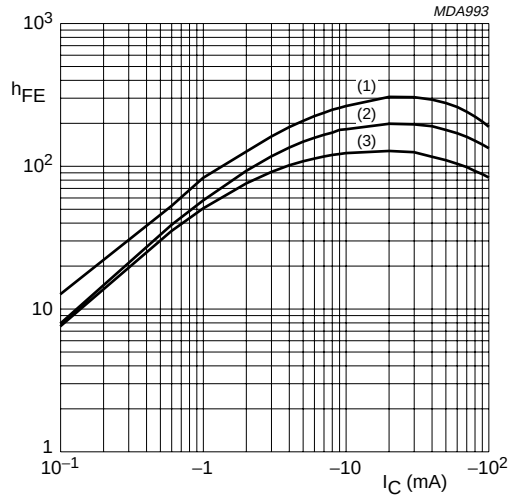
CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor						
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = -50\text{ V}$	–	–	–100	nA
I_{CEO}	collector cut-off current	$I_B = 0; V_{CE} = -30\text{ V}$	–	–	–1	μA
		$I_B = 0; V_{CE} = -30\text{ V}; T_j = 150\text{ °C}$	–	–	–50	μA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = -5\text{ V}$	–	–	–90	μA
h_{FE}	DC current gain	$I_C = -5\text{ mA}; V_{CE} = -5\text{ V}$	80	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10\text{ mA}; I_B = -0.5\text{ mA}$	–	–	–150	mV
$V_{i(off)}$	input-off voltage	$I_C = -100\text{ }\mu\text{A}; V_{CE} = -5\text{ V}$	–	1.2	0.8	V
$V_{i(on)}$	input-on voltage	$I_C = -2\text{ mA}; V_{CE} = -0.3\text{ V}$	3	1.6	–	V
$R1$	input resistor		33	47	61	k Ω
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$I_E = i_e = 0; V_{CB} = -10\text{ V}; f = 1\text{ MHz}$	–	–	3	pF

PNP resistor-equipped double transistor

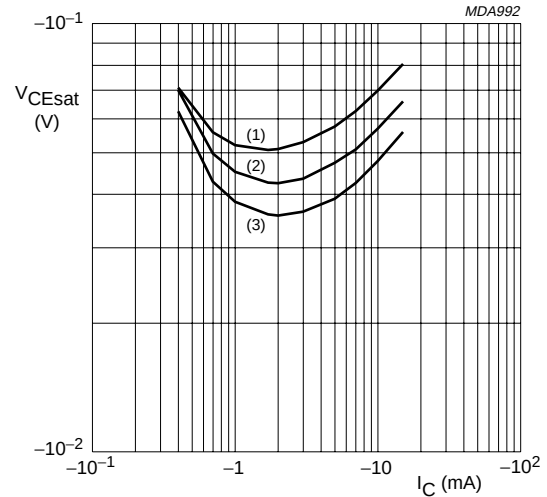
PUMB2



$V_{CE} = -5 \text{ V}$.

- (1) $T_{amb} = 150 \text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = -40 \text{ }^{\circ}\text{C}$.

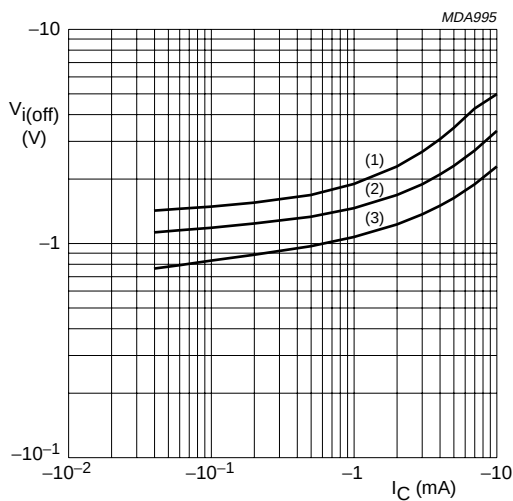
Fig.3 DC current gain as a function of collector current; typical values.



$I_C/I_B = 20$.

- (1) $T_{amb} = 100 \text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = -40 \text{ }^{\circ}\text{C}$.

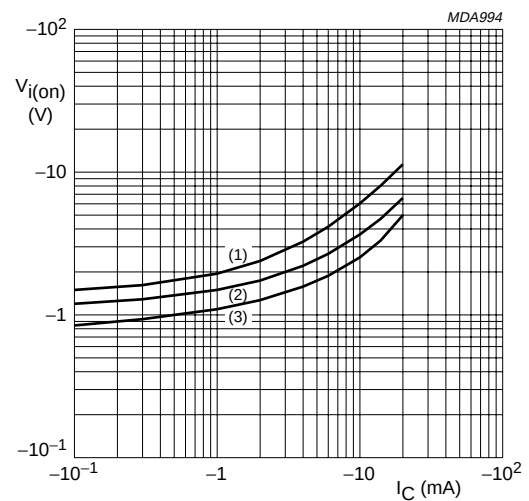
Fig.4 Collector-emitter saturation voltage as a function of collector current; typical values.



$V_{CE} = -5 \text{ V}$.

- (1) $T_{amb} = -40 \text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = 100 \text{ }^{\circ}\text{C}$.

Fig.5 Input-off voltage as a function of collector current; typical values.



$V_{CE} = -0.3 \text{ V}$.

- (1) $T_{amb} = -40 \text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = 100 \text{ }^{\circ}\text{C}$.

Fig.6 Input-on voltage as a function of collector current; typical values.

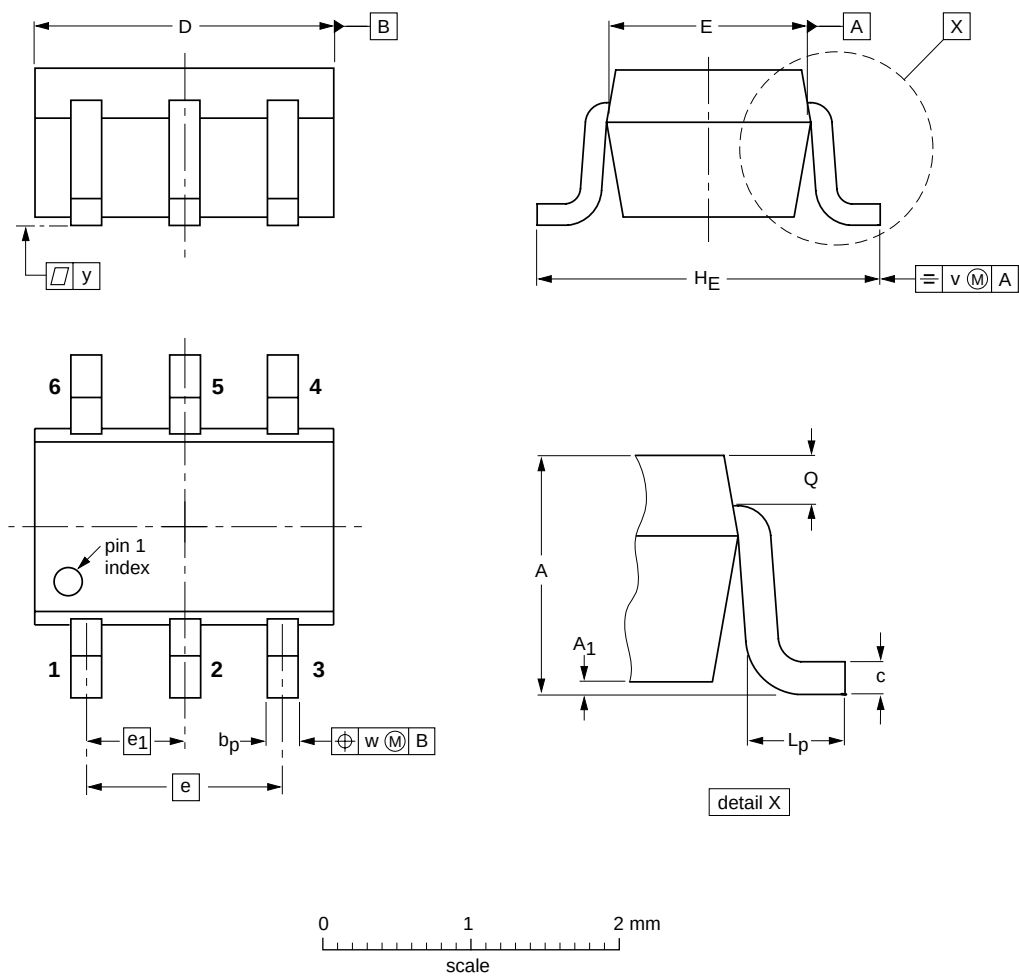
PNP resistor-equipped double transistor

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

PNP resistor-equipped double transistor

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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