Si5350C-B

Factory-Programmable Any-Frequency CMOS Clock Generator + PLL

Features

- www.silabs.com/custom-timing
- Generates up to 8 non-integer-related frequencies from 8 kHz to 160 MHz
- Exact frequency synthesis at each output (0 ppm error)
- Glitchless frequency changes
- Low output period jitter: < 70 ps pp, typ
- Configurable Spread Spectrum selectable at each output
- User-configurable control pins:
  - Output Enable (OEB_0/1/2)
  - Power Down (PDN)
  - Frequency Select (FS_0/1)
  - Spread Spectrum Enable (SSEN)
  - Loss of Lock Status (LOL)
- Supports static phase offset
- Rise/fall time control
- Operates from a low-cost, fixed frequency crystal: 25 or 27 MHz
- Separate voltage supply pins:
  - Core VDD: 2.5 V or 3.3 V
  - Output VDDO: 1.8 V, 2.5 V, or 3.3 V
- Excellent PSRR eliminates external power supply filtering
- Very low power consumption (<45 mA)
- Available in 2 packages types:
  - 10-MSOP: 3 outputs
  - 20-QFN (4x4 mm): 8 outputs
- PCIE Gen 1 compliant
- Supports HCSL compatible swing

10-MSOP

20-QFN

Ordering Information:

See Page 18

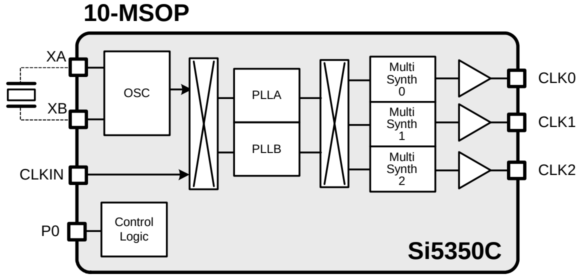
Applications

- HDTV, DVD/Blu-ray, set-top box
- Audio/video equipment, gaming
- Printers, scanners, projectors
- Residential gateways
- Networking/communication
- Servers, storage
- XO replacement

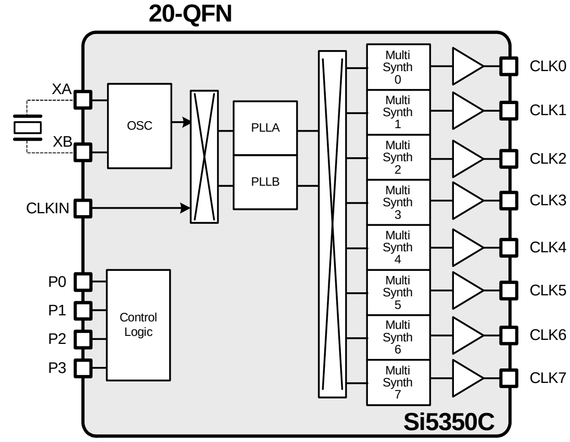
Description

The Si5350C generates free-running and/or synchronized clocks selectable on each of its outputs. A dual PLL + high resolution MultiSynth™ fractional divider architecture enables this user-definable custom timing device to generate any of the specified output frequencies at any of its outputs. This allows the Si5350C to replace a combination of crystals, crystal oscillators, and synchronized clocks (PLL). Custom pin-controlled Si5350C devices can be requested using the ClockBuilder web-based part number utility (www.silabs.com/ClockBuilder).

10-MSOP



20-QFN



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This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Core Supply Voltage	V_{DD}		3.0	3.3	3.6	V
			2.25	2.5	2.75	V
Output Buffer Voltage	V_{DDOx}		1.71	1.8	1.89	V
			2.25	2.5	2.75	V
			3.0	3.3	3.60	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted. VDD and VDDOx can be operated at independent voltages. Power supply sequencing for VDD and VDDOx requires that all VDDOx be powered up either before or at the same time as VDD.

Table 2. DC Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current*	I_{DD}	Enabled 3 outputs	—	20	35	mA
		Enabled 8 outputs	—	25	45	mA
		Power Down (PDN = V_{DD})	—	—	50	µA
Output Buffer Supply Current (Per Output)*	I_{DDOx}	C_L = 5 pF	—	2.2	5.0	mA
Input Current	I_{P1-P3}	Pins P1, P2, P3 V_{P1-P3} < 3.6 V	—	—	10	µA
	I_{P0}	Pin P0	—	—	30	µA
Output Impedance	Z_{OI}	3.3 V VDDO, default high drive.	—	50	—	Ω

***Note:** Output clocks less than or equal to 100 MHz.

Table 3. AC Characteristics
(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power-Up Time	T_{RDY}	From V_{DD} = V_{DDmin} to valid output clock, C_L = 5 pF, f_{CLKn} > 1 MHz	—	2	10	ms
Power-Down Time	T_{PD}	From V_{DD} = V_{DDmin}, C_L = 5 pF, f_{CLKn} > 1 MHz	—	5	100	ms
Output Enable Time	T_{OE}	From OEB assertion to valid clock output, C_L = 5 pF, f_{CLKn} > 1 MHz	—	—	10	µs
Output Frequency Transition Time	T_{FREQ}	f_{CLKn} > 1 MHz	—	—	10	µs
Spread Spectrum Frequency Deviation	SS_{DEV}	Down Spread Selectable in 0.1% steps	–0.1	—	–2.5	%
Spread Spectrum Modulation Rate	SS_{MOD_C}		30	31.5	33	kHz

Table 4. Input Characteristics
(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency	f_{XTAL}		25	—	27	MHz
P0-P3 Input Low Voltage	V_{IL_P0-3}		–0.1	—	0.3 x V_{DD}	V
P0-P3 Input High Voltage	V_{IH_P0-3}		0.7 x V_{DD}	—	3.60	V
CLKIN Frequency Range	f_{CLKIN}		10	—	100	MHz
CLKIN Input Low Voltage	V_{IL_CLKIN}		–0.1	—	0.3 x V_{DD}	V
CLKIN Input High Voltage	V_{IH_CLKIN}		0.7 x V_{DD}	—	3.60	V

Table 5. Output Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency Range	F_{CLK}		0.008	—	160	MHz
Load Capacitance	C_L	F_{CLK} < 100 MHz	—	—	15	pF
Duty Cycle	DC	Measured at $V_{DD}/2$	45	50	55	%
Rise/Fall Time	t_r/t_f	20%–80%, C_L = 5 pF	—	1	1.5	ns
Output High Voltage	V_{OH}	C_L = 5 pF	V_{DD} – 0.6	—	—	V
Output Low Voltage	V_{OL}		—	—	0.6	V
Period Jitter*	J_{PER}	20-QFN, 4 outputs running, 1 per VDDO	-	40	95	ps, pk-pk
		10-MSOP or 20-QFN, all outputs running	-	70	140	ps, pk-pk
Cycle-to-cycle Jitter*	J_{CC}	20-QFN, 4 outputs running, 1 per VDDO	—	50	90	ps, pk
		10-MSOP or 20-QFN, all outputs running	—	70	130	ps, pk

***Note:** Measured over 10k cycles. Jitter is highly dependent on device frequency configuration. Specifications represent a "worst case, real world" frequency plan; actual performance may be substantially better. For 3 output 10-MSOP package, measured with clock outputs of 74.25, 24.576, 48 MHz. For 8 output 20-QFN package, measured with clock outputs of 33.33, 74.25, 27, 24.576, 22.5792, 28.322, 125, 48 MHz.

Table 6. 25 MHz Crystal Requirements[1,2]

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	—	25	—	MHz
Load Capacitance	C_L	6	—	12	pF
Equivalent Series Resistance	r_{ESR}	—	—	150	Ω
Crystal Max Drive Level	d_L	—	—	100	µW

Notes:

1. Crystals which require load capacitances of 6, 8, or 10 pF should use the device's internal load capacitance for optimum performance. See register 183 bits 7:6. A crystal with a 12 pF load capacitance requirement should use a combination of the internal 10 pF load capacitors in addition to external 2 pF load capacitors. Adding external 2 pF load capacitors can minimize jitter by 20%
2. Refer to "AN551: Crystal Selection Guide" for more details.

Table 7. 27 MHz Crystal Requirements[1,2]

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	—	27	—	MHz
Load Capacitance	C_L	6	—	12	pF
Equivalent Series Resistance	r_{ESR}	—	—	150	Ω
Crystal Max Drive Level	d_L	—	—	100	µW

Notes:

1. Crystals which require load capacitances of 6, 8, or 10 pF should use the device's internal load capacitance for optimum performance. See register 183 bits 7:6. A crystal with a 12 pF load capacitance requirement should use a combination of the internal 10 pF load capacitors in addition to external 2 pF load capacitors. Adding external 2 pF load capacitors can minimize jitter by 20%
2. Refer to "AN551: Crystal Selection Guide" for more details.

Table 8. Thermal Characteristics

Parameter	Symbol	Test Condition	Package	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	10-MSOP	131	°C/W
			20-QFN	51	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	10-MSOP	43	°C/W
			20-QFN	16	°C/W

Table 9. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD_max}		–0.5 to 3.8	V
Input Voltage	VIN_P1-3	Pins P1, P2, P3	–0.5 to 3.8	V
	VIN_P0	P0	–0.5 to (VDD+0.3)	V
	VIN_XA/B	Pins XA, XB	–0.5 to 1.3 V	V
Junction Temperature	T_J		–55 to 150	°C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Typical Application

2.1. Si5350C Replaces Multiple Clocks and XOs

The Si5350C is a clock generation device that provides both synchronous and free-running clocks for applications where power, board size, and cost are critical. An example application is shown in Figure 1. Any other combination is possible.

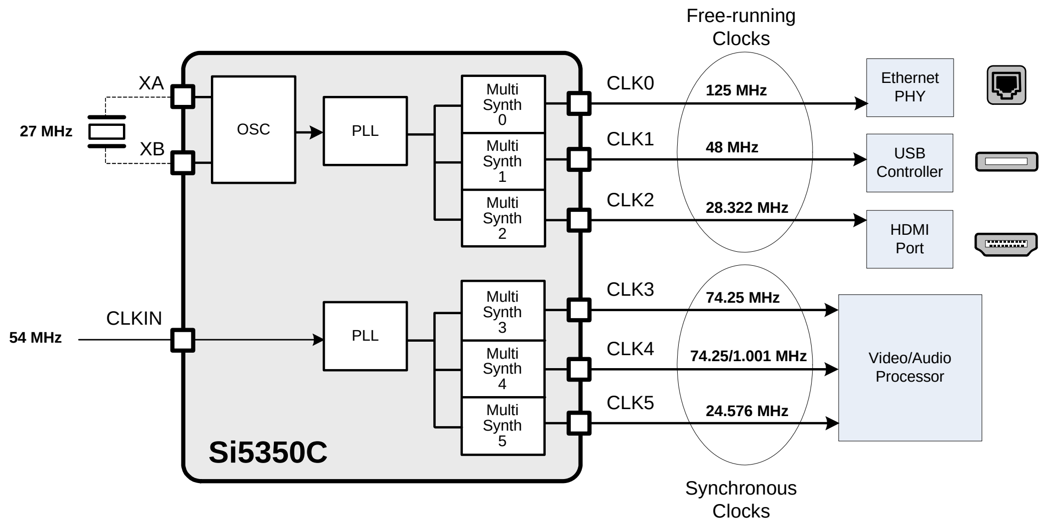
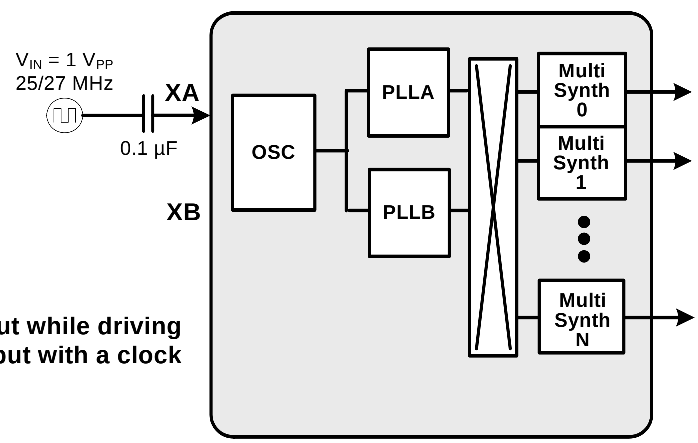


Figure 1. Replacing multiple XTAL/XOs and PLLs with one Si5350C

2.2. Applying a Reference Clock at XTAL Input

The Si5350C can be driven with a clock signal through the XA input pin. This is especially useful when in need of generating clock outputs in two synchronization domains; one reference clock can be provided at the CLKIN pin and at XA.



Note: Float the XB input while driving the XA input with a clock

Figure 2. Si5350C Driven by a Clock Signal

2.3. HCSL Compatible Outputs

The Si5351 can be configured to support HCSL compatible swing when the VDDO of the output pair of interest is set to 2.5 V (i.e., VDDOA must be 2.5 V when using CLK0/1; VDDOB must be 2.5 V for CLK2/3 and so on).

The circuit in the figure below must be applied to each of the two clocks used, and one of the clocks in the pair must also be inverted to generate a differential pair.

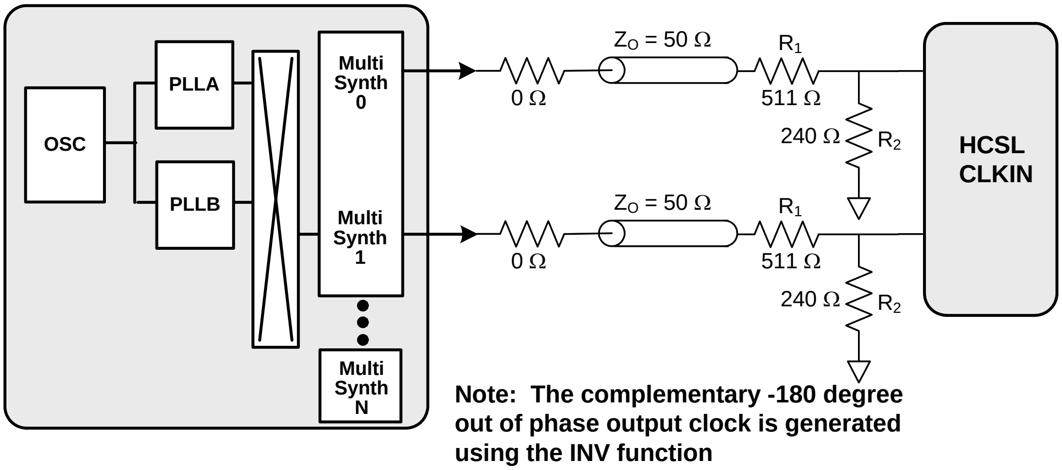


Figure 3. Si5350C Output is HCSL Compatible

3. Functional Description

The architecture of the Si5350C generates up to eight non-integer-related frequencies in any combination of free-running and/or synchronous clocks. A block diagram of both the 3-output and the 8-output versions are shown in Figure 4. Free-running clocks are generated using the on-chip oscillator + PLL, and the clock input pin (CLKIN) provides an external input reference for the synchronous clocks. Each MultiSynth™ is configurable with two frequencies (F1_x, F2_x). This allows a pin controlled glitchless frequency change at each output (CLK0 to CLK5).

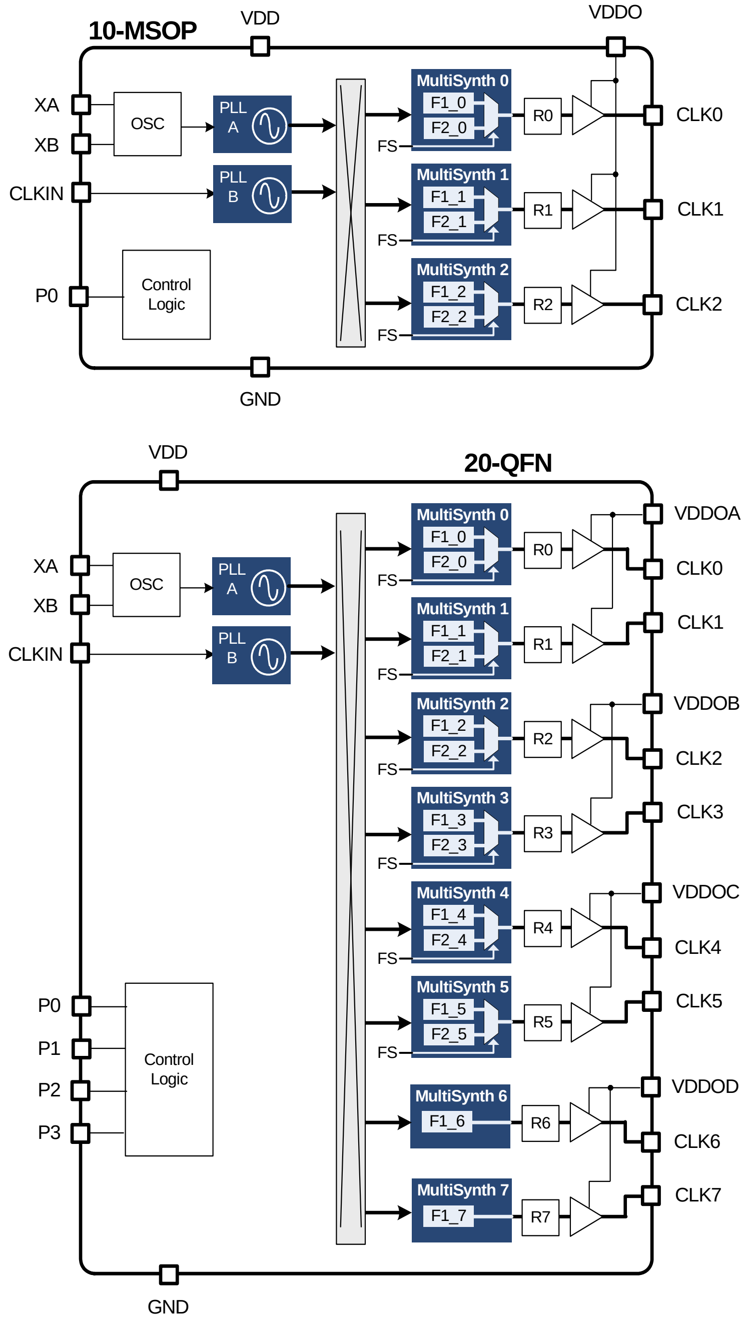


Figure 4. Block Diagrams of the Si5350C Devices with 3 and 8 outputs

4. Configuring the Si5350C

The Si5350C is a factory-programmed custom clock generator that is user definable with a simple to use web-based utility (www.silabs.com/ClockBuilder). The ClockBuilder utility provides a simple graphical interface that allows the user to enter input and output frequencies along with other custom features as described in the following sections. All synthesis calculations are automatically performed by ClockBuilder to ensure an optimum configuration. A unique part number is assigned to each custom configuration.

4.1. Crystal Inputs (XA, XB)

The Si5350C uses an optional fixed-frequency non-pullable standard AT-cut crystal as a reference to generate free-running output clocks. Note that a XTAL is not required for generating synchronous clocks that are locked to CLKIN.

4.1.1. Crystal Frequency

The Si5350C can operate using either a 25 MHz or a 27 MHz crystal.

4.1.2. Internal XTAL Load Capacitors

Internal load capacitors (C_L) are provided to eliminate the need for external components when connecting a XTAL to the Si5350C. Options for internal load capacitors are 6, 8, or 10 pF. XTALs with alternate load capacitance requirements are supported using external load capacitors < 2 pF as shown in Figure 5.

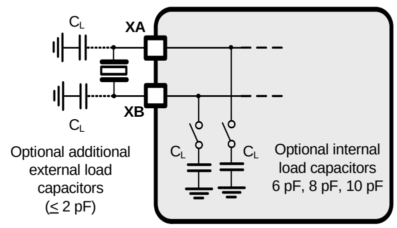


Figure 5. External XTAL with Optional Load Capacitors

4.2. External Clock Input Pin (CLKIN)

The external clock input is used as a reference for generating synchronous clocks. The input frequency can be specified from 10 to 100 MHz including fractional frequencies (e.g., 74.25 MHz x 1000/1001). The ClockBuilder utility automatically determines the exact synthesis ratio to guarantee an output frequency with 0 ppm error with respect to its reference.

4.3. Output Clocks (CLK0–CLK7)

The Si5350C is orderable as a 3-output (10-MSOP) or 8-output (20-QFN) clock generator. Output clocks CLK0 to CLK5 can be ordered with two clock frequencies (F1_x, F2_x) which are selectable with the optional frequency select pins (FS0/1). See “4.4.2. Power Down (PDN)” for more details on the operation of the frequency select pins. Each output clock can select its reference for either of the PLLs.

4.3.1. Output Clock Frequency

Outputs can be configured at any frequency from 8 kHz up to 112.5 MHz. In addition, the device can generate any frequency up to 160 MHz on two of its outputs.

4.3.2. Spread Spectrum

Spread spectrum can be enabled on any of the clock outputs that use PLLA as its reference. Spread spectrum is useful for reducing electromagnetic interference (EMI). Enabling spread spectrum on an output clock modulates its frequency, which effectively reduces the overall amplitude of its radiated energy. Note that spread spectrum is not available on clocks synchronized to PLLB.

The Si5350C supports several levels of spread spectrum allowing the designer to choose an ideal compromise between system performance and EMI compliance.

An optional spread spectrum enable pin (SSEN) is configurable to enable or disable the spread spectrum feature. See “4.4.1. Spread Spectrum Enable (SSEN)” for details.

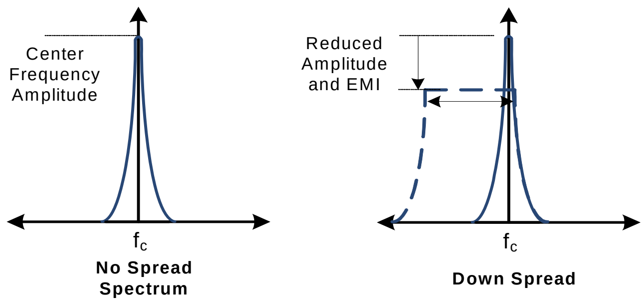


Figure 6. Available Spread Spectrum Profiles

4.3.3. Invert/Non-Invert

By default, each of the output clocks are generated in phase (non-inverted) with respect to each other. An option to invert any of the clock outputs is also available.

4.3.4. Output State When Disabled

There are up to three output enable pins configurable on the Si5350C as described in “4.4.4. Output Enable (OEB_0, OEB_1, OEB_2)” . The output state when disabled for each of the outputs is configurable as output high, output low, or high-impedance.

4.3.5. Powering Down Unused Outputs

Unused clock outputs can be completely powered down to conserve power.

4.4. Programmable Control Pins (P0–P3) Options

Up to four programmable control pins (P0-P3) are configurable allowing direct pin control of the following features:

4.4.1. Spread Spectrum Enable (SSEN)

An optional control pin allows disabling the spread spectrum feature for all outputs that were configured with spread spectrum enabled. Hold SSEN low to disable spread spectrum. The SSEN pin provides a convenient method of evaluating the effect of using spread spectrum clocks during EMI compliance testing.

4.4.2. Power Down (PDN)

An optional power down control pin allows a full shutdown of the Si5350C to minimize power consumption when its output clocks are not being used. The Si5350C is in normal operation when the PDN pin is held low and is in power down mode when held high. Power consumption when the device is in power down mode is indicated in Table 2 on page 4.

4.4.3. Frequency Select (FS_0, FS_1)

The Si5350C offers the option of configuring up to two frequencies per clock output (CLK0-CLK5) for either free-running or synchronous clocks. This is a useful feature for applications that need to support more than one free-running or synchronous clock rate on the same output. An example of this is shown in Figure 7. The FS pins select which frequency is generated from the clock output. In this example, FS0 selects the output frequency on CLK0 and FS1 selects the frequency on CLK1.

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FS0 Bit Level	Free-running Frequency	
0	F1_0:	74.25 MHz
1	F2_0:	$\frac{74.25}{1.001}$ MHz

FS1 Bit Level	Synchronous Frequency	
0	F1_1:	24.576 MHz
1	F2_1:	22.5792 MHz

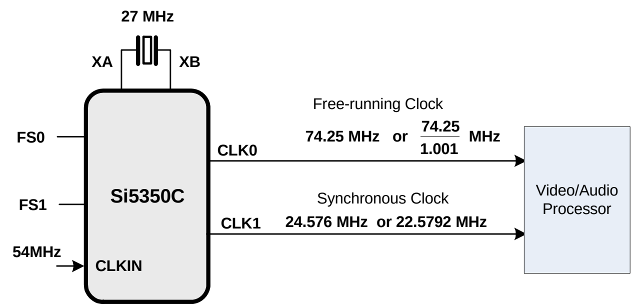

Figure 7. Example of Generating Two Clock Frequencies from the Same Clock Output

Up to two frequency select pins are available on the Si5350C. Each of the frequency select pins can be linked to any of the clock outputs as shown in Figure 8. For example, FS_0 can be linked to control clock frequency selection on CLK0, CLK3, and CLK5; FS_1 can be used to control clock frequency selection on CLK1, CLK2, and CLK4. Any other combination is also possible.

The Si5350C uses control circuitry to ensure that frequency changes are glitchless. This ensures that the clock always completes its last cycle before starting a new clock cycle of a different frequency.

FS_0	Output Frequency
0	F1_0, F1_3, F1_5
1	F2_0, F2_3, F2_5

FS_1	Output Frequency
0	F1_1, F1_2, F1_4
1	F2_1, F2_2, F2_4

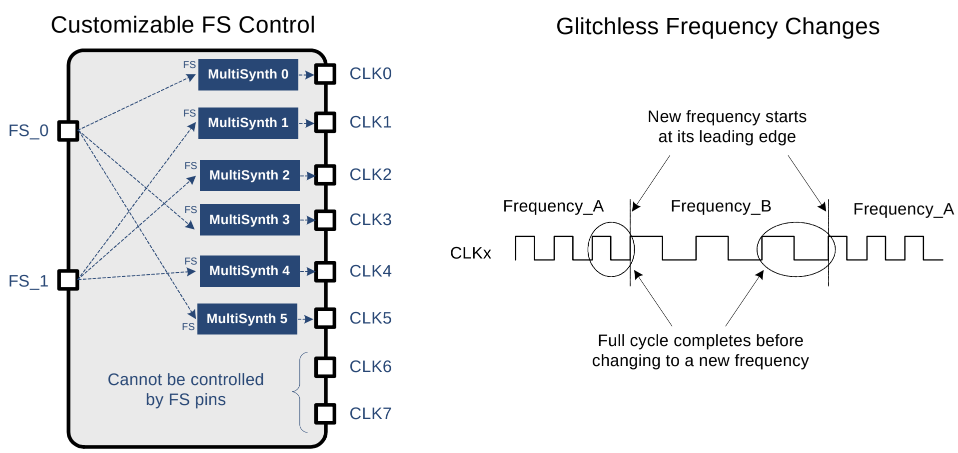

Figure 8. Example Configuration of a Pin-Controlled Frequency Select (FS)

4.4.4. Output Enable (OEB_0, OEB_1, OEB_2)

Up to three output enable pins (OEB_0/1/2) are available on the Si5350C. Similar to the FS pins, each OEB pin can be linked to any of the output clocks. In the example shown in Figure 9, OEB_0 is linked to control CLK0, CLK3, and CLK5; OEB_1 is linked to control CLK6 and CLK7, and OEB_2 is linked to control CLK1, CLK2, CLK4, and CLK5. Any other combination is also possible. If more than one OEB pin is linked to the same CLK output, the pin forcing a disable state will be dominant. Clock outputs are enabled when the OEB pin is held low.

The output enable control circuitry ensures glitchless operation by starting the output clock cycle on the first leading edge after OEB is asserted (OEB = low). When OEB is released (OEB = high), the clock is allowed to complete its full clock cycle before going into a disabled state. This is shown in Figure 9. When disabled, the output state is configurable as disabled high, disabled low, or disabled in high-impedance.

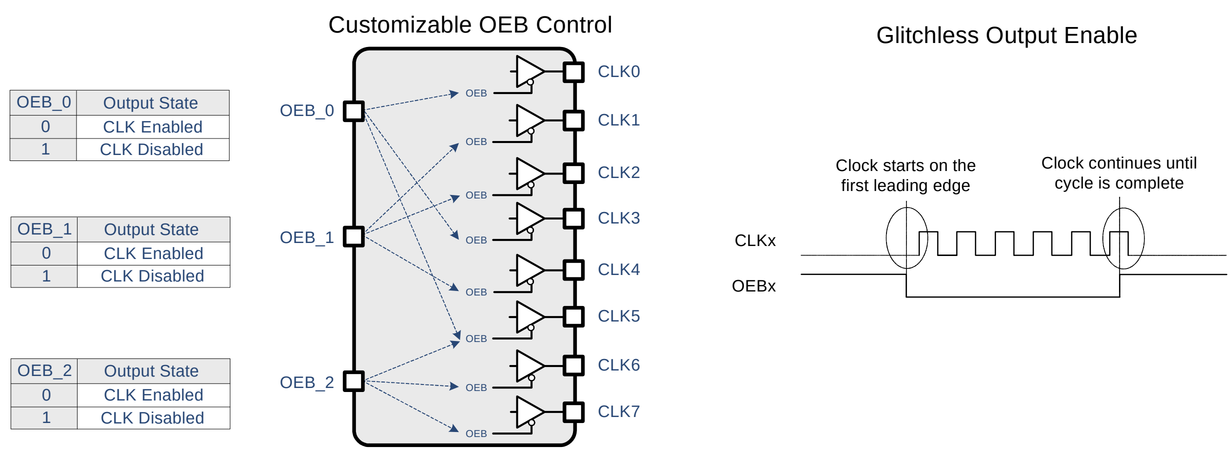

Figure 9. Example Configuration of a Pin-Controlled Output Enable

4.4.5. Loss Of Lock (LOL)

A loss of lock pin (LOL) is available to indicate the status of the synchronous clock outputs. The LOL pin is set to a low state when the synchronous clock outputs are locked to the clock input (CLKIN). This is the normal operating state for the synchronous clocks. The LOL pin will go high when the reference clock at the CLKIN input is removed or if its frequency deviates by more than 2000 ppm from its defined center frequency. In this case, the synchronous clocks will continue to free-run. An option to disable the synchronous output clocks during an LOL condition (LOL pin = high) is available. This only affects the clock outputs that were designated as synchronous clock outputs.

4.5. Design Considerations

The Si5350C is a self-contained clock generator that requires very few external components. The following general guidelines are recommended to ensure optimum performance.

4.5.1. Power Supply Decoupling/Filtering

The Si5350C has built-in power supply filtering circuitry to help keep the number of external components to a minimum. All that is recommended is one 0.1 to 1.0 µF decoupling capacitor per power supply pin. This capacitor should be mounted as close to the VDD and VDDO pins as possible without using vias.

4.5.2. Power Supply Sequencing

The VDD and VDDOx (i.e., VDDO0, VDDO1, VDDO2, VDDO3) power supply pins have been separated to allow flexibility in output signal levels. If a minimum output-to-output skew is important, then all VDDOx must be applied before or at the same time as VDD. Unused VDDOx pins should be tied to VDD.

4.5.3. External Crystal

The external crystal should be mounted as close to the pins as possible using short PCB traces. The XA and XB traces should be kept away from other high-speed signal traces. See “AN551: Crystal Selection Guide” for more details.

4.5.4. External Crystal Load Capacitors

The Si5350C provides the option of using internal and external crystal load capacitors. If external load capacitors are used, they should be placed as close to the XA/XB pads as possible. See “AN551: Crystal Selection Guide” for more details.

4.5.5. Unused Pins

Unused control pins (P0–P3) should be tied to GND.

Unused CLKIN pin should be tied to GND.

Unused XA/XB pins should be left floating. Refer to "2.2. Applying a Reference Clock at XTAL Input" on page 8 when using XA as a clock input pin.

Unused output pins (CLK0–CLK7) should be left unconnected.

4.5.6. Trace Characteristics

The Si5350C features various output drive strength settings. It is recommended to configure the trace characteristics as shown in Figure 10 when the default high output drive setting is used.

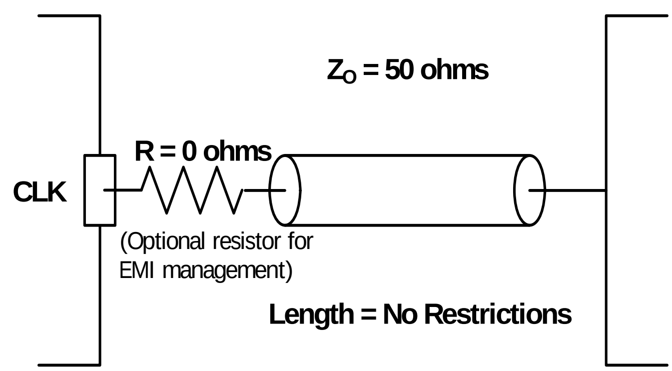

Figure 10. Recommended Trace Characteristics with Default Drive Strength Setting

Note: Jitter is only specified at default high drive strength.

5. Pin Descriptions

5.1. 20-pin QFN

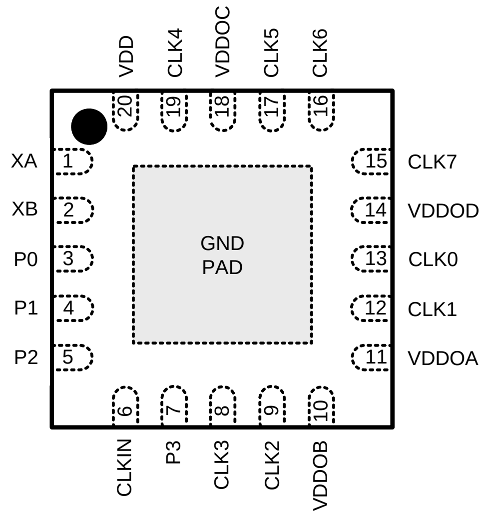

Figure 11. Si5350C 20-QFN Top View

Table 10. Si5350C 20-QFN Pin Descriptions

Pin Name	Pin Number	Pin Type	Function
XA	1	I	Input pin for external XTAL
XB	2	I	Input pin for external XTAL
CLKIN	6	I	External reference clock input
CLK0	13	O	Output clock 0
CLK1	12	O	Output clock 1
CLK2	9	O	Output clock 2
CLK3	8	O	Output clock 3
CLK4	19	O	Output clock 4
CLK5	17	O	Output clock 5
CLK6	16	O	Output clock 6
CLK7	15	O	Output clock 7
P0	3	I	User configurable input pin 0. See 4.5.5
P1	4	I	User configurable input pin 1. See 4.5.5
P2	5	I	User configurable input pin 2. See 4.5.5
P3	7	I	User configurable input pin 3. See 4.5.5
VDD	20	P	Core voltage supply pin. See 4.5.2
VDDOA	11	P	Output voltage supply pin for CLK0 and CLK1. See 4.5.2
VDDOB	10	P	Output voltage supply pin for CLK2 and CLK3. See 4.5.2
VDDOC	18	P	Output voltage supply pin for CLK4 and CLK5. See 4.5.2
VDDOD	14	P	Output voltage supply pin for CLK6 and CLK7. See 4.5.2
GND	Center Pad	P	Ground
Note: Pin Types: I = Input, O = Output, P = Power			

5.2. 10-pin MSOP

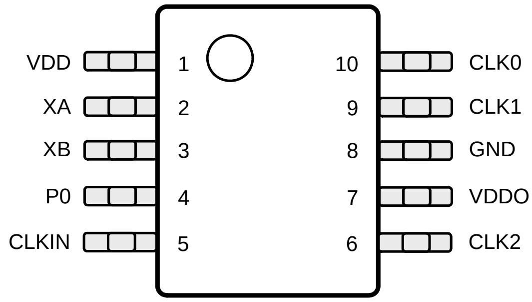

Figure 12. Si5350C 10-MSOP Top View

Table 11. Si5350C 10-MSOP Pin Descriptions

Pin Name	Pin Number	Pin Type	Function
XA	2	I	Input pin for external XTAL
XB	3	I	Input pin for external XTAL
CLKIN	5	I	External reference clock input
CLK0	10	O	Output clock 0
CLK1	9	O	Output clock 1
CLK2	6	O	Output clock 2
P0	4	I	User configurable input pin 0. See 4.5.5
VDD	1	P	Core voltage supply pin. See 4.5.2
VDDO	7	P	Output voltage supply pin for CLK0, CLK1, and CLK2. See 4.5.2
GND	8	P	Ground
Note: Pin Types: I = Input, O = Output, P = Power			

6. Ordering Information

Factory-programmed Si5350C devices can be requested using the ClockBuilder web-based utility available at: www.silabs.com/ClockBuilder. A unique part number is assigned to each custom configuration as indicated in Figure 13.

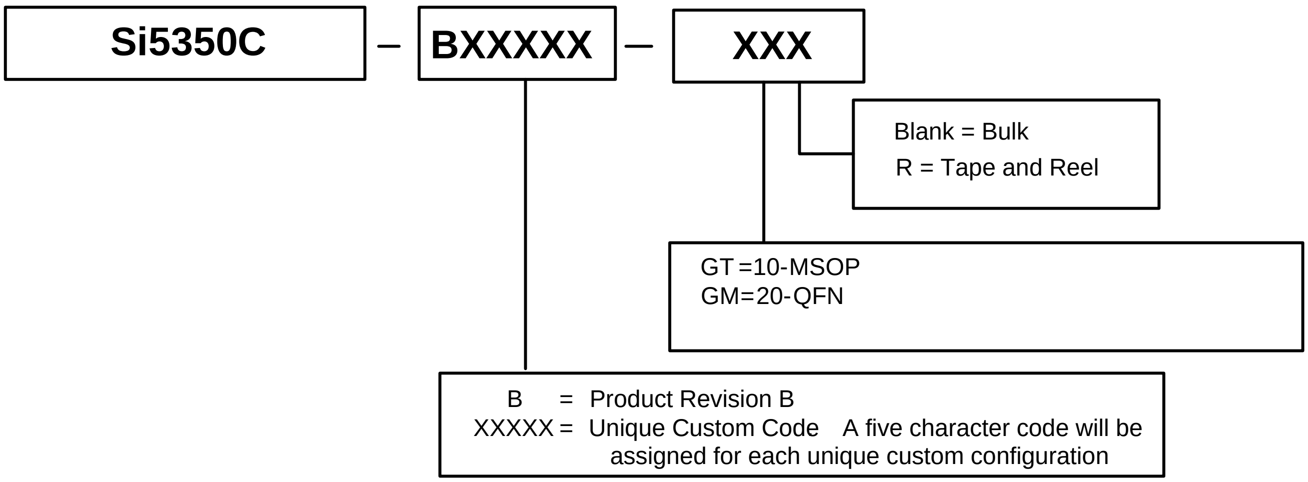

Figure 13. Custom Clock Part Numbers

7. Package Outline

7.1. 20-Pin QFN

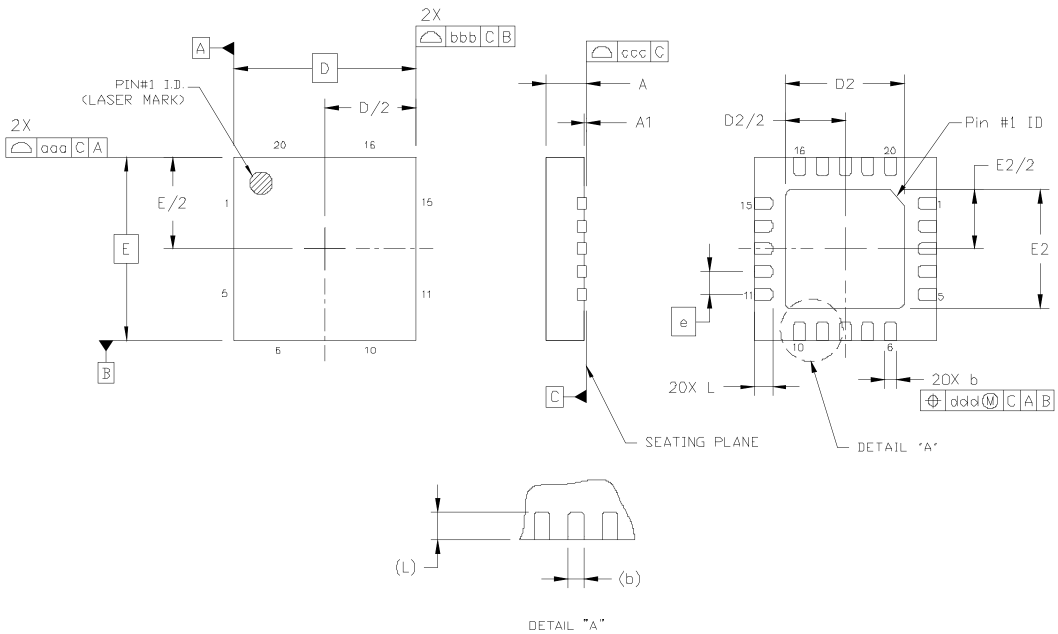

Figure 14. 20-pin QFN Package Drawing

Table 12. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.65	2.70	2.75
e		0.50 BSC	
E		4.00 BSC	
E2	2.65	2.70	2.75
L	0.30	0.40	0.50
aaa			0.10
bbb			0.10
ccc			0.08
ddd			0.10
eee			0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2. 10-Pin MSOP

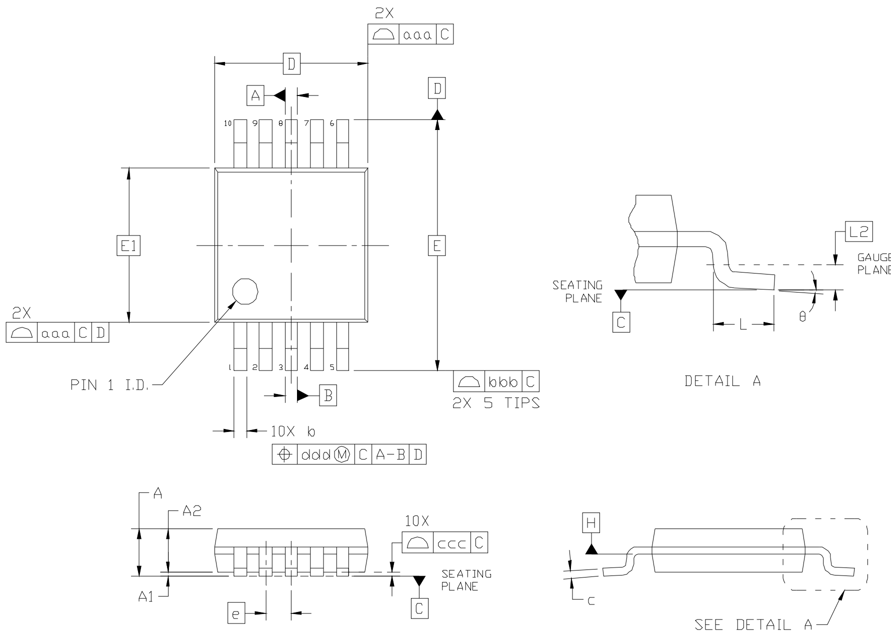

Figure 15. 10-pin MSOP Package Drawing

Table 13. 10-MSOP Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
b	0.17	—	0.33
c	0.08	—	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
L	0.40	0.60	0.80
L2	0.25 BSC		
q	0	—	8
aaa	—	—	0.20
bbb	—	—	0.25
ccc	—	—	0.10
ddd	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation C
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.75 to Revision 0.76

- Updated Table 3 on page 5.
  - Updated spread-spectrum frequency deviation parameter test condition and minimum spec value.
- Updated “6. Ordering Information” .
  - Updated Figure 13, “Custom Clock Part Numbers,” on page 18.

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