

853S314I

Low Skew 1-to-4 Differential to LVPECL Fanout Buffer

NOTICE - The following device(s) are recommended alternatives:

8T33FS314I - Low Skew, 1-to-4 Differential-to-2.5V, 3.3V LVPECL/ECL Fanout Buffer

Pin-to-pin compatible

The 853S314I is a low skew 1-to-4 Differential Fanout Buffer, designed with clock distribution in mind, accepting two clock sources into an input MUX. The MUX is controlled by a CLK_SEL pin. This makes the 853S314I very versatile, in that, it can operate as both a differential clock buffer as well as a signal-level translator and fanout buffer. The device is designed on a SiGe process and can operate at frequencies in excess of 2.7GHz. This ensures negligible jitter introduction to the timing budget which makes it an ideal choice for distributing high frequency, high precision clocks across back planes and boards in communication systems. Internal temperature compensation guarantees consistent performance across various platforms.

Features

- 4 differential ECL/LVPECL level outputs
- 1 differential ECL/LVPECL or single-ended input (CLKA)
- 1 differential HSTL or single-ended input (CLKB)
- Maximum output frequency: 2.7GHz
- Additive phase jitter, RMS: 0.138ps (typical) @ 156.25MHz,
- Output skew: 50ps (maximum)
- Part-to-part skew: 150ps (maximum)
- LVPECL and HSTL mode operating voltage supply range: VCC = 2.5V±5% or 3.3V±5%, VEE = 0V
- ECL mode operating voltage supply range: VEE = -3.3V±5% or -2.5V±5%, VCC = 0V
- -40°C to 85°C ambient operating temperature
- Available inlead-free RoHS (RoHS 6) package

Product Options

| Orderable Part ID | Part Status | Pkg. Code | Pkg. Type | Lead Count (#) | Temp. Grade | Pb (Lead) Free | Carrier Type | Buy Sample |
|-------------------|-------------|-----------|-----------|----------------|-------------|----------------|--------------|------------------------------|
| 853S314AFILFT | Obsolete | PYG20 | SSOP | 20 | I | Yes | Reel | Availability |
| 853S314AGILF | Obsolete | PGG20 | TSSOP | 20 | I | Yes | Tube | Availability |

Technical Documentation

| Title | Other Languages | Type | Format | File Size | Date |
|---|-----------------|------------------|--------|-----------|--------------|
| Application Notes & White Papers | | | | | |
| AN-828 Termination - LVPECL | - | Application Note | PDF | 229 KB | Jul 5, 2016 |
| AN-844 Termination - AC Coupling Clock Receivers | - | Application Note | PDF | 82 KB | May 12, 2014 |
| AN-842 Thermal Considerations in Package Design and Selection | - | Application Note | PDF | 403 KB | May 11, 2014 |
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PCNs & PDNs

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| PDN# : N-13-03R1 PRODUCT DISCONTINUANCE NOTICE | Product Discontinuation Notice | PDF | 72 KB | Jun 12, 2013 |
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| PCN# : TB1303-02 Change of E&P, New Product Method for Selective Locks | SOCIAL Product Change | CORPORATE |
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| Other | YOUR EMAIL@DOMAIN.COM | GO | INVESTORS |
| IDT Clock Distribution Overview | 日本語 | Overview | PDF 3.79 MB |
| IDT Fanout Buffers Product Overview | - | Product Brief | PDF 739 KB |
| High-Performance, Low-Phase Noise Clocks Buffers product brief | ©2018 Integrated Device Technology, Inc. | Product Brief | PDF 378 KB |
| | | | Aug 13, 2012 |

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