STM7710

Single-chip, low-cost HD set-top box decoder

Data Brief

Features

The STM7710 is a single-chip, high-definition MPEG decoder including:

- CPU core
- Transport filtering and descrambling
- Video decoder
- Graphics engine
- Dual display
- Audio decoder

The STM7710 also features the following embedded interfaces:

- USB 2.0 for hard-disk drive support
- DVI/HDMI (Digital Visual Interface and High-Definition Multimedia Interface™)
- Digital audio and video auxiliary input
- Low-cost modem solution

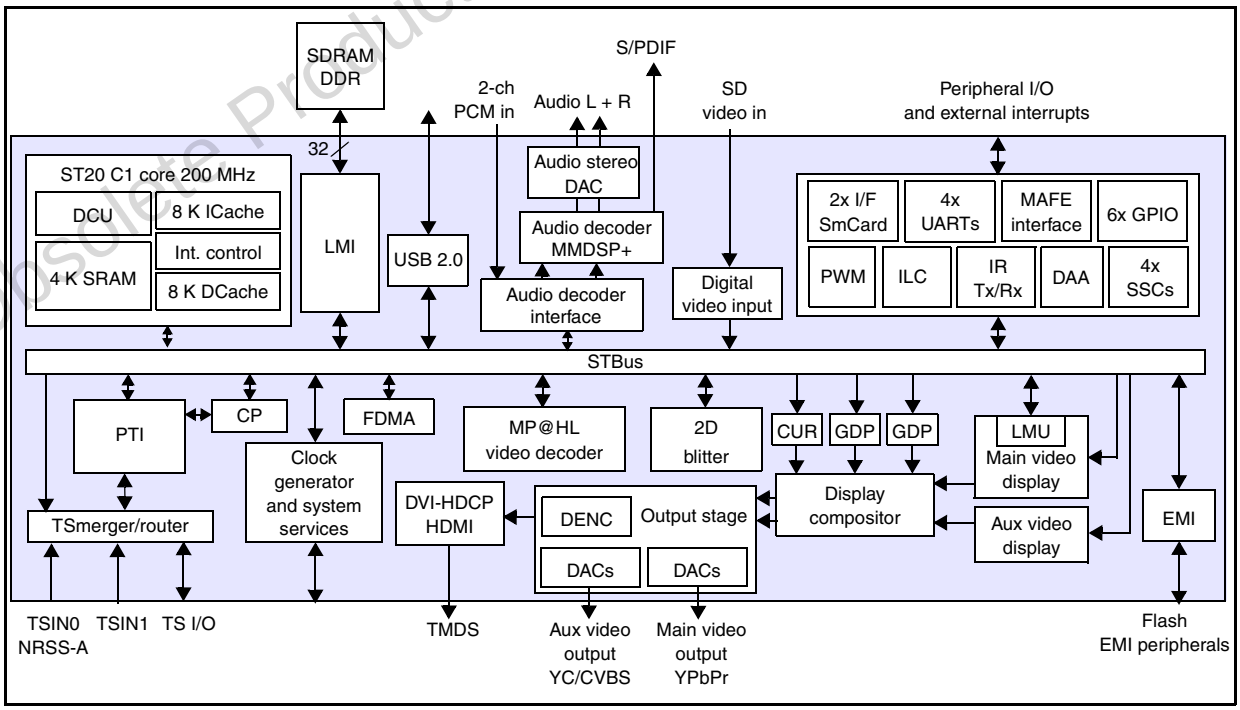
Subsystems and interfaces

These are detailed in *Section 1.1 on page 4*:

- Processor subsystem
- Transport stream subsystem
- Video/graphics subsystem
- Audio subsystem
- External memory interface
- Local memory interface
- USB 2.0 host interface
- Hard-disk drive support
- On-chip peripherals
- Flexible multichannel DMA

Support

- JTAG/TAP interface
- DCU toolset support



Contents

1 Introduction

The STM7710 is exactly the same as the STi7710. The STM7710 is a new generation of high-definition set-top box decoder chip, and provides very high performance for low-cost HD systems.

Based on the STBus architecture, this system on chip is a full back-end processing solution for digital terrestrial, satellite and cable high-definition set-top boxes compliant with ATSC, DVB, DIRECTV, DCII, OpenCable and ARIB BS4 specifications.

1.1 Subsystems and interfaces

Processor subsystem

- Enhanced ST20 32-bit VL RISC CPU
  - 200 MHz 8-Kbyte ICache, 8-Kbyte DCache, 4-Kbyte SRAM
  - diagnostic controller unit (DCU)
  - 16 level interrupt controller

Transport stream subsystem

- TS merger/router
  - 2 serial/parallel inputs
  - 1 bidirectional interface
  - merging of 3 transport streams
  - software transport stream support
  - NRSS-A module interface
- Programmable transport interface (PTI)
  - transport stream demux: DVB, DIRECTV, ATSC, OpenCable, DCII, BS4
  - integrated DES, DVB and Multi2 encryption descramblers

Video/graphics subsystem

- MPEG-2 MP@HL video decoder core
- SD (ITU-R BT 601/656) digital video input
- Displays
  - 1 HD display, multiformat capable (1080I, 720P, 480P, 480I)
    - analog HD output RGB or YPbPr
    - HDMI encoded output
  - 1 standard-definition analog display output: YPbPr, or YC and CVBS

- 2D/3D graphics processor
  - dual source blitter engine
  - alpha blending and logical operations
  - color space and format conversion
  - fast color fill
  - arbitrary resizing with high quality filters
  - acceleration of direct drawing by CPU
- Compositor and video processor
  - 5 channel mixer for high definition output
  - independent 2-channel mixer for SD output
  - 2 graphic display planes
  - hardware cursor
  - picture up-conversion hardware
  - linear/nonlinear resizing and format conversions
  - horizontal and vertical filtering
- Copy protection
  - HDMI / HDCP copy protection hardware
  - Macrovision™ copy protection for 480I and 480P output

Audio subsystem

- Digital audio decoder
  - MPEG-1 layer I/II, MPEG-2 layer II, MPEG-2 AAC and AC3 Dolby® Digital
  - SRS® TruSurround XT™,TruBass® and FOCUS™
  - PCM mixing with internal or external source and sample rate conversion
  - 6 to 2 channel downmixing
  - PCM audio input
- Stereo 24-bit audio DAC for analog output
- IEC958/IEC1937 digital audio output interface (S/PDIF)

Interfaces

- External memory interface
  - 16-bit interface supporting ROM, Flash, SFlash, SRAM
  - access in 5 banks
- Local memory interface
  - 32-bit DDR interface
- USB 2.0 host interface
- Hard-disk drive support
  - record and playback
  - pause and time shifting
  - watch and record
- On-chip peripherals
  - 4 ASCs (UARTs) with Tx and Rx FIFOS, 2 of which can be used in smartcard interfaces
  - 2 smartcard interfaces and clock generators (improved to reduce external circuitry)
  - 4 SSCs for I²C/SPI master slaves interfaces
  - 2 PWM outputs
  - teletext serializer and DMA module
  - 6 banks of general purpose I/O, 5 V tolerant
  - SiLabs line-side (DAA) interface
  - modem analog front end (MAFE) interface
  - infrared transmitter/receiver supporting RC5, RC6 and RECS80 codes
  - dual noise filters for IR inputs with programmable active levels
  - interrupt level controller and external interrupts, 5 V tolerant
  - low power / RTC / watchdog controller
  - integrated VCXO
  - UHF input interface
- Flexible multichannel DMA

Package

27 x 27 PGBA, 420 + 36 balls, 1 mm pitch

1.2 STM7710 applications

The STM7710 demultiplexes, decrypts and decodes a single HD or SD video stream with associated multichannel audio. Video is output to two independently formatted displays: a full resolution display intended for a TV monitor and a downsampled display intended for a VCR. A TV or display panel can be connected through an analog component interface or a copy protected DVI/HDMI interface. Composite outputs are provided for connection to the VCR with Macrovision protection. Audio is output with optional PCM mixing to an S/PDIF interface or through integrated stereo audio DACs.

Digitized NTSC or PAL programs can also be input to the STM7710 for reformatting and display.

The STM7710 includes a graphics rendering and display capability with a 2D-graphics accelerator, two graphics planes and a cursor plane. A dual display compositor provides mixing of graphics and video with independent composition for each of the TV and VCR outputs.

The STM7710 includes a stream merger to allow three different transport streams from different sources to be merged and processed concurrently. Applications include DVR time shifted viewing of a terrestrial program while acquiring an EPG/data stream from a satellite or cable front end.

The flexible descrambling engine is compatible with required standards including DVB, DES and Multi2.

The STM7710 has an embedded 200 MHz ST20 CPU for applications and device control and allows a unified memory architecture by providing a high bandwidth DDR DRAM interface. A second memory bus is also provided for Flash memory to store resident software and connect peripherals.

An external hard-disk drive (HDD) can be connected either to the EMI or as an expansion drive through the USB 2.0 port.

The STM7710 is supported by STMicroelectronics' STAPI software, and provides a compatible next-generation architecture for applications currently running on the STi5517 and STi7020.

Figure 1. Low-cost satellite HD set-top box

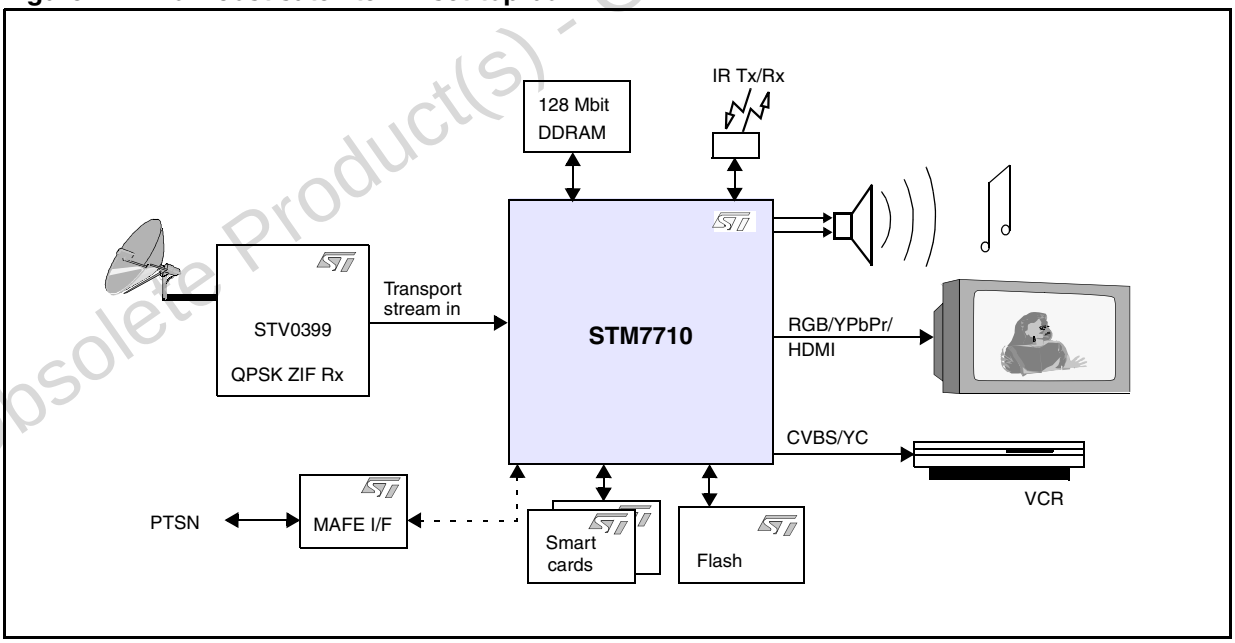


Figure 2. Low-cost cable HD set-top box

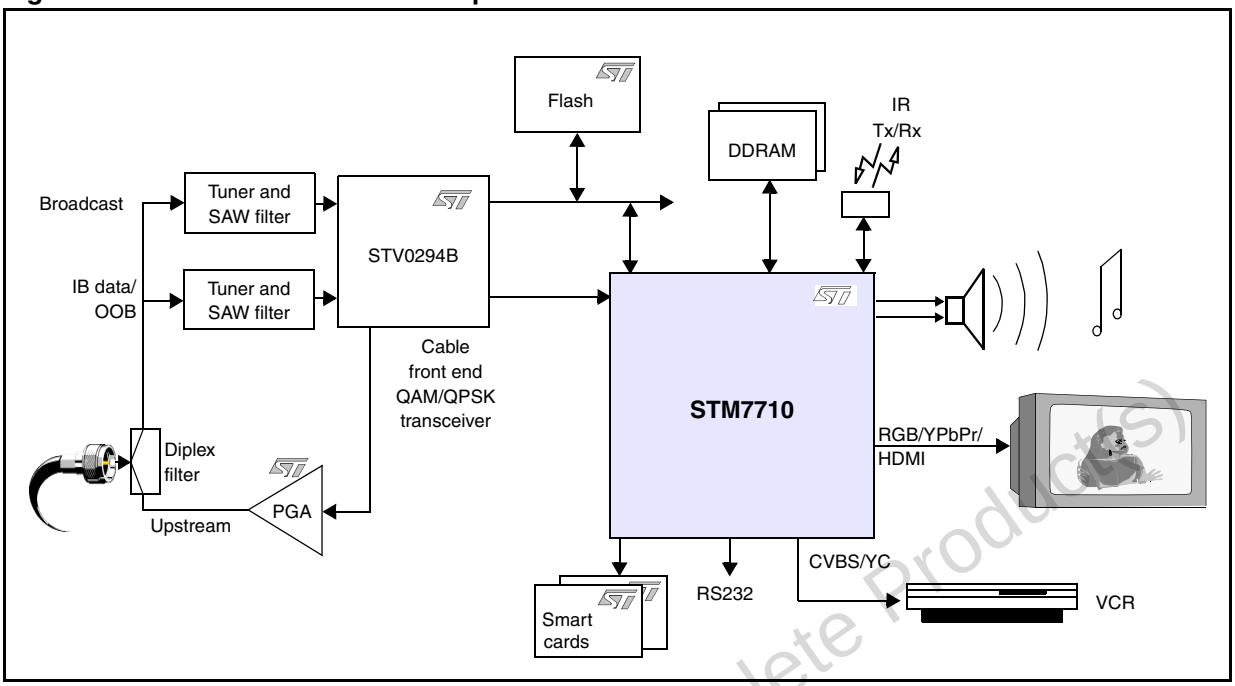
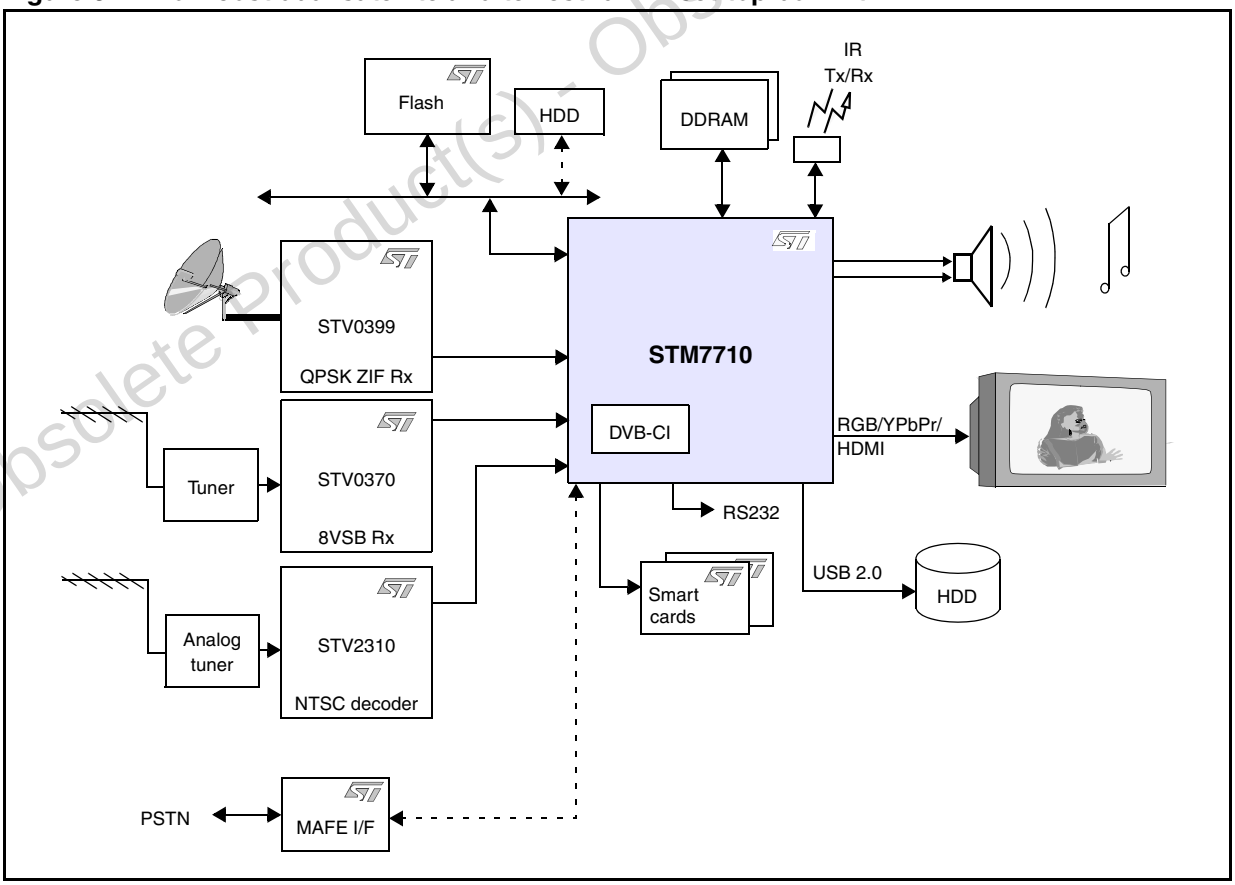


Figure 3. Low-cost dual satellite and terrestrial HD set-top box with HDD



2 Architecture

2.1 Architecture overview

The STM7710 is designed around the well-proven STBus interconnect.

Transport streams are received and processed by the TS subsystem. The resulting PES streams and section data are stored in memory buffers in DDR SDRAM attached to the local memory interface (LMI).

A flexible DMA controller (FDMA) performs PES parsing and start code detection. It routes elementary streams to audio and video bit buffers in DDR SDRAM. An MP@HL video decoder decodes HD or SD video streams. Audio decoding and PCM mixing is performed by the MMDSP and output through S/PDIF or integrated 24-bit stereo DACs.

After video decoding, two independently formatted video displays (main and auxiliary) can be generated, and each mixed independently with graphics to create main and auxiliary display compositions. The main display composition (HD or SD) can be output as RGB or YPbPr analog component video and digitally through a copy-protected DVI/HDMI interface. The auxiliary display composition (SD only) can be output as a YPbPr analog component or as composite video on a separate interface for connection to a VCR.

A digital video input interface allows the STM7710 to receive SD uncompressed digital video and to output this to the main and auxiliary displays in place of decoded video. A separate PCM input allows any associated audio to be received, mixed and output in place of decoded audio.

The graphics subsystem comprises a separate 2D-blitter, two graphics planes, a cursor plane and dual display compositor. Graphics buffers are created, stored in and displayed from buffers in DDR SDRAM.

The STM7710 embeds an ST20-C1 CPU core for applications and data processing and device control. The CPU boots from Flash/SFlash on the external memory interface (EMI) and can execute in place or transfer the main executable to the DDR SDRAM and execute from there. CPU data is held in DDR SDRAM where cacheable and noncacheable regions can be programmed. The 16-bit EMI is also used for connecting to external peripherals.

System performance is enhanced with the multichannel FDMA which can be used for 2D block move and stream data transfers with minimal CPU intervention.

DVR applications are supported using a hard-disk drive (HDD) connected either to the EMI or to the USB 2.0 HDD interface.

The STM7710 also integrates a range of peripherals, system services and a clock generator module with embedded VCXO (programmable frequency synthesizers able to replace the classical external VCXO) to significantly reduce external component cost.

2.2 Processor core

The STM7710 integrates a 200 MHz ST20-C105 processor core composed of the ST20C1+ CPU, a diagnostic controller unit (for low intrusion, real-time debugging), memory (8 Kbyte instruction cache, 8 Kbyte data cache and 4 Kbyte SRAM) and a 16 priority-level interrupt controller.

2.3 External memory interface (EMI)

The EMI is a 16-bit general-purpose interface for attaching system Flash or synchronous Flash devices and peripherals. Up to 5 separate banks are available, each capable of its own strobe timing configuration and each with its own chip select signal. Two banks provide PC-Card compatible strobes for implementing a DVB-CI or CableCard (POD) module interface.

2.4 Local memory interface (LMI)

The LMI is a 32-bit, high-bandwidth memory interface that enables a unified data memory architecture through the use of DDR SDRAM. CPU instructions can also be placed here. It can operate in a 16-bit or 32-bit configuration and has a target operating frequency of 200 MHz for a peak bandwidth of 1.6 Gbyte/s. In a 32-bit configuration, the LMI supports one x32 device or two x16 devices. 64-Mbit, 128-Mbit or 256-Mbit DDR devices can be used providing a maximum capacity of 64 Mbytes.

To get the maximum transfer efficiency from the interface, the LMI includes optimizations in the control of the page structure of DDR DRAMs.

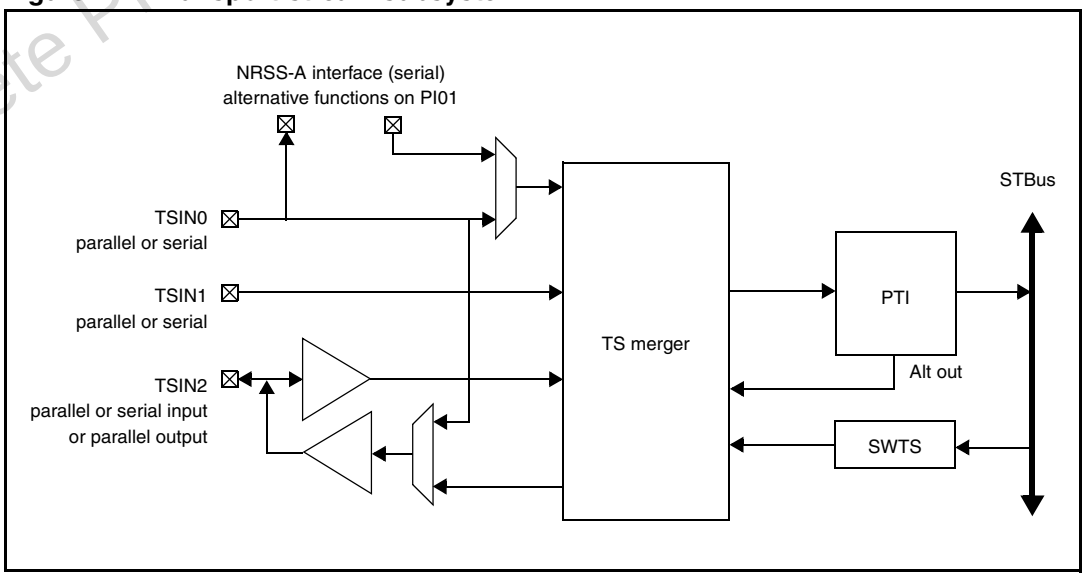
2.5 Transport subsystem

The transport stream subsystem comprises the TS merger/router and a programmable transport stream interface (PTI).

2.5.1 Transport stream input/output

Transport streams are input to the STM7710 through one of three interfaces. Two of these are parallel inputs which can also be configured for serial input if required. The third is a bidirectional parallel interface that can be configured as an input or output.

Figure 4. Transport-stream subsystem



A five input, two output transport stream merger/router allows any of the three external inputs to be routed to the PTI. A fourth input is provided for routing internal transport streams stored in memory to the PTI. A fifth input receives a full/partial transport stream created by the PTI and can output it from the STM7710 through the bidirectional interface when configured as an output. This allows transport streams to be sent to a D-VCR through an IEEE1394 link layer controller, EMI or USB 2.0 port. Routing can be concurrent to two outputs.

When TS0 is operating in serial mode, an NRSS-A interface is available for routing serial transport streams to and from an NRSS-A compatible CA module.

The stream merger/router is also capable of merging any three of the input streams into one transport stream and forwarding this to the PTI allowing the PTI to process three independently sourced transport streams at the same time.

2.5.2 Programmable transport interface (PTI)

The PTI performs PID filtering, demultiplexing, descrambling, and data filtering on up to three transport streams at the same time up to an aggregate rate of 100 Mbit/s. The PTI extracts PCRs with time stamps and makes them available to the CPU for clock recovery and audio/video synchronization.

PES data is transferred by DMA to memory buffers. Section data is transferred by DMA to separate buffers for further processing by the CPU. The PTI can also extract indexing information and then transfer packets, using DMA, to an intermediate buffer for writing to HDD.

Transport streams supported include DIRECTV®, DVB, ATSC, OpenCable, DCII and ARIB BS4.

The PTI performs PID filtering to select audio, video and data packets to be processed. Up to 48 PID slots are supported.

The PTI can descramble streams using the following ciphers:

- DES-ECB including DVS-042 termination block handling,
- DES-CBC including DVS-042 termination block handling,
- DES-OFB,
- Multi2-ECB including DVS-042 termination block handling,
- Multi2-CBC including DVS-042 termination block handling,
- Multi2-OFB,
- DVB-CSA,
- Fast-I,
- NDS specific streams can also be supported by the integration of ICAM functionality.

The PTI has a 48 x 16-byte section filter core. Four filtering modes are available:

- Wide match mode: 48 x 16-byte filters,
- Long match mode: 96 x 8-byte filters,
- Positive/negative mode: 48 x 8-byte filters with positive/negative filtering at the bit level.

Matching sections are transferred to memory buffers for processing by software.

When the PTI is required to output a transport stream, it can output the entire transport stream or selected packets filtered by PID. A latency counter is provided to ensure packet timing is preserved. Packets can also be substituted.

2.6 MPEG-2 video decoder

The STM7710's video decoder is a single-stream decoder for either SD or HD streams. The decoder is fully compliant with ISO/IEC13818-2 MP@ML and MP@HL formats.

A stream is decoded picture by picture from an elementary stream buffer. Decoding, reconstruction and prediction buffers are set up by the CPU. CPU control of bit buffer pointers provides flexibility for trick modes and out-of-sequence decoding.

Semantic or syntax errors are detected by the decoder and failing macroblocks are replaced up to the next slice or picture.

Pictures can be reconstructed with decimation for VCR recording to reduce memory bandwidth while keeping full resolution pictures for anchor frames and main display.

2.7 Digital video input

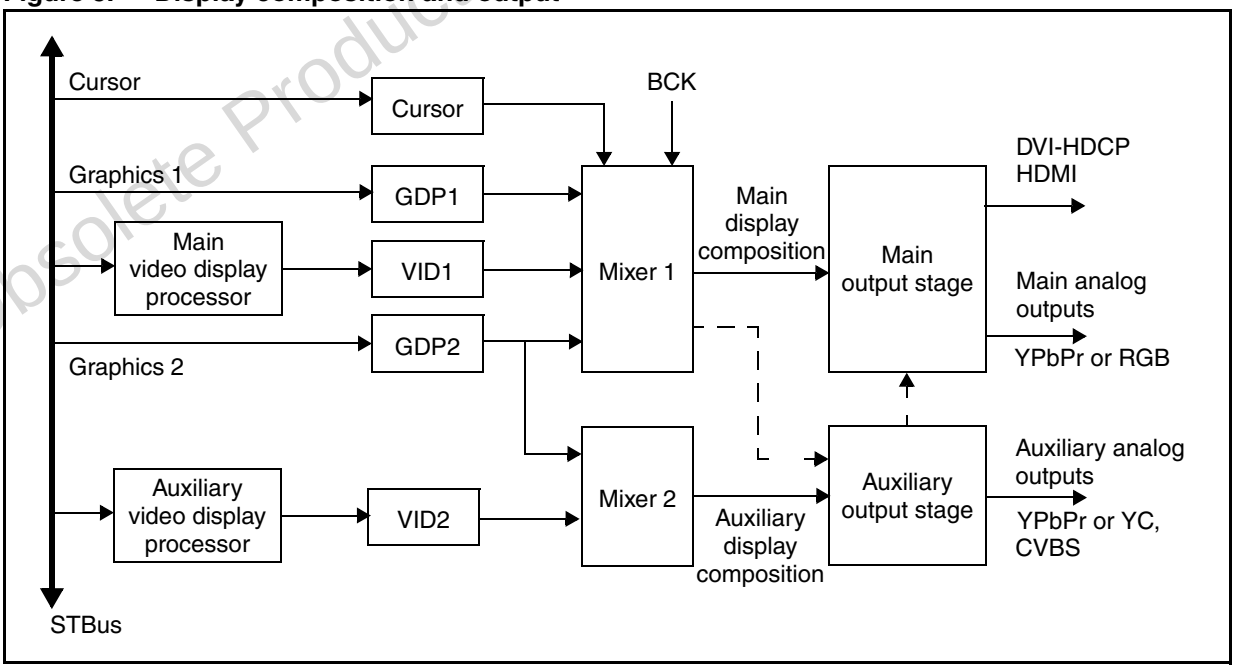
Digital SD video data can be input to the STM7710 through an 8-bit digital video input port.

The 8-bit mode is intended for inputting SD video data conforming to ITU-R BT656 with embedded syncs or ITU-R BT601 with external syncs. In ITU-R BT656 mode, auxiliary data embedded in the stream can be extracted to a separate buffer.

2.8 Video display processors

The STM7710 displays video using the main and auxiliary display processors (*Figure 5*). The video may have been decoded and reconstructed by the MPEG decoder or acquired through the digital video interface.

Figure 5. Display composition and output



The same video appears on both displays but each can be set up to format the video differently and display with different timing. Separate video timing generators (VTGs) are provided to support this.

The display processors are used to present the video from the display buffers and adapt the decoded video format to a format suitable for display taking into account differences in scanning method, resolution, aspect ratio and scanning frequency.

The main-display processor receives decoded or acquired video from memory and performs block-to-line conversion, pan and scan, and vertical and horizontal format conversion. There is also a linear median upconverter (LMU) to perform interlace-to-progressive conversion on standard definition pictures using motion estimation.

The auxiliary-display processor receives decoded or acquired (and possibly decimated) video and performs pan and scan, vertical format conversion, horizontal format conversion. The output line size is limited to 720 pixels on the auxiliary-display processor and is intended to output video for VCR recording.

2.9 Graphics display

2.9.1 Graphics layers

The STM7710 has two independent and identical graphics layers known as generic display pipelines (GDPs) (see *Figure 5*). Each GDP receives pixel data from memory and features the following.

- Link-list-based display engine, for multiple viewport capabilities.
- Support for ARGBargb formats, including:
  - ARGB1555,
  - ARGB4444,
  - RGB565,
  - RGB888,
  - ARGB8565,
  - ARGB8888.
- Support for YCbCr4:2:2R, YCbCr888 formats.
- Support for premultiplied or non-premultiplied RGB components.
- Color space conversion matrix, (YCbCr 601/709, chroma signed/unsigned to RGB).
- Gain and offset adjustment.
- Per-pixel alpha channel combined with per-viewport global alpha.
- 5-tap horizontal sample rate converter for horizontal upscaling only, not downscaling. Vertical resize is not possible. The horizontal sample rate converter can be used to adapt the pixel aspect ratio. The resolution is 1/8th pixel (polyphase filter with eight subpositions).
- Color keying capability.

2.9.2 Cursor layer

The cursor is defined as a 128 x 128 pixel area held in local memory, in ACLUT8 format. Each cursor entry is a 16-bit ARGB4444 color + alpha value. The alpha factor of four bits handles an antialiased cursor pattern on top of the composed output picture. The cursor-plane features are:

- ACLUT8 format, with ARGB4444 CLUT entries. 256 colors can be simultaneously displayed for the cursor pattern, among 4096 colors associated with a 16-level translucency channel.
- Size is programmable up to 128 x 128.
- Hardware rectangular clipping window, out of which the cursor is never displayed (per-pixel clipping, so only part of the cursor can be out of this window, therefore transparent).
- Current bitmap is specified using a pointer register to an external memory location, making cursor animation easy.
- Programmable pitch, so all cursor patterns can be stored in a single global bitmap.

2.10 Display compositor

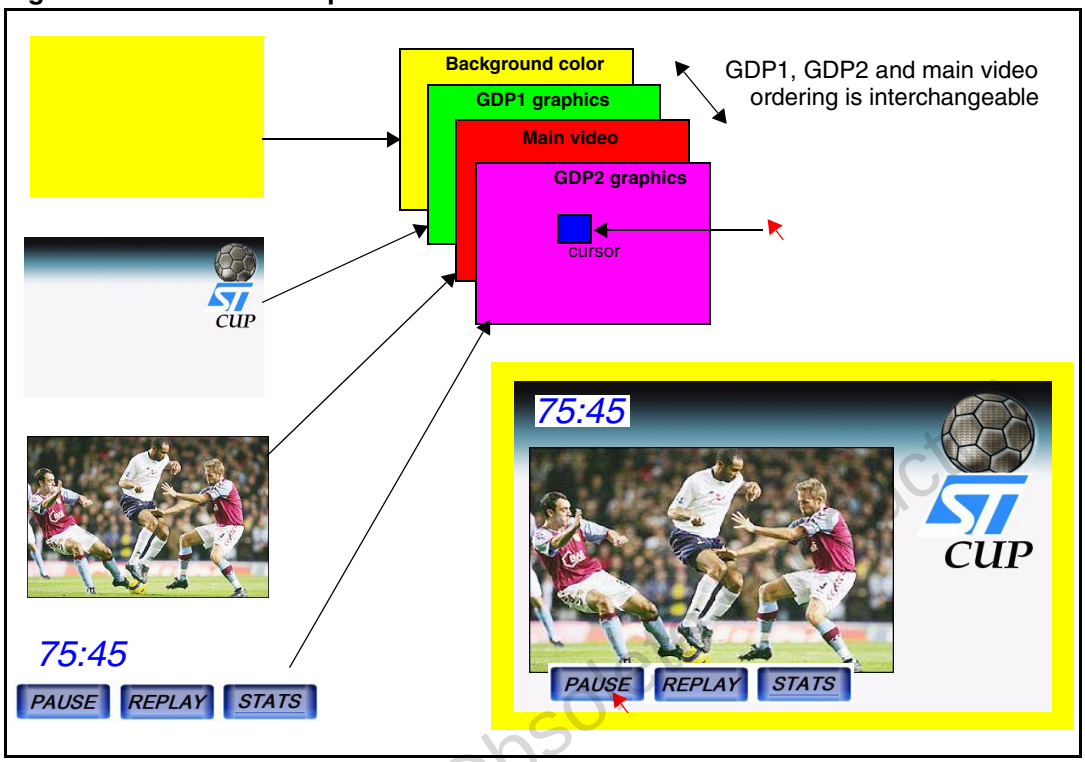
The graphic compositor consists of a five-layer digital mixer (Mix1) intended for the main TV display (*Figure 6*) and a two-layer digital mixer (Mix2) intended as an auxiliary display for applications including connection to a VCR (*Figure 7*).

Each mixer alpha blends graphics and video layers on a pixel-by-pixel basis based on alpha component values provided by each layer.

The Mix1 display planes are:

- A background color (RGB888 format, programmable through the registers),
- The two graphics layers GDP1 and GDP2,
- The main video display,
- The cursor plane.

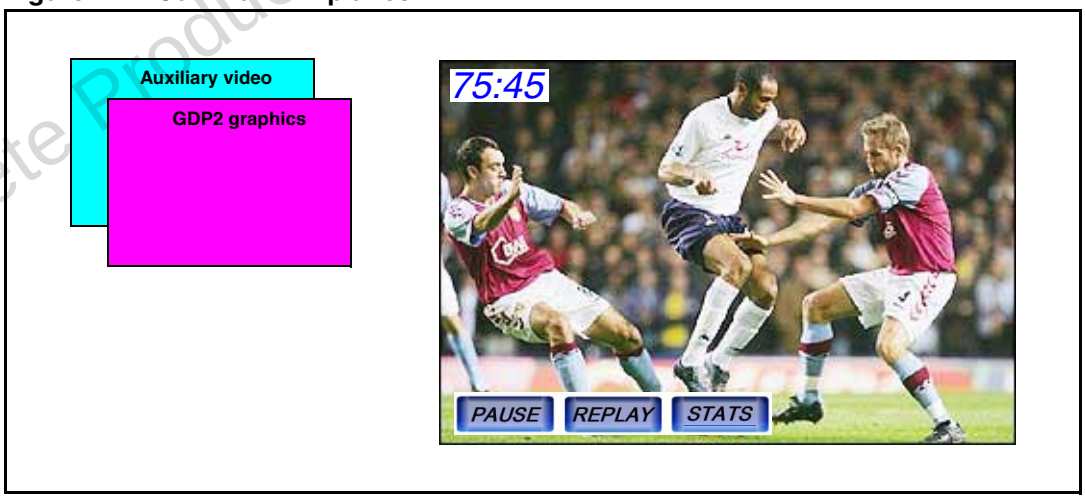
Figure 6. Gamma Mix1 planes



The Mix2 display planes are:

- The auxiliary video display,
- The graphics layer GDP2.

Figure 7. Gamma Mix2 planes



2.11 Main display output stage

The display composition from MIX1 can be output on any of the main display output interfaces (*Figure 5*). These are:

- the main analog output,
- the DVI/HDMI output.

The main analog output interface supports YPbPr or RGB analog output with or without embedded syncs. High current HD DACs are used to minimize external component count.

Programming flexibility is provided to support different display timings and resolutions. These include support for:

- SMPTE,
- BS4 SD and HD formats,
- standard formats supported:
  - 480i (full scanning 525i) / 576i (full scanning 625i),
  - 480p (full scanning 525p) / 576p (full scanning 625p),
  - 720p (full scanning 750p),
  - 1080i (full scanning 1125i),
- panel displays with a pixel clock up to 74.25 MHz.

Timings and levels can be programmed to comply with EIA770.x (x = 1, 2, 3) requirements.

The main analog output can also have Macrovision™ encoding for 480i and 480p and CGMS encoding.

The HDMI output provides DVI-HDCP or HDMI compliant copy protected digital output of the main display composition.

2.12 Auxiliary display output stage

The display composition from MIX2 is output on the auxiliary display output interface (*Figure 5*).

This interface uses a digital encoder that encodes the output from the auxiliary mixer into a standard analog baseband PAL/NTSC signal and into YPbPr components.

The digital encoder performs closed-caption, CGMS, WSS, teletext and VPS encoding and allows Macrovision 7.01/ 6.1 copy protection.

An integrated tri-DAC provides three analog TV outputs, on which it is possible to output either (S-VHS(Y/C) + CVBS), YPbPr or RGB.

2.13 2D blitter

The 2D-graphics processor (also called the blitter engine) is a CPU-independent engine for graphics picture processing. It functions as a dual-source 2D DMA, with a set of powerful operators.

The 2D-graphics processor receives data from local memory through two input sources: source 1 and source 2. Source 1 is used for frequent operations such as color-fill or simple source-copy; it has a 64-bit wide internal bus and performs according to the pixel format. All operators always apply to source 2. The processing pipeline bus is always a pixel bus (ARGB8888 format) whatever the format of the source inputs. Sources 1 and 2 are used simultaneously for read/modify/write operations.

The 2D-graphics processor is software controlled by a link-list mechanism. Each node of the link list is an instruction that contains all the necessary information to proceed.

The STM7710 blitter features:

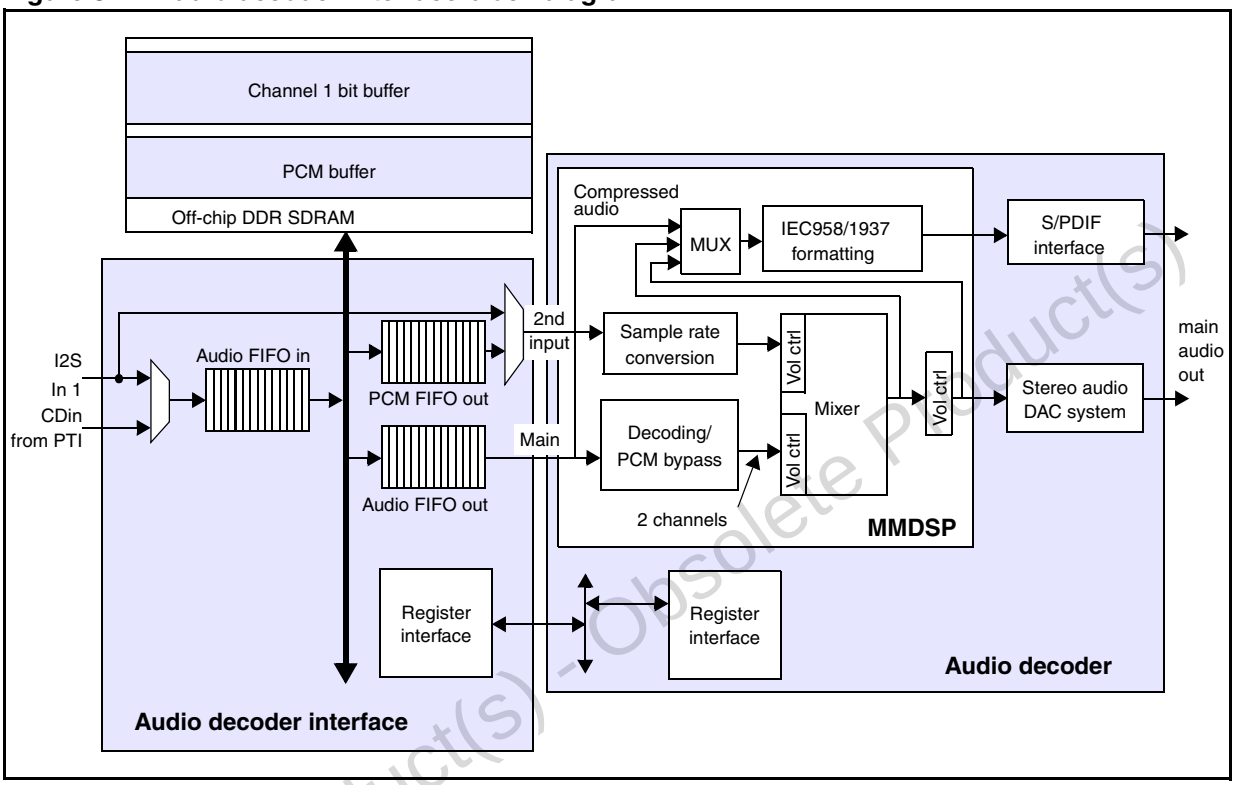
- solid color fill of rectangular windows,
- solid color shade (fill + alpha blending),
- one source copy, with one or several operators enabled (color format conversion, 2D scaling),
- two-source copy with alpha blending or logical operation between them,
- 4:2:2 raster/macroblock and 4:2:0 macroblock as source formats, 4:2:2 raster as a destination format,
- color space conversion RGB to and from YCbCr.
- color expansion (CLUT to true color),
- color correction (gamma, contrast, gain),
- color reduction (true color to ACLUTn) using an error diffusion algorithm,
- 2D resize engine with high-quality filtering,
- adaptive flicker filter from memory to memory,
- color keying capability,
- rectangular clipping,
- programmable source/target scanning direction, both horizontally and vertically, to cope correctly with overlapping source and destination areas,
- 1-bit/8-bit clipmask bitmap for random shape clipping can be achieved in two passes.
- plane mask feature available,
- special XYLC access mode, for speeding random pixel access, or horizontal line drawing (polygon filling, run-length decoder accelerator).

Source and destination windows can all be defined using an XY descriptor, with pixel accuracy whatever the format, from 1 to 32 bpp. Most of these operators can be combined in a single blitter pass: for example, convert a YCbCr 4:2:2 bitmap to 4:4:4 RGB, resize it and blend it on an RGB565 background picture.

2.14 Audio subsystem

The audio subsystem comprises the audio controller, the MMDSP 24-bit audio digital signal processor and the audio output interfaces. The audio subsystem is shown in *Figure 8*.

Figure 8. Audio decoder interface block diagram



2.14.1 Audio decoder interface

The audio decoder interface receives, buffers and reformats audio data. It handles up to three audio data flows concurrently.

- It receives a raw PCM stream from an external source through the PCM input interface or receives a compressed data stream from an internal source such as the PTI and stores this in a memory buffer through DMA. This is used to buffer and play the main audio for the digital or analog program.
- It receives a PCM file or stream from a memory buffer through DMA and delivers this to the MMDSP's 2nd input for sample rate conversion and mixing with the main audio. The second input may also receive a PCM stream directly from the PCM input interface. This is used to play PCM data which is mixed with the main audio.

2.14.2 Audio decoder

The audio decoder receives the compressed audio (PES or ES) or PCM audio stream on its main input. For compressed data it performs PES parsing, PTS extraction, multichannel decoding and downmixing. At the same time, it formats the multichannel compressed data stream for output over the S/PDIF interface for external decoding. Decoded multichannel audio is downmixed before emerging as downmixed stereo or Dolby Pro Logic® encoded audio. True Surround XT® post processing can be applied. PCM audio is passed straight through.

Decoding of MPEG-1 layers I, II, Dolby® Digital and AAC stereo are supported at sample rates of 32 kHz, 44.1 kHz and 48 kHz.

The decoded/downmixed channels can be mixed with PCM files from the 2nd input which the audio decoder has sample rate converted.

The audio decoder can generate programmable tones for dish alignment.

The audio decoder generates the following:

- Main 2-channel output: the left and right decoded/downmixed channels (L/Lt, R/Rt) with PCM file mixing.
- S/PDIF output: a digital audio stream selected from one of the following:
  - IEC61937 formatted compressed audio received on the audio decoder's main input,
  - IEC60958 formatted version of the main 2-channel output.

2.14.3 Audio output interfaces

The audio output interfaces from the STM7710 are:

- S/PDIF interface. This outputs the S/PDIF output from the audio decoder.
- Analog stereo output from integrated 24-bit DACs. This outputs the main 2-channel output from the audio decoder.

2.15 FDMA controller

The STM7710 has a multichannel, burst-capable direct memory access controller that supports the following.

- Fast 2D unaligned memory to memory transfers of graphics and stills.
- Real-time stream transfers to and from memory with or without pacing. These channels are suitable for transfers with internal or external peripherals and for audio and video stream transfers within the STM7710.
- Two external pacing signals for paced transfers to and from external peripherals.

2.16 Interfaces

2.16.1 USB

The STM7710 has an integrated USB host controller with one host port. The USB host interface is partially compliant with OHCI/EHCI rev 1.0 and USB rev 2.0, allowing connection to a hard-disk drive only. All speeds up to 480 Mbit/s are supported.

2.16.2 Modem

Standard solutions are available for V22bis software modems and V34/V90 controllerless modems ported to the STM7710 architecture.

An integrated interface to the SiLabs DAA allows a two-wire capacitively coupled connection to the line-side device (no transformer required).

A modem analog front-end (MAFE) interface allows direct connection to an external codec to support this software modem capability. The MAFE interface has its own two-channel DMA controller for sample transfers to and from buffers.

2.16.3 Internal peripherals

The STM7710 has many dedicated internal peripherals for digital TV receiver applications, including:

- 2 smartcard controllers,
- 4 ASCs (UARTs), two of which are generally used by the smartcard controllers,
- Teletext serializer and DMA,
- 4 SSCs for I^2C/SPI master/slave interfaces,
- 6 GPIO ports (5V tolerant),
- 2 PWM modules:
  - the first (“PWM4”, also used as ST20-C1 time slicer), usable as timer or to control one PWM output,
  - a second, dual module (“PWM-Timer2”) with each channel usable as a timer or to control a PWM output,
- a multi-channel, infrared blaster/decoder interface module,
- an interrupt level controller with 4 external interrupt inputs (5 V tolerant).

2.16.4 Smartcard interfaces

Both STM7710 smartcard interfaces are ISO7816, EMV2000 and NDS compliant by adding a simple external power switch.

A programmable hardware power control feature allows the power control signal to be switched when a card’s insertion or removal is detected.

2.17 Clock generation

All system clocks are generated on chip using the clock generator module.

VCXO functionality has been integrated using a special purpose frequency synthesizer, removing the need for an external varactor diode or VCXO module. However support for an external VCXO module is also available.

A bank of digital frequency synthesizers is also provided for specific precise clock generation purposes, including generation of a low jitter PCM audio clock, a smartcard clock, and an external auxiliary clock.

2.18 System services

The STM7710 supports several on chip system service functions including:

- Reset control,
- Watchdog control and reset out,
- Low-power control with wake up from internal timer or external interrupt or IR blaster,
- Real-time clock,
- JTAG boundary scan,
- Diagnostic control / support for DCU toolset.

3 ECOPACK packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Revision history

Table 1. Document revision history

Date	Revision	Changes
25-Aug-2006	2	Replaced STi7710 with STM7710 *Chapter 1: Introduction on page 4*: Added “The STM7710 is exactly the same as the STi7710.”
10-Aug-2006	1	Initial release.

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