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PI2126
Cool-ORing® Series

30 Volt, 12 Amp Full-Function Active ORing Solution

Description

The ***Cool-ORing®*** PI2126 is a complete full-function Active ORing solution with a high-speed ORing MOSFET controller and a very low on-state resistance MOSFET designed for use in 12V Bus redundant power system architectures. The PI2126 *Cool-ORing* solution is offered in an extremely small, thermally enhanced 5mm x 7mm LGA package and can be used in high side Active ORing applications. The PI2126 enables extremely low power loss with fast dynamic response to fault conditions, critical for high availability systems.

The PI2126, with its 4.5mΩ internal MOSFET provides very high efficiency and low power loss during steady state operation. The PI2126 monitors the current direction in the MOSFET and will respond very fast to a reverse current due to input power source fault condition to prevent undesired high current build-up in the system. The PI2126 provides an active low fault flag output to the system during reverse current, excessive forward over-current and UVLO fault conditions.

Features

- Integrated High Performance 12A, 4.5mΩ MOSFET
- Very small, high density fully-optimized solution with simple PCB layout
- Fast dynamic response to power source failures, with 90ns reverse current turn-off delay time
- Accurate sensing capability to indicate system fault conditions (-6mV reverse threshold)
- Internal charge pump
- Fault Status output

Applications

- N+1 Redundant Power Systems
- Servers & High End Computing
- Telecom Systems
- High-side Active ORing

Package Information

The PI2126 is offered in the following package:

- 25-pin 5mm x 7mm thermally enhanced LGA package, achieving <11°C/W $R_{\theta J\text{-}PCB}$

Typical Application:

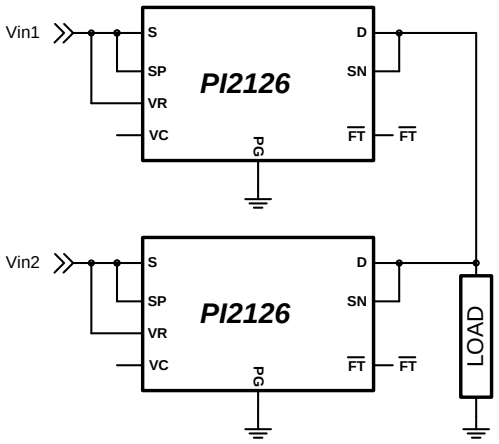

Figure 1: PI2126 High Side Active ORing

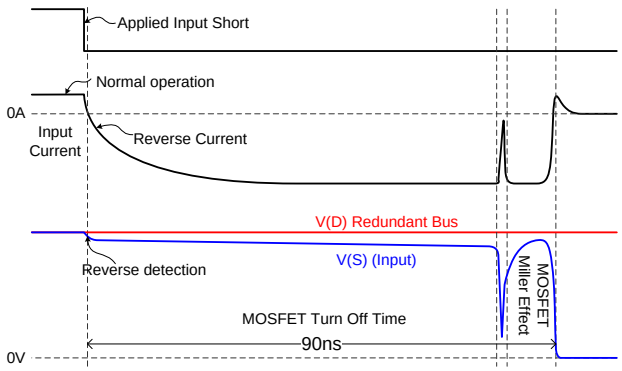

Figure 2: PI2126 response time to an input short fault condition

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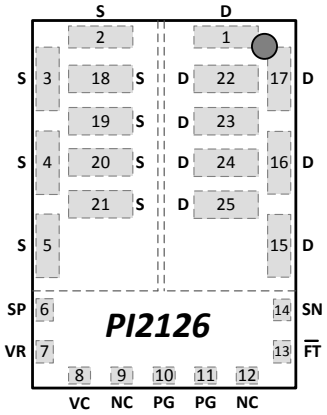
Pin Description

Pin Name	Pin Number	Description
D	1, 15, 16 17, 22, 23, 24, 25	**Drain:** The Drain of the internal N-channel MOSFET. Connect this pin to the output load.
S	2, 3, 4, 5, 18, 19, 20, 21	**Source:** The source of the internal N-channel MOSFET. Connect this pin to the input power source bus voltage.
SP	6	**Positive Sense Input & Clamp:** Connect SP pin to the trace between S pin and the input source (outside of the PI2126 foot print). The polarity of the voltage difference between SP and SN provides an indication of current direction through the MOSFET.
VR	7	**Controller Input Supply With Limiting Resistor:** This pin is connected internally to VC through a 420Ω resistor added for Bus voltages greater than 10V and less than 14V.
VC	8	**Controller Input Supply:** This pin is the supply pin for the control circuitry and gate driver. Voltage on this pin is regulated to 11.7V with respect to PG pin by an internal shunt regulator.
NC	9, 12	**Not Connected:** Leave these pins unconnected.
PG	10, 11	**Control Circuitry Return:** These pins are ground return for the gate driver and control circuitry. In 12V applications connect these pins to ground.
$\overline{FT}$	13	**Fault Status Output:** This open collector pin pulls low after a delay when a reverse fault or a forward fault occurs. When the input voltage to the control circuitry is in under voltage, V_{VC-PG} < 7V this pin pulls low. When V_{VC-PG} > 7.15V and 6mV < SP-SN < 275mV this pin clears (High). Leave this pin unconnected if unused.
SN	14	**Negative Sense Input:** Connect SN pin to the trace between D pin and the output load (outside of the PI2126 foot print). The polarity of the voltage difference between SP and SN provides an indication of current direction through the MOSFET.

Package Pin-Out



25-pin LGA (5mm x 7mm)
Top view

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Absolute Maximum Ratings

Note: All voltage nodes are referenced to PG

Drain-to-Source Voltage (V_{DS})	30V @ 25°C
Source Current (Is) Continuous	12A
Source Current (Is) Pulsed (10µs) (1)	60A
Single Pulse Avalanche Current (T_{AV}<40µs) (1)	60A
Source (S), SP, $\overline{FT}$	-0.3V to 17.3V / 10mA
SN	-0.3V to 40V / 4mA
Thermal Resistance $R_{\theta JA}$ (3)	46°C/W
Thermal Resistance $R_{\theta J\text{-}PCB}$ (3)	11°C/W
Storage Temperature	-65°C to 150°C
Operating Junction Temperature	-40°C to 140°C
Soldering Temperature for 20 seconds	260°C
ESD Rating	2kV HBM

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, V_S =VC=10.5V,

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Control Circuit Supply (VC to PG)						
Operating Supply Range	$V_{VC\text{-}PG}$	8.5		10.5	V	No VC limiting Resistor
Quiescent Current	I_{VC}		1.5	2.0	mA	Normal operation, no fault
Clamp Voltage	$V_{VC\text{-}CLM}$	11	11.7	12.5	V	I_S=3mA
Clamp Shunt Resistance	R_{VC}			10	Ω	Delta I_S=10mA
Under-Voltage Rising Threshold	V_{VCUVR}	6.1	7.15	8.5	V	
Under-Voltage Falling Threshold	V_{VCUVF}	6	7.00	7.9	V	
Under-Voltage Hysteresis	$V_{VCUV\text{-}HS}$	100	150	200	mV	
VR Supply *(VR pin connected to Vin, Figure 1)*						
Operating Supply Range	$V_{VR\text{-}PG}$	10		14	V	Biased From VR pin
Quiescent Current	I_{VR}			10	mA	VR = 14V
Bias Resistor	R_{Bias}	300	420	550	Ω	

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Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, V_S=VC=10.5V,

Parameter	Symbol	Min	Typ	Max	Units	Conditions
DIFFERENTIAL AMPLIFIER AND COMPARATORS						
Common Mode Input Voltage	V_{CM}	-3		3	V	SP to S and SN to S
Differential Operating Input Voltage[(1)]	V_{SP-SN}	-80		400	mV	SP-SN
SP Input Bias Current	I_{SP}	35	55	75	µA	$V_{SP} = V_{SN} = V_S$
SN Input Bias Current	I_{SN}	35	55	75	µA	$V_{SP} = V_{SN} = V_S$
SN Current	I_{SN}		0.2	0.5	mA	V_{SN} = 14V, $V_{SP} = V_S = V_D$=0V
Reverse Comparator Threshold	V_{RVS-TH}	-11	-6	-2	mV	V_{SN} = 10.5V @ 25°C
Reverse Comparator Hysteresis	V_{RVS-HY}	10	12	14	mV	V_{SP-PG} = 10.5V @ 25°C
MOSFET Turn On Threshold	V_{FET-ON}	+1	+6	+11	mV	V_{SN} = 10.5V @ 25°C
Reverse Fault to MOSFETs Turn-off Time	t_{RVS}		90	150	ns	V_{SP-SN} = ± 50mV step
Forward Comparator Threshold	V_{FWD-TH}	250	275	300	mV	
Forward Comparator Hysteresis	V_{FWD-HY}	15	25	35	mV	
Internal N-Channel MOSFET						
Drain-to-Source Breakdown Voltage	BV_{DSS}	30			V	$V_S=V_{PG}=V_{SP}$=0V, I_D=2mA , Tj=25°C; V_{SN}=10.5V
Source Current Continuous	I_S			12	A	In ON state, Tj=25°C
Drain-to-Source On Resistance	$R_{DS(on)}$		4.5	6	mΩ	In ON state, Is=10A, Tj=25°C,
Body Diode Forward Voltage	V_{f-BD}		0.75	1.0	V	In OFF state, Is=4A, Tj=25°C
Fault: $\overline{FT}$						
$\overline{FT}$ Output Low Voltage	$V_{\overline{FT}}$		0.2	0.5	V	I_{GST}=1.5mA, VC>4.5V
$\overline{FT}$ Output High Leakage Current	$I_{\overline{FT}}$	-1			µA	$V_{\overline{FT}} = 14V$
$\overline{FT}$ Delay time	$t_{\overline{FT}-DLY}$	4	8	16	µs	V_{SP-SN} = ± 50mV step to 90% of $V_{\overline{FT}}$max,

Note 1*:* These parameters are not production tested but are guaranteed by design, characterization, and correlation with statistical process control.

Note 2: Current sourced by a pin is reported with a negative sign.

Note 3: Thermal resistance characterized on PI2126-EVAL1 evaluation board with 0LFM airflow.

Functional Description:

The PI2126 integrated *Cool-ORing* product takes advantage of two different technologies combining a 4.5mΩ on-state resistance ($R_{DS(on)}$) N-channel MOSFET with high density control circuitry. This combination provides superior density, minimizing PCB space to achieve an ideal ORing diode function, significantly reducing power dissipation and eliminating the need for heat sinking, while minimizing design complexity.

The PI2126's 4.5mΩ on-state resistance MOSFET used in the conduction path enables a dramatic reduction in power dissipation versus the performance of a diode used in conventional ORing applications due to its high forward voltage drop.

Due to the inherent characteristics of the MOSFET, while the gate remains enhanced above the gate threshold voltage it will allow current to flow in the forward and reverse directions. Ideal ORing applications do not allow for reverse current flow, so the controller has to be capable of very fast and accurate detection of reverse current caused by input power source failures, and turn off the gate of the MOSFET as quickly as possible. Once the gate voltage falls below the gate threshold, the MOSFET is off and the body diode will be reverse biased preventing reverse current flow and subsequent excessive voltage droop on the redundant bus.

Differential Amplifier:

The PI2126 integrates a high-speed low offset voltage differential amplifier to sense the difference between the Sense Positive (SP) pin voltage and Sense Negative (SN) pin voltage with high accuracy. The amplifier output is connected to the Reverse and Forward comparators.

Reverse Current Comparator: RVS

The reverse current comparator provides the critical function in the controller, detecting negative voltage caused by reverse current. When the SN pin is 6mV higher than the SP pin, the reverse comparator will force the gate discharge circuit to turn off the MOSFET in typically 90ns and assert the Fault ($\overline{FT}$) low with a typical delay of 8µs to report a fault condition.

The reverse comparator will hold the gate low until the SP pin is 6mV higher than the SN pin. Reverse comparator hysteresis is shown in Figure 3.

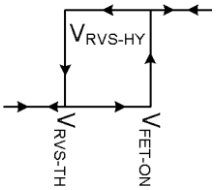

Figure 3: Reverse comparator hysteresis, the hysteresis voltage is SP-SN

Forward Voltage Comparator: FWD

The FWD comparator detects when a forward voltage condition exists and SP is above 275mV (typical) positive with respect to SN. When SP-SN is more than 275mV, the FWD comparator will assert the Fault ($\overline{FT}$) low to report a fault condition.

VC and Internal Voltage Regulator:

The PI2126 has a separate input VC that provides power to the control circuitry. An internal regulator clamps the VC voltage with respect to PG pin (V_{VC-PG}) to 11.7V typical.

The internal regulator circuit has a comparator to monitor VC voltage and pulls the MOSFET Gate low when VC is lower than the VC Under-Voltage Threshold.

The VR input pin can be connected to the input voltage eliminating the need for an external limiter in 12V Bus applications (10V to 14V). An internal 420Ω resistor is connected between the VR pin and the internal regulator VC pin.

Fault Indication: $\overline{FT}$

The $\overline{FT}$ pin is an open collector NPN that will be pulled low under the following fault conditions.

		Typical Condition	Indication of possible faults
1	Reverse:	V_{SP}-V_{SN} ≤ -6mV	Input supply shorted (MOSFET turned OFF)
2	Forward:	V_{SP}-V_{SN} ≥ +275mV	Open FET, Gate short or open, High current (MOSFET turned ON)
3	Forward	V_{SP}-V_{SN} ≤ +6mV	Shorted FET on power-up (MOSFET turned OFF)
4	UVLO	4.5V < V_{VC-PG} <7.15V	Controller not ready (MOSFET turned OFF)

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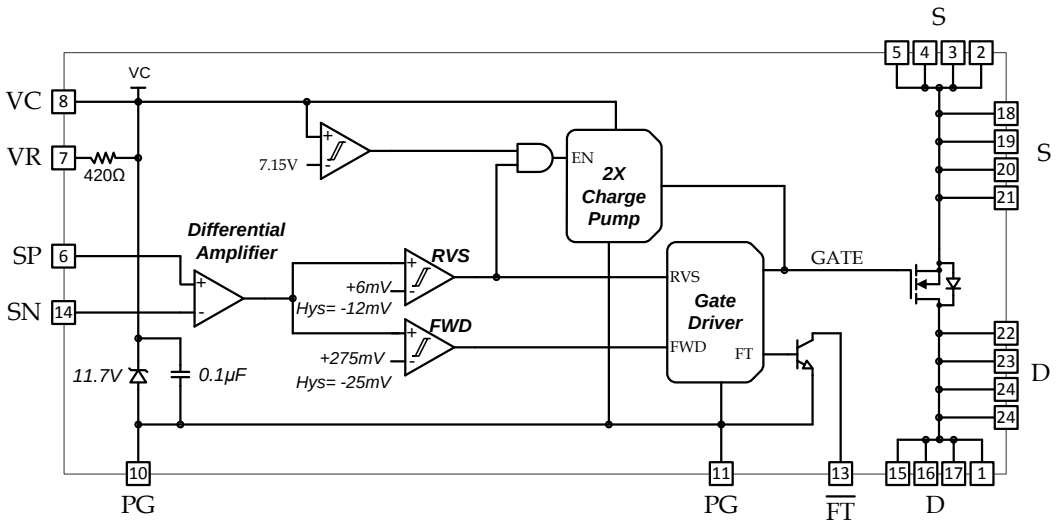


Figure 4: PI2126 Internal Block Diagram

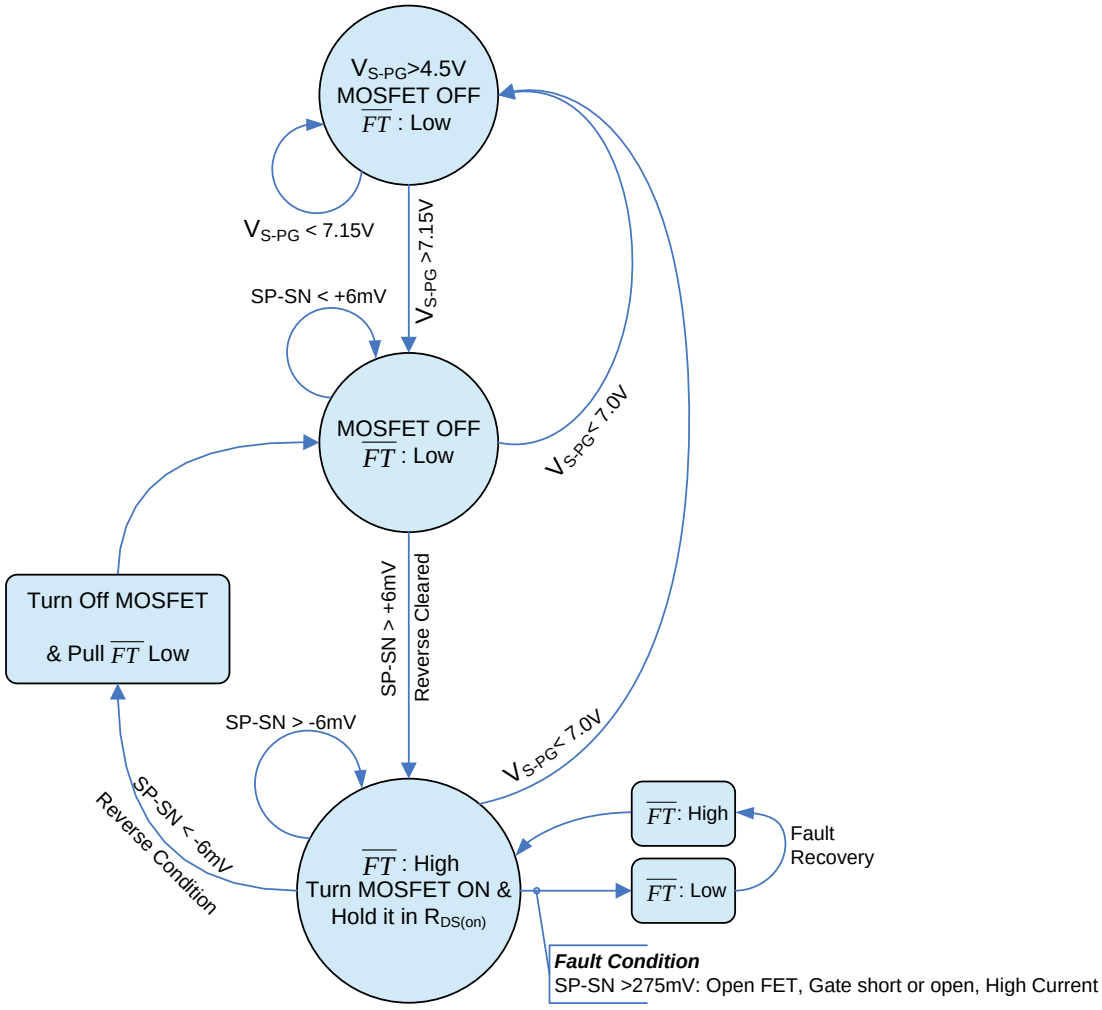
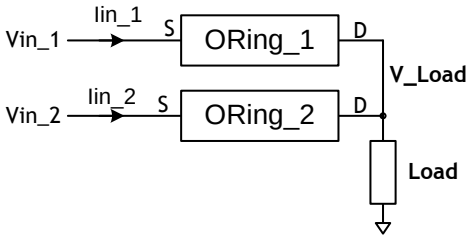


Figure 5: PI2126 State Diagram.



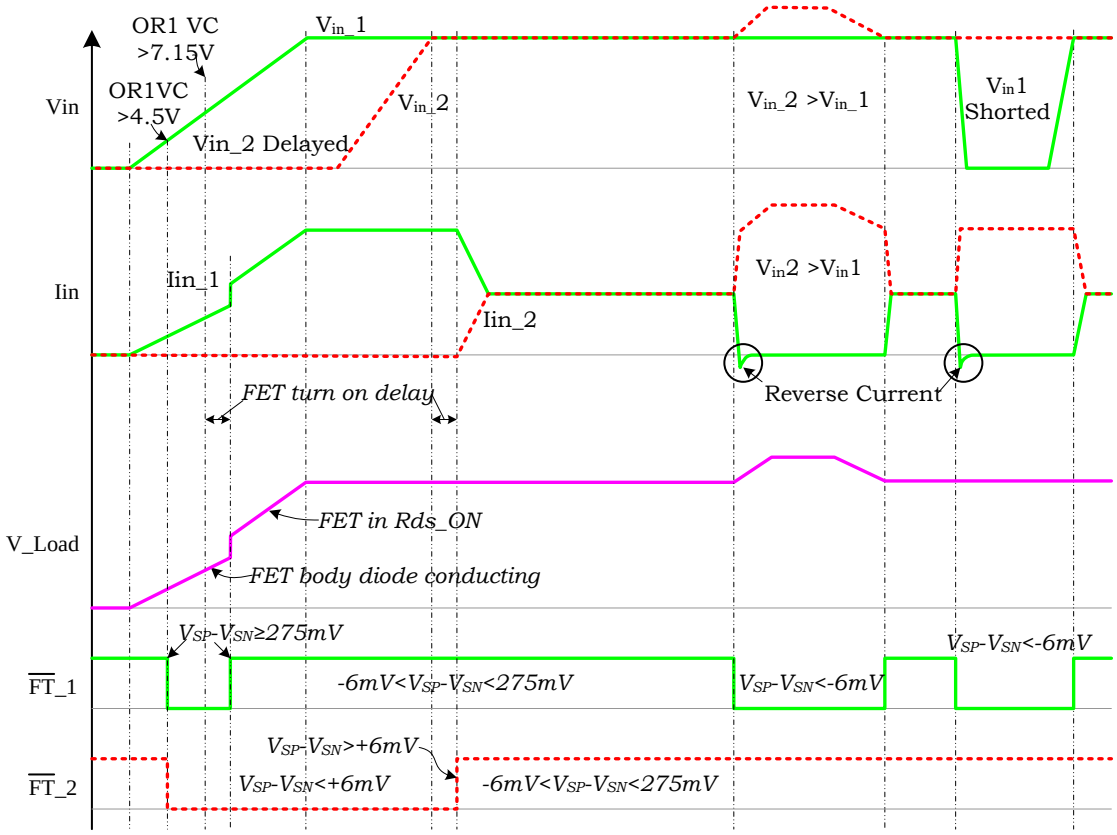


Figure 6: PI2126 Timing Diagram

Typical Characteristics:

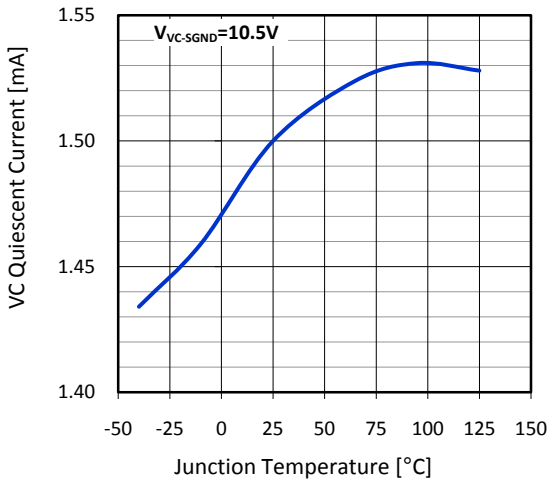


Figure 7: Controller quiescent current ($I_{VC:}$) vs. temperature.

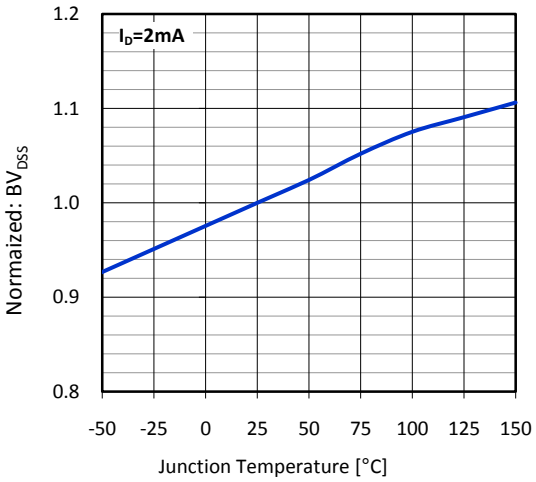


Figure 8: Drain-to-Source Breakdown Voltage (BV_{DSS}) vs. temperature

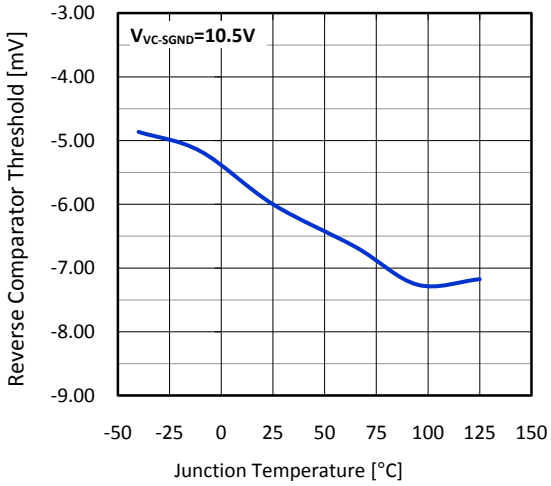


Figure 9: Reverse Comparator Threshold (V_{RVS-TH}) vs. temperature

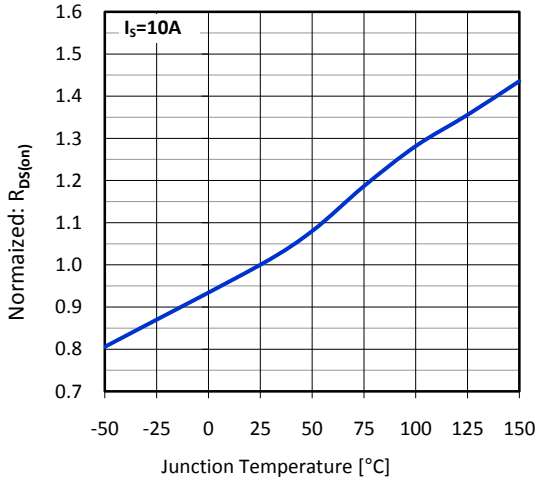


Figure 10: Drain-to-Source On Resistance ($R_{DS(on)}$) vs. temperature.

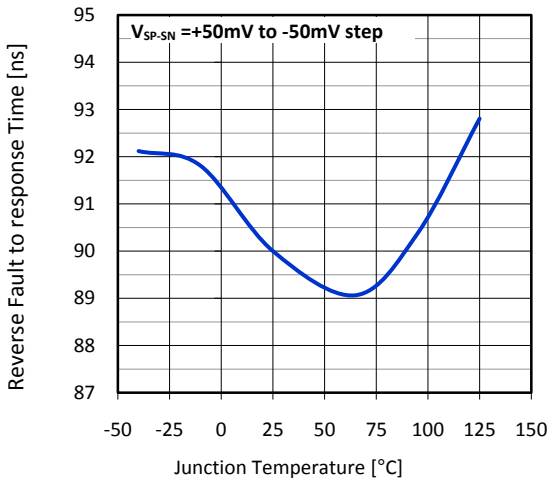


Figure 11: Reverse Fault to MOSFETs Turn-off Time (t_{RVS}) vs. temperature.

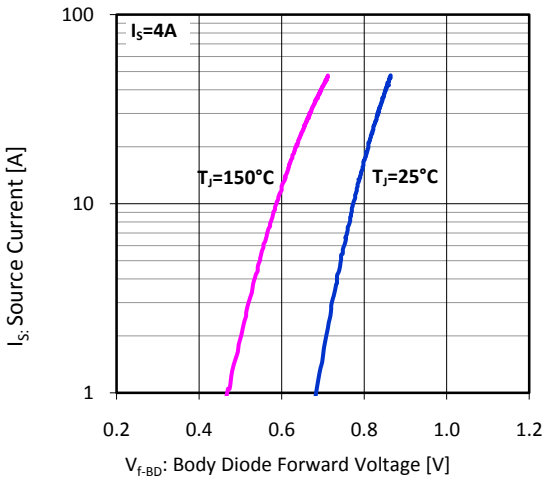


Figure 12: Body Diode Forward Voltage (V_{f-BD}) vs. temperature.

Thermal Characteristics:

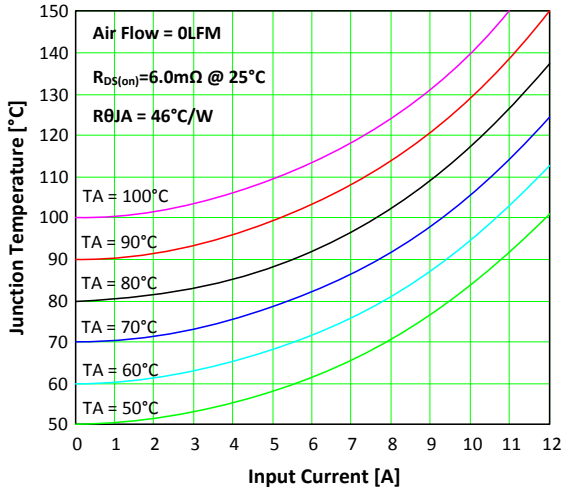


Figure 13: Junction Temperature vs. Input Current (0LFM)

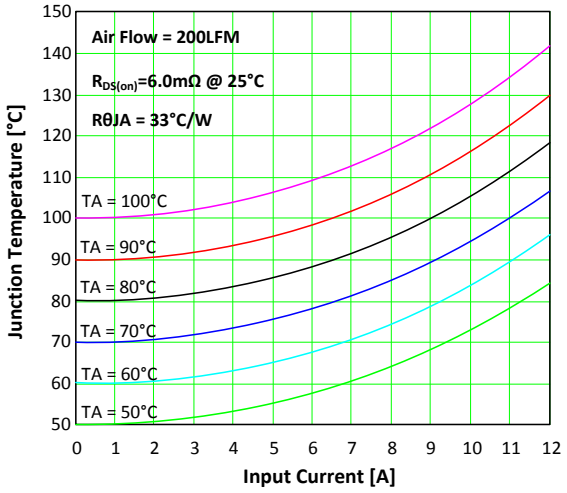


Figure 14: Junction Temperature vs. Input Current (200LFM)

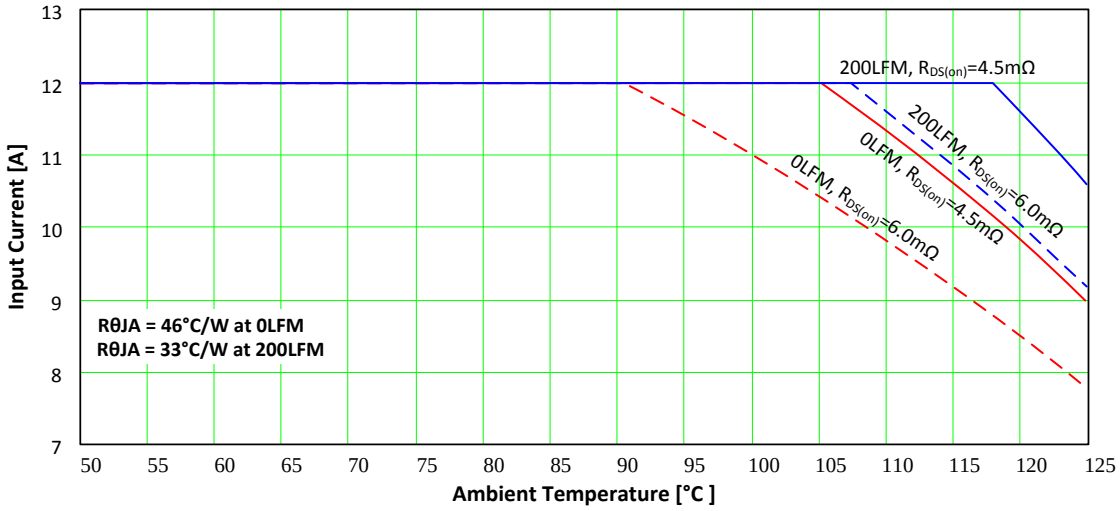


Figure 15: PI2126 input current de-rating based on maximum T_J=150°C vs. ambient temperature

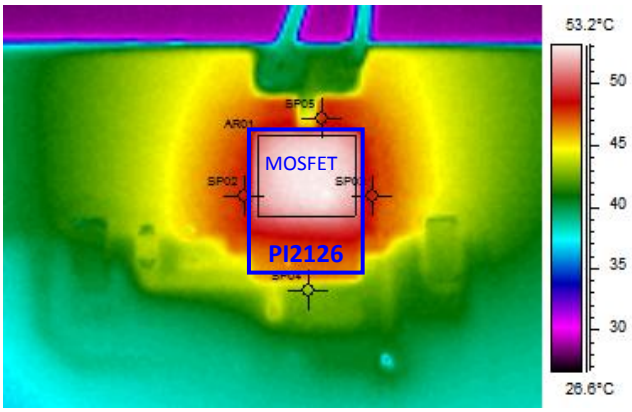


Figure 16: Thermal image of PI2126 mounted on PI2126-EVAL1Thermal Image picture, Iout=12A, T_A=25°C, Air Flow=0LFM
Note that the MOSFET $R_{DS(on)}$ of PI2126 under test is **4.1mΩ at T_A=25°C**

Application Information

The PI2126 is designed to replace high side ORing diodes in high current low voltage bus redundant power architectures. Replacing a traditional diode with a PI2126 will result in significant power dissipation reduction as well as board space reduction, efficiency improvement and additional protection features.

This section describes in detail the procedure to follow when designing with the PI2126 Active ORing solution.

Control Circuitry Bias:

The PI2126 control circuitry and the gate driver for the internal MOSFET are biased through the VC pin or VR pin. An internal regulator clamps the VC voltage (V_{VC-PG}) to 11.7V typically. An internal bypass ceramic capacitor (0.1µF) is connected between VC and PG to hold V_{VC-PG} steady.

In 12V system applications, where the input voltage (Vin) is between 10V and 14V, connect the VR pin to Vin and connect PG to the Vin return, **Figure 1**. A 420Ω internal resistor (R_{Bias}) is connected between the VR pin and the VC pin.

In high voltage applications above 14V, PG pin has to float above ground and VC pin will be connected directly to Vin. As shown in Figure 17, VR pin is disconnected and PG pin float on a bias resistor (R_{PG}). A low current low forward voltage drop Schottky diode is required for the PI2126 when PI2126 is configured floating on PG. Connect one terminal of R_{PG} to the PG pin and the other end of R_{PG} to ground (Vin return). Connect the Schottky diode anode to the PG pin and connect its cathode to the VC pin.

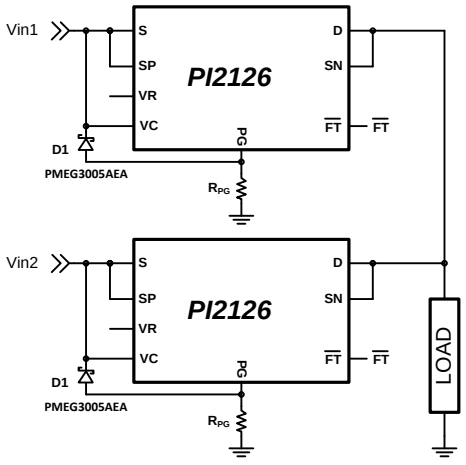


Figure 17: PI2126 in application above 14V

Recommended Schottky Diode:

PMEG3005AEA: from NXP or equivalent

R_{PG} selection for input voltage greater than 14V:

Select the resistor (R_{PG}) value at the minimum input voltage to avoid a voltage drop that may reduce V_{VC-PG} lower than VC under voltage lockout.

Select the value of R_{PG} using the following equations:

$$R_{PG} = \frac{Vin_{Min} - V_{VCUVR\_Max}}{I_{VC\ Max} + 0.1mA}$$

And R_{PG} maximum power dissipation is:

$$Pd_{RPG} = \frac{(Vin_{Max} - V_{VC-CLM\_Max})^2}{R_{PG}}$$

Where:

Vin_{Min}: Minimum applied input voltage

Vin_{Max}: Maximum applied input voltage

V_{VCUVR_Max}: Controller maximum Under-Voltage Rising Threshold, 8.5V

V_{VC-CLM_Max}: Controller maximum clamp voltage, 12.5V

$I_{VC\ Max}$: Controller maximum bias current, use 2.0mA

$0.1mA$: 0.1mA is added for margin

R_{PG} calculation example

Vin (minimum) = 11V and Vin (maximum) = 18V

$$R_{PG} = \frac{Vin_{Min} - V_{VCUVR\_Max}}{I_{VC\ Max} + 0.1mA}$$

$$R_{PG} = \frac{11V - 8.5V}{2mA + 0.1mA} = 1.190K\Omega$$

Select a lower typical resistor value (1KΩ) and calculate its power dissipation.

$$Pd_{RPG} = \frac{(Vin_{Max} - V_{VC-CLM\_Max})^2}{R_{PG}}$$

$$Pd_{RPG} = \frac{(18V - 11V)^2}{1K\Omega} = 49mW$$

Internal N-Channel MOSFET BV_{DSS}:

The PI2126's internal N-Channel MOSFET breakdown voltage (BV_{DSS}) is rated for 30V at 25°C and will degrade to 28V at -40°C, refer to Figure 8. Drain to source voltage should not exceed B_{VDSS} in nominal operation. During a fast switching transient the MOSFET can tolerate voltages higher than its B_{VDSS} rating under avalanche conditions, refer to the Absolute Maximum Ratings table.

In Active ORing applications when one of the input power sources is shorted, a large reverse current is sourced from

the load through the MOSFET. Depending on the output impedance of the system and the parasitic inductance, the reverse current in the MOSFET may exceed the source pulsed current rating (60A) before the PI2126 MOSFET is turned off.

The peak current during an input short condition is calculated as follows, assuming that the output has very low impedance and it is not a limiting factor:

$$I_{PEAK} = \frac{V_S * t_{RVS}}{L_{PARASITIC}}$$

Where:

I_{PEAK}: Peak current in PI2126 MOSFET before it is turned off.

V_S: Input voltage or load voltage at S pin before input short condition did occur.

t_{RVS}: Reverse fault to MOSFET turn-off time.

$L_{PARASITIC}$: Circuit parasitic inductance

The high peak current during an input short stores energy in the circuit parasitic inductance, and as soon as the MOSFET turns off, the stored energy will be released and this will produce a high negative voltage and ringing at the MOSFET source. At the same time the energy stored at the drain side of the internal MOSFET will be released and produce a voltage higher than the load voltage. This event will create a high voltage difference between the drain and source of the MOSFET. ***The MOSFET may avalanche, but this avalanche will not affect the MOSFET performance because the PI2126 has a fast response time to the input fault condition and the stored energy will be well below the MOSFET avalanche capability***.

MOSFET avalanche during input short is calculated as follows:

$$E_{AS} = \frac{1}{2} * \frac{1.3 * BV_{DSS}}{1.3 * BV_{DSS} - V_S} * L_{PARASITIC} * {I_{PEAK}}^2$$

Where:

E_{AS}: Avalanche energy

BV_{DSS}: MOSFET breakdown voltage (30V)

Power dissipation:

In Active ORing circuits the MOSFET is always on in steady state operation and the power dissipation is derived from the total source current and the on-state resistance of the MOSFET.

The PI2126 internal MOSFET power dissipation can be calculated with the following equation:

$$Pd_{MOSFET} = Is^2 * R_{DS(on)}$$

Where:

Pd_{MOSFET}: MOSFET power dissipation

Is: Source Current

$R_{DS(on)}$: MOSFET on-state resistance

Note: For the worst case condition, calculate with maximum rated $R_{DS(on)}$ at the MOSFET maximum operating junction temperature because $R_{DS(on)}$ value is directly proportional to temperature. Refer to Figure 10 for normalized $R_{DS(on)}$ values over temperature. The PI2126 maximum $R_{DS(on)}$ at 25°C is 6mΩ and will increase by 40% at 125°C junction temperature.

The Junction Temperature rise is a function of power dissipation and thermal resistance.

$$T_{rise} = R_{\theta JA} * Pd_{MOSFET} = R_{\theta JA} * Is^2 * R_{DS(on)}$$

Where:

$R_{\theta JA}$: Junction-to-Ambient thermal resistance, 46°C/W

This may require iteration to get to the final junction temperature. Figure 13 and Figure 14 show the PI2126 internal MOSFET final junction temperature curves versus conducted current at maximum $R_{DS(on)}$, given ambient temperatures and air flow.

Typical application Example:

Requirement:

Redundant Bus Voltage = 12V (±10%, 10.8V to 13.2V)

Load Current = 10A (assume through each redundant path)

Maximum Ambient Temperature = 60°C

Solution:

A single PI2126 for each redundant 12V power source should be used, configured as shown in the circuit schematic in Figure 18. PG pin is connected to ground and VR pin is connected to Vin,

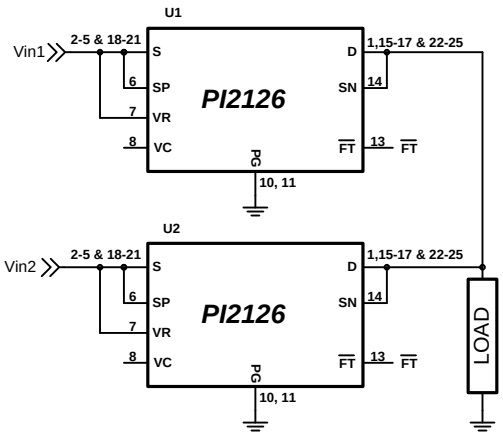


Figure 18: PI2126 in 12V redundant bus voltage application

The fault pin ($\overline{FT}$) can be pulled to the system logic level voltage via a resistor (10kΩ), or it can be connected to the input voltage (Vin) via a 25kΩ resistor.

Power Dissipation and Junction Temperature:

First use Figure 13 (Junction Temperature vs. Input Current) to find the final junction temperature for 10A load current at 60°C ambient temperature. In Figure 13 (illustrated in Figure 19) draw a vertical line from 10A to intersect the 60°C ambient temperature line. At the intersection draw a horizontal line towards the Y-axis (Junction Temperature). The Junction Temperature at maximum load current (10A) and 60°C ambient is 95°C.

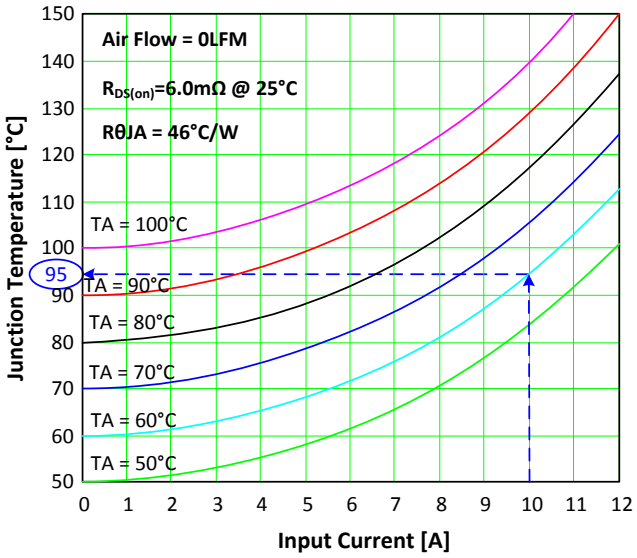


Figure 19: Example 1 final junction temperature at 10A/60°C

$R_{DS(on)}$ is 6mΩ maximum at 25°C and will increase as the Junction temperature increases. From Figure 10, at 95°C $R_{DS(on)}$ will increase by 26%, then

$R_{DS(on)} = 6m\Omega * 1.26 = 7.56m\Omega$ maximum at 95°C

Maximum power dissipation is:

$$Pd_{Max} = Iin^2 * R_{DS(on)} = (10A)^2 * 7.56m\Omega = 756\text{mW}$$

Recalculate T_J:

$$T_{J\_Max} = T_A + (T_{JA} * Pd_{Max})$$

$$T_{J\_Max} = 60℃ + \frac{46℃}{W} * 0.756W = \ 94.8℃$$

Layout Recommendation:

Use the following general guidelines when designing printed circuit boards. An example of the typical land pattern for the PI2126 is shown in Figure 20:

- Make sure to have a solid ground (return) plane to reduce circuit parasitic inductance.
- Connect all S pads together with a wide trace to reduce trace parasitics to accommodate the high current input, and also connect all D pads together with a wide trace to accommodate the high current output.
- Connect the SP pin to the S pins and connect the SN pin to D pins outside the SiP as shown in Figure 20.
- Use 1oz copper or thicker if possible to reduce trace resistance and power dissipation.
- C6 typically is not required, but if addition bypassing is preferred, Figure 20 shows the appropriate layout for an extra VC capacitor.

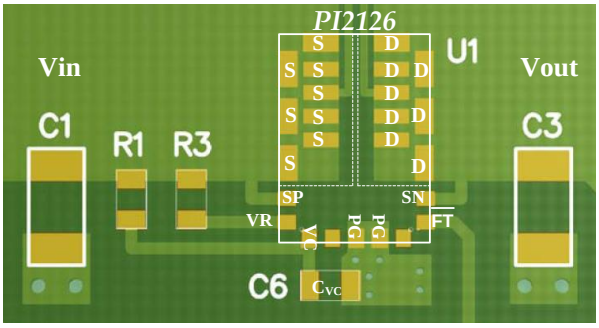


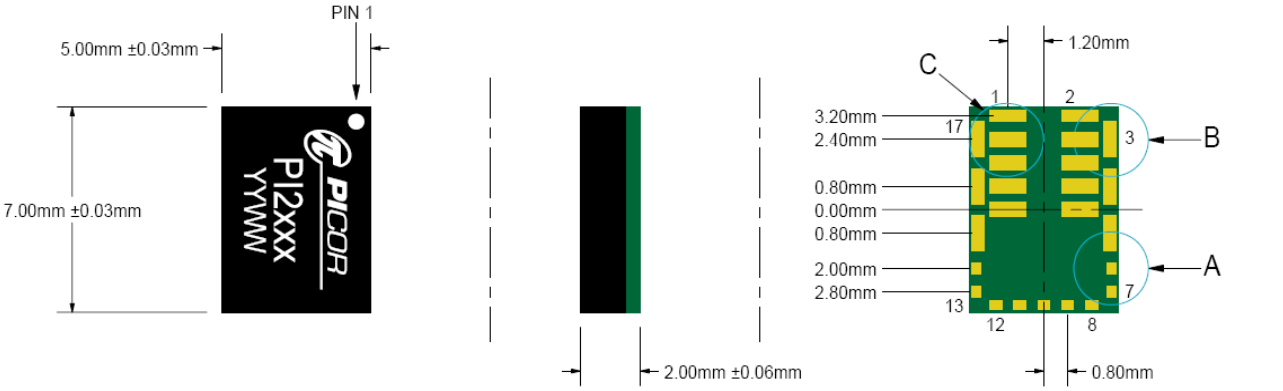
Figure 20: Layout recommendation

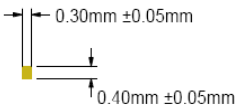
Figure 21: PI2126 Mounted on PI2126-EVAL1

Please visit http://vicorpower.com/picorpower/ for information on PI2122-EVAL1

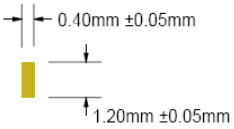
EOL

Package Drawings:

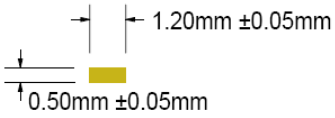




A: I/O Pads (Pins 6 - 14)
Copper Defined



B: Power Pads (Pins 1 - 5, 15 - 17)
Soldermask Defined



C: Internal Power Pads
Soldermask Defined (8 Places)

Ordering Information:

Part Number	Package	Transport Media
PI2126-00-LGIZ	5mm x 7mm 25-pin LGA	TRAY

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