

74LVX112

Low Voltage Dual J-K Flip-Flops with Preset and Clear

General Description

The LVX112 is a dual J-K Flip-Flop where each flip-flop has independent inputs (J, K, PRESET, CLEAR, and CLOCK) and outputs (Q, $\bar{Q}$). These devices are edge sensitive and change states synchronously on the negative going transition of the clock pulse. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. Clear and Preset are independent of the clock and are accomplished by a low logic level on the corresponding input. The J and K inputs can change when the clock is in

either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock.

The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

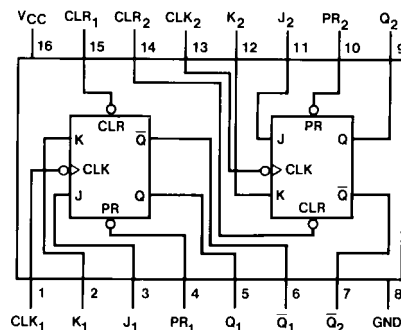
- Input voltage level translation from 5V–3V
- Ideal for low power/low noise 3.3V applications

Ordering Code:

Order Number	Package Number	Package Description
74LVX112M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVX112SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX112MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
J ₁ , J ₂ , K ₁ , K ₂	Data Inputs
CLK ₁ , CLK ₂	Clock Pulse Inputs (Active Falling edge)
CLR ₁ , CLR ₂	Direct Clear Inputs (Active LOW)
PR ₁ , PR ₂	Direct Preset Inputs (Active LOW)
Q ₁ , Q ₂ , $\bar{Q}_1$, $\bar{Q}_2$	

Truth Table

Inputs					Outputs	
PR	CLR	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\sim$	h	h	$\overline{Q}_0$	Q_0
H	H	$\sim$	l	h	L	H
H	H	$\sim$	h	l	H	L
H	H	$\sim$	l	l	Q_0	$\overline{Q}_0$

H (h) = HIGH Voltage Level

L (l) = LOW Voltage Level

X = Immaterial

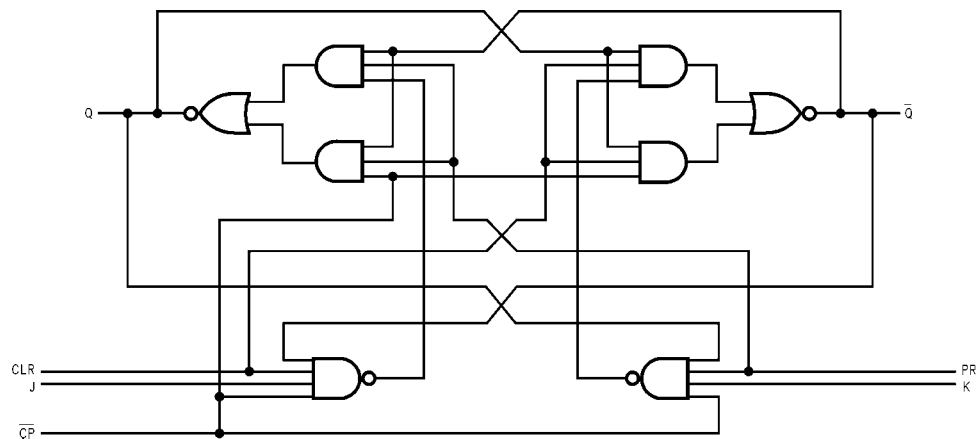
$\sim$ = HIGH-to-LOW Clock Transition

Q_0 ($\overline{Q}_0$) = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram

(One Half Shown)



Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current	
(I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Typ	Max	Min	Max		
V_{IH}	HIGH Level Input Voltage	2.0	1.5			1.5		V	
		3.0	2.0			2.0			
		3.6	2.4			2.4			
V_{IL}	LOW Level Input Voltage	2.0			0.5		0.5	V	
		3.0			0.8		0.8		
		3.6			0.8		0.8		
V_{OH}	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -4 \text{ mA}$
		3.0	2.9	3.0		2.9			
		3.6	2.58			2.48			
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 4 \text{ mA}$
		3.0		0.0	0.1		0.1		
		3.6			0.36		0.44		
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	$V_{IN} = 5.5V \text{ or } GND$
I_{CC}	Quiescent Supply Current	3.6			2.0		20.0	μA	$V_{IN} = V_{CC} \text{ or } GND$

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	C _L (pF)
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay CP _n to Q _n or $\overline{Q}_n$	2.7		7.5	12.0	1.0	14.2	ns	15
t _{PHL}				11.0	16.7	1.0	19.0		50
		3.3 ± 0.3		8.5	11.0	1.0	13.4		15
				10.0	15.0	1.0	16.5		50
t _{PLH}	Propagation Delay PR or CLR to Q _n or $\overline{Q}_n$	2.7		7.0	11.5	1.0	12.3	ns	15
t _{PHL}				10.1	14.3	1.0	16.5		50
		3.3 ± 0.3		6.7	10.2	1.0	11.7		15
				9.7	13.5	1.0	15.0		50
t _W	Pulse Width (CP or CLR or PR)	2.7	5.0			5.0		ns	
		3.3 ± 0.3	5.0			5.0			
t _S	Setup Time (J _n or K _n to CP _n)	2.7	5.5			5.5		ns	
		3.3 ± 0.3	5.0			5.0			
t _H	Hold Time (J _n or K _n to CP _n)	2.7	1.0			1.0		ns	
		3.3 ± 0.3	1.0			1.0			
t _{REC}	Recovery Time (CLR or PR to CP)	2.7	6.5			6.5		ns	
		3.3 ± 0.3	6.0			6.0			
f _{MAX}	Maximum Clock Frequency	2.7	90	140		85		MHz	15
			85	115		70			50
		3.3 ± 0.3	110	150		100			15
			90	120		80			50
t _{OSLH} ¹	Output to Output Skew (Note 3)	2.7			1.5		1.5	ns	50
t _{OSHL}		3.3			1.5		1.5		

Note 3: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$; $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

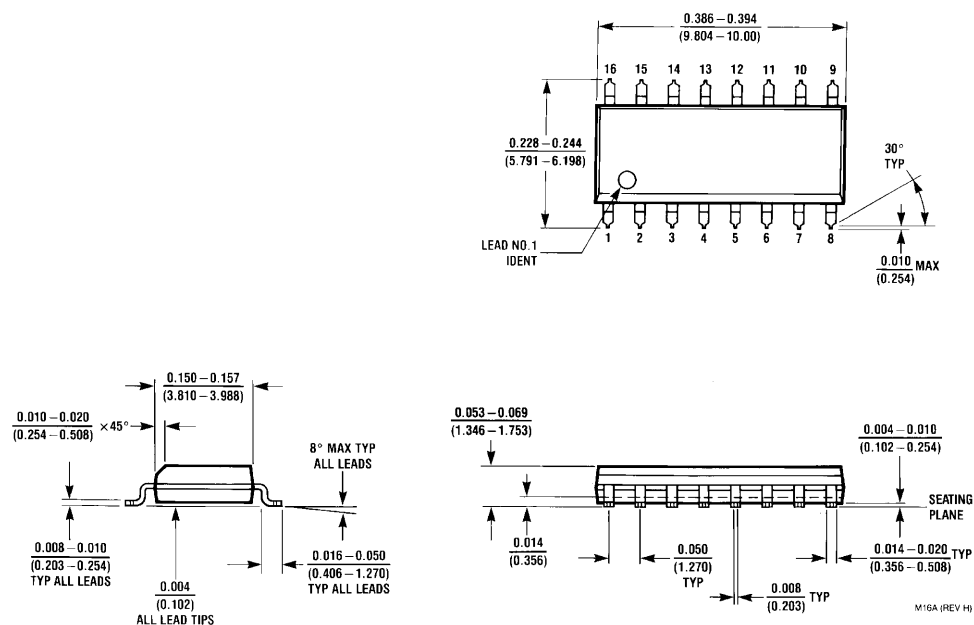
Capacitance

Symbol	Parameter	T _A = +25°C			T _A = -40°C to +85°C		Units
		Min	Typ	Max	Min	Max	
C _{IN}	Input Capacitance		4	10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 4)		18				pF

Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

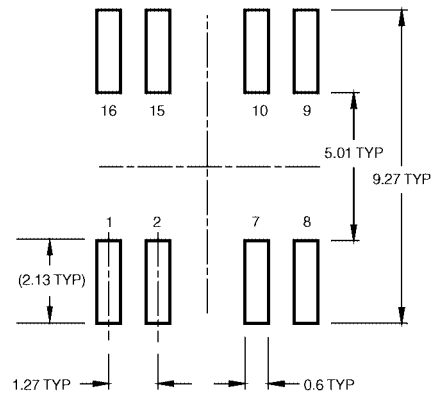
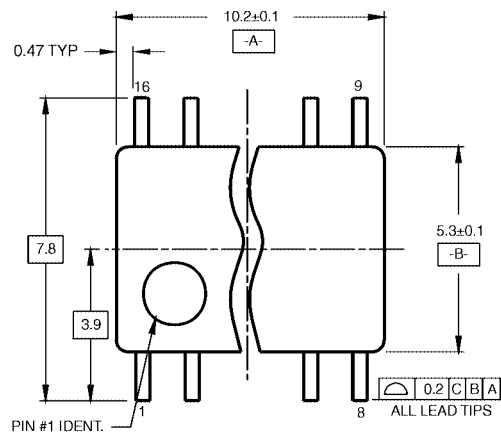
$$\text{Average operating current can be obtained by the equation: } I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{2 \text{ (per F/F)}}$$

Physical Dimensions inches (millimeters) unless otherwise noted

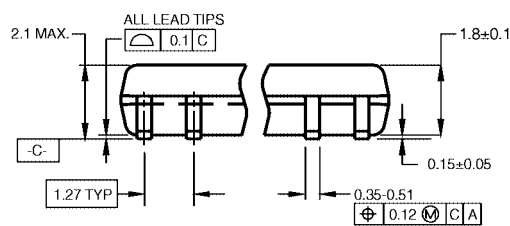


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

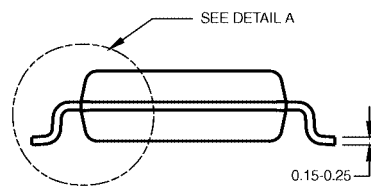
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



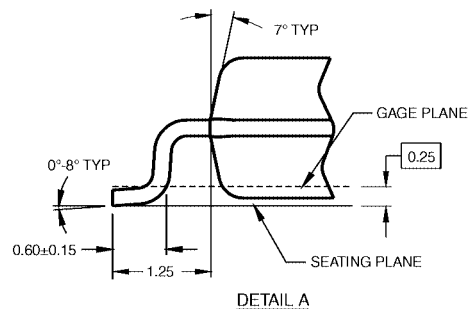
DIMENSIONS ARE IN MILLIMETERS



NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

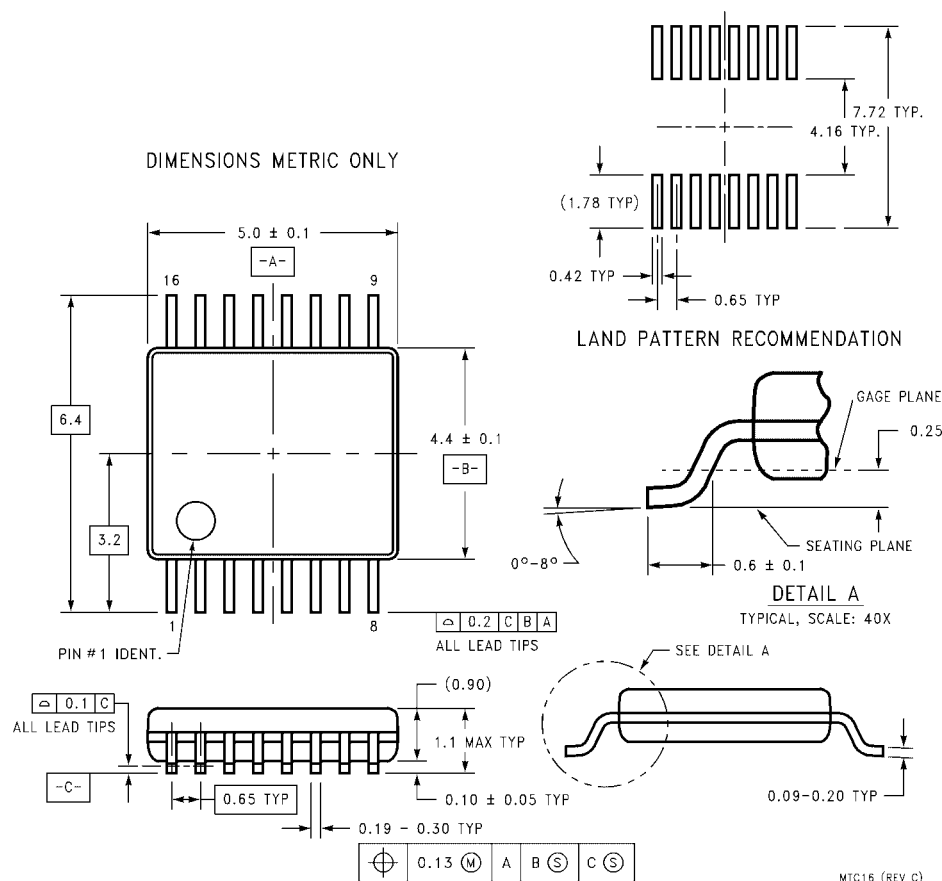
M16DRevB1



DETAIL A

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

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