NCP5021

High Voltage White LED Driver with Ambient Light Sensing

The NCP5021 product is a single output boost LED driver capable of driving up to 8 LEDs in series for portable backlight applications.

The built−in DC/DC converter is based on a high efficient PWM boost structure with 32 V output voltage span. It provides a peak 90% efficiency together with a 1% I−LED current tolerance.

Features

- 2.7 to 5.5 V Input Voltage Range
- 90% Peak efficiency with 4.7 μH / 150 mΩ Inductor
- Gradual Dimming Built−in (Automatic Fade In/Fade Out Effect)
- Integrated Ambient Light Sensing Automatically Adjusts the LCD Backlight Contrast
- Built−in Zero Current Load Leakage under Idle Mode
- Support the Full I2C Protocol with Address Extension
- Tight 1% I−LED Tolerance
- Ultra Thin 0.5 mm QFN16 Package
- This is a Pb−Free Device

Typical Applications

- Cellular Phone, Smartphone
- Portable Media Player (PMP)
- Global Positioning System (GPS)

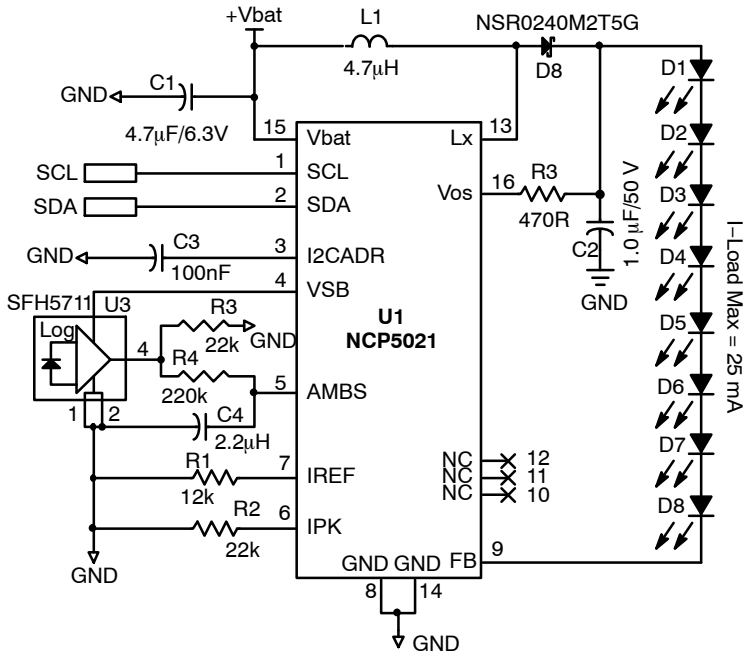
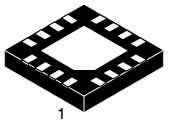


Figure 1. Typical Large Display LED Driver

ON Semiconductor®

http://onsemi.com



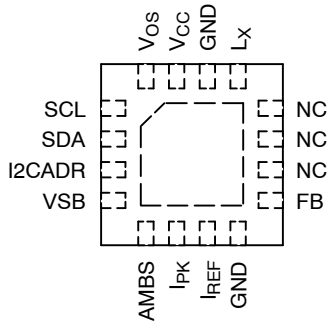
UQFN16
MU SUFFIX
CASE 523AF

MARKING DIAGRAM

5021	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)
NC = Not Connected

ORDERING INFORMATION

Device	Package	Shipping†
NCP5021MUTXG	UQFN16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. PIN DESCRIPTIONS

PIN	Name	Type	Description
1	SCL	INPUT, DIGITAL	This pin carries the I2C clock to control the DC/DC converter and to set up the output current and the photo sensor. The SCL clock is associated with the SDA signal.
2	SDA	INPUT, DIGITAL	This pin carries the data provided by the I2C protocol. The content of the SDA byte is used to program the mode of operation and to set up the output current.
3	I2CADR	INPUT, DIGITAL	This pin is used to select the I2C address of the NCP5021: – I2CADR = Low → address = %0111 0010 = $72 – I2CADR = High → address = %0111 0100 = $74 In order to avoid any risk during the operation, the digital levels are intended to be hardwired prior to power up the system.
4	VSB	POWER, OUTPUT	This pin provides a switched voltage, derived from the Vbat supply, to bias the external photo sense. The current capability of this voltage is 1 mA. The VSB pin is disconnected when the Shutdown mode has been engaged.
5	AMBS	INPUT, ANALOG	This pin senses the voltage developed across the external Photo Bias resistor. Since this is a very high impedance input, cares must be observed to minimize the leakage current and the noise that may influence the photo sense analog function. The bias parameters associated with the AMBS pin are reloaded when the chip resumes from Shutdown to Normal operation.
6	I_{PK}	INPUT, ANALOG	This pin provides the inductor peak current during normal operation. In no case shall the voltage at I_{PK} pin be forced either higher or lower than the 1144 mV provided by the internal reference.
7	I_{REF}	INPUT, ANALOG	This pin provides the reference current, based on the internal band−gap voltage reference, to control the output current flowing in the LED. A 1% tolerance, or better, resistor shall be used to get the highest accuracy of the LED biases. An external current source can be used to bias this pin to dim the light coming out of the LED. In no case shall the voltage at I_{REF} pin be forced either higher or lower than the 1144 mV provided by the internal reference.
8	AGND	POWER	This pin is the GROUND signal for the analog and digital blocks and must be connected to the system ground. A ground plane is strongly recommended.
9	FB	INPUT, ANALOG	This pin is the current sense of the series arranged LED. The built−in current mirror will automatically adapt the voltage drop across this pin (typically 400 mV).
10	NC		This pin shall be left open for normal operation.
11	NC		This pin shall be left open for normal operation.
12	NC		This pin shall be left open for normal operation.
13	Lx	POWER	The external inductor shall be connected between this pin (drain of the internal Power switch) and Vbat. The voltage is internally clamped at 40 V under worst case conditions. The external Schottky diode shall be connected as close as possible to this pin. See Note 1 for ESR recommendations.
14	PGND	POWER	This pin is the GROUND reference for the DC/DC converter and the output current control. The pin must be connected to the system ground, a ground plane being strongly recommended.
15	VBAT	INPUT, POWER	Input Battery voltage to supply the analog , the digital blocks and the main Power switch driver. The pin must be decoupled to ground by a 10 μF ceramic capacitor.
16	Vos	OUTPUT, POWER	This pin senses the output voltage supplied by the DC/DC converter. The Vos pin must be bypassed by 1.0 μF/50 V ceramic capacitor located as close as possible to the pin to properly bypass the output voltage to ground. The circuit shall not operate without such bypass capacitor connected to the Vos pin. The output voltage is internally clamped to 40 V maximum in the event of no load situation. NOTE: Due to the very fast dV/dt transient developed during the operation, using a low pass filter is strongly recommended as depicted in the schematic diagram Figure 1.
NC	–	Not Connected	Back side exposed pad is not internally connected and can be either left floating or connected to the system Ground.

1. Using low ESR ceramic capacitor (X5R or better) and low ESR inductor with minimum Eddie losses is mandatory to optimize the DC/DC efficiency.

Table 2. MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{BAT}	Power Supply	−0.3 < V < 7.0	V
V_{LX}	Output Switching Voltage	34	V
SCL, SDA	Digital Input Voltage Digital Input Current	−0.3 < V < V_{BAT} 1	V mA
ESD	Human Body Model: R = 1500 Ω, C = 100 pF (Note 2) Machine Model	2 200	kV V
 P_D $R_{\theta JC}$ $R_{\theta JA}$	LLGA16 package Power Dissipation @ T_A = +85°C (Note 3) Thermal Resistance Junction to Case Thermal Resistance Junction to Air	 300 50 130	 mW °C/W °C/W
T_A	Operating Ambient Temperature Range	−40 to +85	°C
T_J	Operating Junction Temperature Range	−40 to +125	°C
T_{Jmax}	Maximum Junction Temperature	+150	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
	Latch−up current maximum rating per JEDEC standard: JESD78.	±100	mA
MSL	Moisture Sensitivity Level (Note 4)	1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115
3. The maximum package power dissipation limit must not be exceeded.
4. per IPC/JEDEC standard: J−STD−020A.

Table 3. POWER SUPPLY SECTION (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted), operating conditions 2.85 V < V_{bat} < 5.5 V, unless otherwise noted.

Symbol	Rating	Min	Typ	Max	Unit
V_{bat}	Power Supply Operating Range	2.7		5.5	V
V_{UVLO}	Power Supply Undervoltage Lockout	2.0	2.2	2.4	V
V_{UVLOHY}	Undervoltage Lockout Hysteresis		150		mV
I_{out}	Continuous DC Current in the load, V_{out} pin @ 3.0 V< V_{bat} < 5.5 V	25			mA
I_{LKLX}	Power Switch Leakage Current (Lx pin) @ I_{out} = 0			200	nA
V_{OVP}	Output Voltage Overvoltage Protection	30	32	34	V
V_{OVPHYS}	OVP Output Voltage Hysteresis		1.5		V
t_{start}	DC/DC Start time (C_{out} = 4.7 μF), 3.0 V < V_{bat} = nominal < 5.5 V from last ACK bit to full load operation		600		μs
I_{STBY}	Standby Current, V_{bat} = 3.6 V, I_{out} = 0 mA @ SCL = SDA = H (no port activity)			1.0	μA
I_{op}	Operating Current, @ I_{out} = 0 mA, V_{bat} = 3.6 V		2.0		mA
I_{PK}	Maximum Inductor Peak Current	−10%	855	+10%	mA
I_{TOL}	Output Current Tolerance @ V_{bat} = 3.6 V, I_{LED} = 10 mA, −25°C < T_A < 85°C		±1		%
F_{PWR}	Boost Operating Frequency, −40°C < T_A < 85°C	1.13	1.30	1.47	MHz
T_{SD}	Thermal Shut Down Protection		160		°C
T_{SDH}	Thermal Shut Down Protection Hysteresis		30		°C
E_{PWR}	Efficiency @ V_{bat} = 3.6 V, ESR < 150 mΩ, Coilcraft = LPO3310−472ML, C_{out} = 1.0 μF (Note 5) I_{LED} = 10 mA, Vf = 2.85 V I_{LED} = 25 mA, Vf = 3.4 V		 75 80		%

5. Using low ESR inductor with low Eddy current losses is mandatory to get the high efficiency operation.

Table 4. ANALOG SECTION: (Typical values are referenced to Ta = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted), operating conditions 2.85 V < Vbat < 5.5 V, unless otherwise noted.

Pin	Symbol	Rating	Min	Typ	Max	Unit
7	I_{REF}	Reference Current @ Vref = 1144 mV (Note 6)	1.0		100	μA
6	I_{PK}	Reference Current @ Vref = 1144 mV (Note 6)	1.0		100	μA
	k_{ref}	Reference Current to ILED Peak Current Ratio		250		
	k_{pk}	Reference Current to Inductor Peak Current Ratio		9700		
7	V_{REF}	Reference Voltage (Note 6)	−3%	1144	+3%	mV
6	V_{REFK}	Reference Voltage (Note 6)	−10%	1144	+10%	mV
9	V_{FB}	Feedback Voltage (Note 7)		425		mV
	M_{DCY}	Boost Operating Maximum Duty Cycle	90.5	94		%
9	I_{LKGM}	Current Mirror Leakage Current			200	nA
	F_{LF}	Low Frequency Clock derived from the internal 1.3 MHz clock (Note 9)	0.6		20	Hz
4	V_{VSD}	Photo Sense Bias Supply @ Ibias = 1 mA	2.5		Vbat	V
4	R_{VSD}	Photo Sense Bias Supply internal impedance		30		Ω
4	I_{SDUSD}	Photo Sense Leakage Current (Note 9)			100	nA
	$G_{AMB0.25}$	Photo Sense Internal Gain 1/4		0.25		
	$G_{AMB0.50}$	Photo Sense Internal Gain 1/2		0.5		
	G_{AMB01}	Photo Sense Internal Gain 1		1		
	G_{AMB02}	Photo Sense Internal Gain 2		2		
	G_{AMB04}	Photo Sense Internal Gain 4		4		
5	V_{iph}	Photo Sense Input Voltage (Note 10)			1.5	V

6. The external circuit must not force the $I_{REF\ or}$ I_{PK} pin voltage either higher or lower than the 1144 mV specified. The reference voltage applies to both IREF and IPK pins.
7. The overall output current tolerance depends upon the accuracy of the external resistor. Using 1% or better resistor is recommended.
8. This parameter guarantees the function for production test purposes.
9. Guaranteed by design and characterized.
10. The ambient sense linearity is guaranteed when the voltage at the output of the internal amplifier is limited to 1.5 V. This voltage is equal to the input voltage times the programmed gain. Beyond this value, the operational amplifier is in the saturation region and the linearity is no longer guaranteed.

Table 5. DIGITAL PARAMETERS SECTION (Typical values are referenced to Ta = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted), operating conditions 2.85 V < Vbat < 5.5 V, unless otherwise noted. (Note 11)

Symbol	Rating	Min	Typ	Max	Unit
F_{SCK}	InputI2C Clock Frequency (Note 9)			400	kHz
V_{IH}	Positive going Input High Voltage Threshold, SCL, SDA signals	1.6		V_{BAT}	V
V_{IL}	Negative going Input High Voltage Threshold, SCL, SDA signals	0		0.4	V
C_{IN}	SDA Input Capacitance (Note 9)		10	15	pF
V_{IHD}	I2C Address Extension	Vbat * 0.7		Vbat + 0.3 V	V
V_{ILD}	I2C Address Extension	0		0.3	V

11. Digital inputs undershoot < −0.30 V to ground, Digital inputs overshoot < 0.30 V to V_{BAT}

ESD Protection Circuit

Depending upon the function of the pin, different circuitry is applied. The basic structure are illustrated in Figure 2.

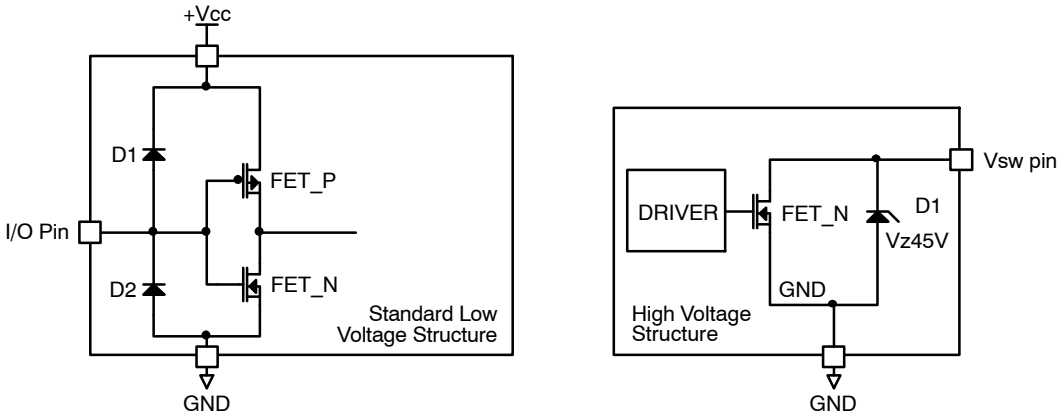


Figure 2. Typical ESD Protection Structures

Although the structures are capable to handle the ESD stresses (as defined by the JEDEC specifications), no current or voltage, either DC or AC, beyond the maximum ratings specifications shall be applied to any pin.

DC/DC Operation

The boost converter is based on a PWM structure to generate the output voltage necessary to drive the series arranged LED. The system includes an open load detection to avoid over voltage situation when the LED are disconnected from the Vout pin. A built−in circuit prevent high inrush current when the system is powered.

The ILED is regulated by means of a built−in current mirror controlled by the digital content of the ILEDREG register. With a typical 1.3 Mhz operation frequency, the converter can run at full power with a tiny 4.7 μH inductor. However, cares must be observed, at ESR level, to optimize the total DC/DC conversion efficiency. In particular, the ferrite material shall have limited eddy current losses at high frequency. Depending upon the type of material, the eddy losses in the inductor can range from a low 40 mW to a high 250 mW under the same bias and load conditions.

Table 6. RECOMMENDED INDUCTOR MANUFACTURERS

Manufacturers	Part Number
TDK	
COILCRAFT	LPO3310−472ML
MURATA	

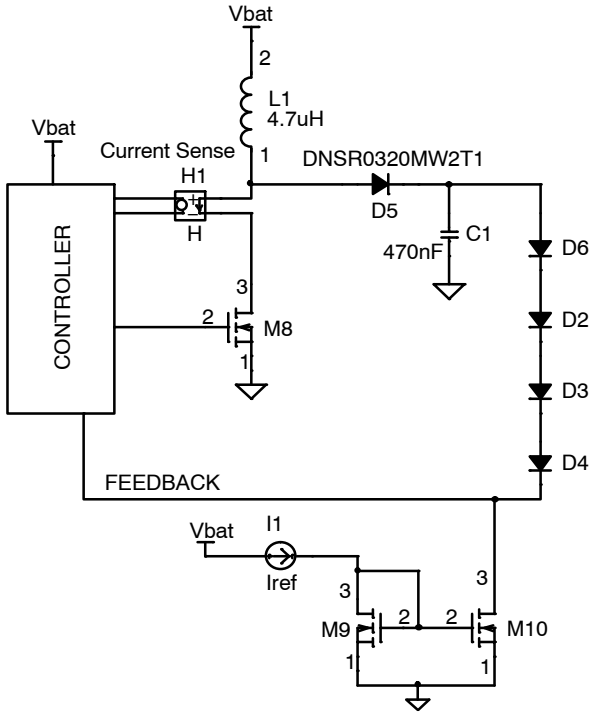


Figure 3. Basic Boost Structure

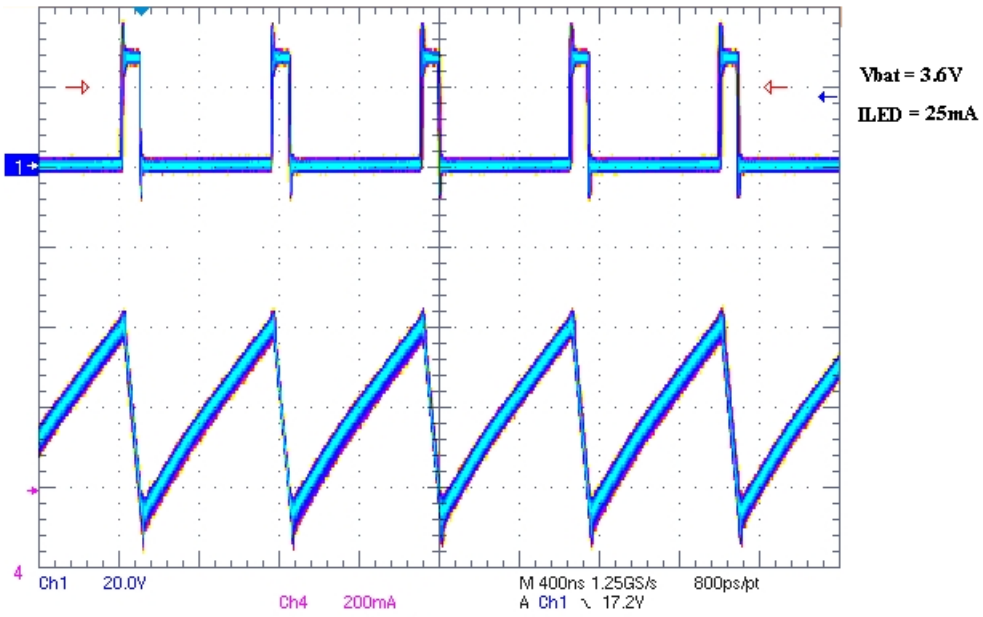


Figure 4. Typical Switching Operation

Although the total ohmic resistance plays an important role in the losses developed in the converter, the switching losses are key when the operating frequency is beyond a few kilohertz range. To minimize such losses, the internal power NMOS is designed to minimize the dI/dt, thus minimizing the I*V crossing time. As a consequence, the slope of the positive going voltage −VLX− present at the Lx pin is very fast as well and an overshoot is created since the Schottky rectifier has an intrinsic turn-on time: the voltage keeps going until the diode turns−on, clamping the VLX voltage at the output value. Such a mechanism is depicted in Figure 5. The proposed Schottky, depicted in the schematic Figure NO TAG, is a good alternative to minimize such an overshoot.

On the other hand, the same overshoot is propagated to the Vout voltage when the system operates under open load condition. As a consequence, it is strongly recommended to implement a simple filter, built with a small footprint resistor, to makes sure that no any uncontrolled operation of the high sensitive pin Vos will happen under the worst case conditions: see Figure 1, resistor R5.

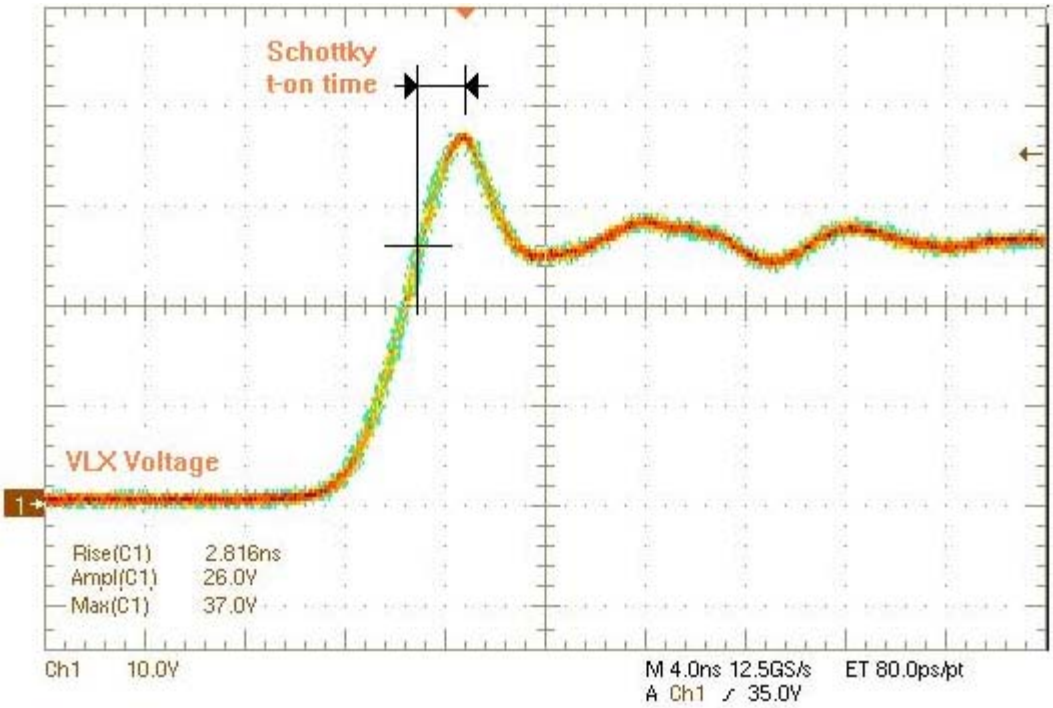


Figure 5. Typical Turn On Time of the Schottky Rectifier

I2C Protocol

The standard I2C protocol is used to transfer the data from the MCU to the NCP5021. Leaving aside the Acknowledge bit, the NCP5021 chip does not return data back to the MCU.

The physical address of the NCP5021 can be selected as 0111 001X or 0111 010X (the X being the Read / Write identifier as defined by the I2C specification) depending upon the digital status present at the I2CADR pin:

– I2CADR = Low → address = %0111 0010 = $72

– I2CADR = High → address = %0111 0100 = $74

In order to avoid any risk during the operation, the digital levels are intended to be hardwired either to GND or to Vbat prior to power up the system.

The first byte of the I2C frame shall be selected address ($72 or $74) when a Write is send to the chip.

To set up a new output current value, a full frame shall be send by the MCU. The frame contains three consecutive bytes and shall fulfill the I2C specifications (see Figure 6):

First byte:	I2C address, write	→ $72 (assuming I2CADR = Low)
Second byte:	register selection	→ %0000 0000 = internal register address
Third byte:	DATA	→ %0000 0000 = function / output current value

An infinite number of register selection / data pair can be send on the I2C port once the physical address has been decoded (see Figure 7). The transmission ends when the STOP signal is send by the SCL/SDA digital code.

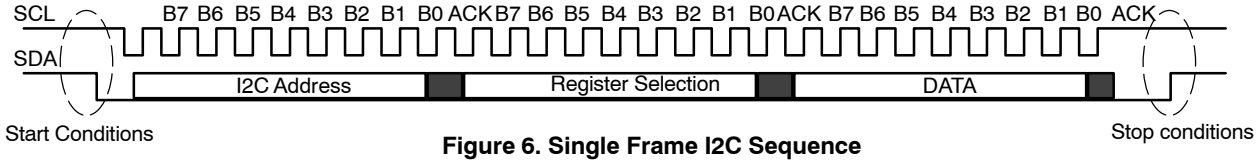


Figure 6. Single Frame I2C Sequence

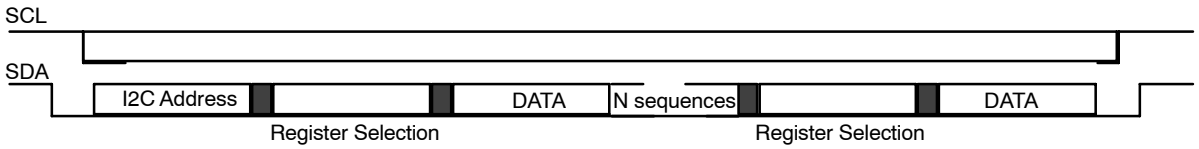


Figure 7. Multi Frames I2C Sequence

Registers Setup Selection

The register selection follows the I2C address of a new frame and must be followed by the DATA register. The content of the register selection byte is not stored into the chip and a new one shall be send for every DATA update. The low nibble contains the selected register number as depicted in Table 7. The high nibble is reserved for future use.

The last code $0F is reserved for ON Semiconductor to control the manufacturing test and access to this register is not permitted outside the ON Semiconductor final test facilities.

Table 7. REGISTER SELECTION CODE

$	B7	B6	B5	B4	B3	B2	B1	B0	
00	0	0	0	0	0	0	0	0	Shut Down the chip
01	0	0	0	0	0	0	0	1	Select I−LED current setup and immediate LED update
02	0	0	0	0	0	0	1	0	Set ILED target and Gradual Dimming UPWARD
03	0	0	0	0	0	0	1	1	Set ILED target and Gradual Dimming DOWNWD
04	0	0	0	0	0	1	0	0	Set timing and start the gradual dimming
05	0	0	0	0	0	1	0	1	Reserved for future use
06	0	0	0	0	0	1	1	0	Reserved for future use
07	0	0	0	0	0	1	1	1	Reserved for future use
08	0	0	0	0	1	0	0	0	Set up Photo sense input stage gain
09	0	0	0	0	1	0	0	1	Set up Photo Sense I−LED minimum value
0A	0	0	0	0	1	0	1	0	Set up Photo Sense up/down timing
0B	0	0	0	0	1	0	1	1	Reserved for future use
0C	0	0	0	0	1	1	0	0	Reserved for future use
0D	0	0	0	0	1	1	0	1	Reserved for future use
0E	0	0	0	0	1	1	1	0	Reserved for future use
0F	0	0	0	0	1	1	1	1	Reserved for manufacturing test: *do not access*

Table 8. REGISTERS IDENTIFICATION

DEC	Register Functions	Register Identification	Command
1	Shut Down the chip	SDN	$00
2	Select I−LED current setup and immediate LED update	ILEDREG[4..0]	$01
3	Select I−LED target Gradual Dimming command UP	GDIM[4..0]	$02
4	Select I−LED target Gradual Dimming command DOWN	GDIM[4..0]	$03
5	Set Timing & Start gradual Dimming Sequence	TDIM[4..0]	$04
6	Reserved for future use		
7	Reserved for future use		
8	Reserved for future use		
9	Set up Photo sense input stage gain	PHGAIN[4..0]	$08
10	Set up Photo Sense I−LED minimum value	PHMIN[3..0]	$09
11	Set up Photo Sense timing	PHCLK[5..0]	$0A
12	Reserved for future use		$0B
13	Reserved for future use		$0C
14	Reserved for future use		$0D
15	Reserved for future use		$0E
16	Reserved for manufacturing test: *do not access*	FTEST[7..0]	$0F

ILED Peak Current

The ILED peak current depends upon the reference current (I_{REF} pin) and the digital contain of the ILEDREG register. The I2C port is used to setup the ILED peak current stored into the ILEDREG register. The load current is derived from the 1144 mV reference voltage provided by the internal Band Gap associated to the external resistor connected across I_{REF} pin and Ground (see Figure 8). The maximum ILED current is given by the internal current mirror ratio (multiplier − k −) equal to 250. In other word, to get a 25 mA maximum, with a full $1F command, the reference current shall be 25 mA/250 = 100 μA. This current is used to calculate the resistor connected between the IREF pin and GND: R_{REF} = 1.144 / 100e−6 = 11.44 kΩ. In any case, no voltage shall be forced at I_{REF} pin, either downward or upward.

The tolerance of the external resistor must be 1% or better, with a 100 ppm thermal coefficient, to get the expected overall tolerance.

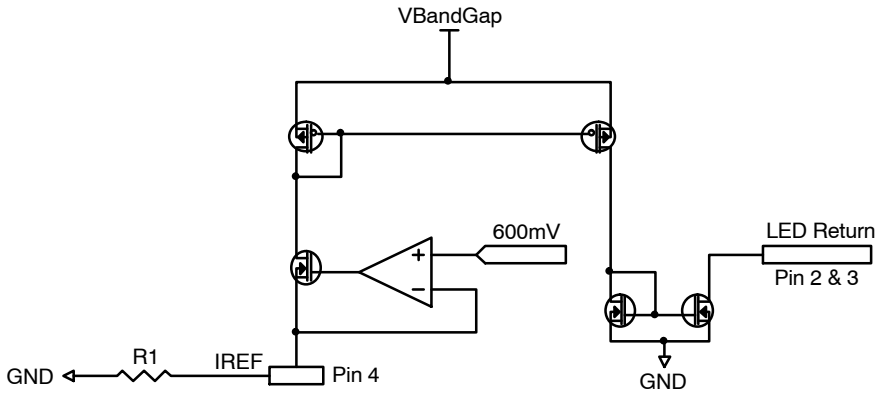


Figure 8. Basic Reference Current Source

NOTE: The I_{REF} pin must never be biased by an external voltage higher than 1.44 V.

The ILED current is given by Table 9 as a percentage of the maximum programmed ILED value (100% will give 25 mA when Iref = 100 μA).

Table 9. OUTPUT CURRENT PROGRAMMED VALUE (Iout % = F(Step))

$Step	Iout %	Step	Iout %	$Step	Iout %	$Step	Iout %
00	0.00	08	0.50	10	3.16	18	19.95
01	0.10	09	0.63	11	3.98	19	25.12
02	0.13	0A	0.79	12	5.01	1A	31.62
03	0.16	0B	1.00	13	6.31	1B	39.81
04	0.20	0C	1.26	14	7.94	1C	50.12
05	0.25	0D	1.58	15	10.00	1D	63.10
06	0.32	0E	2.00	16	12.59	1E	79.43
07	0.40	0F	2.51	17	15.85	1F	100.00

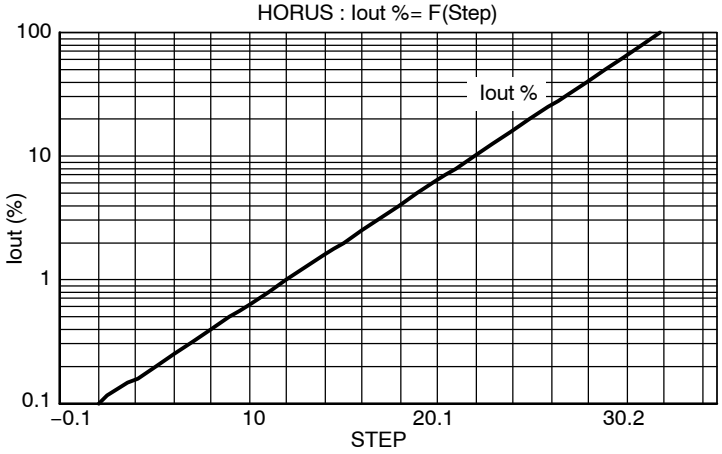


Figure 9. Typical ILED Programming Curve

ILEDREG[0..7] I−LED PEAK CURRENT

	B7	B6	B5	B4	B3	B2	B1	B0
step	0	0	0	ILED16	ILED8	ILED4	ILED2	ILED1
RESET	0	0	0	0	0	0	0	0

Bits [B7:B5] : Reserved for future use
Bits [B4:B0] : ILED peak current setup

Inductor Peak Current

The peak current flowing into the inductor during normal application is set up by the external resistor R_{PCA} connected between the I_{PK} pin and ground.

The maximum I_{PK} current is given by the internal current mirror ratio (multiplier − kk −) typically equal to 9700. In other word, to get a 750 mA maximum peak current in the inductor, the reference current shall be 750 mA/9700 = 79 μA. This current is used to calculate the resistor connected between the I_{PK} pin and GND: R_{REF} = 1.144 / 79e−6 = 14.4 kΩ.

The concept depicted in the ILED peak current paragraph applies as well and cares must be observed to avoid any voltage source connection to the IPK pin.

Gradual Dimming

The purpose of that function is to gradually Increase or Decrease the brightness of the backlight / keyboard LED upon command from the external MCU. The function is activated and controlled by means of the I2C protocol.

The period (either upward or downward) is equal to the time defined for each step, multiplied by the number of steps. The number of step is derived from the value associated with the target current.

To operate such a function, the MCU will provide three information:

1. The target current level (either upward or downward)
2. The time per step
3. The Upward or Downward mode of operation

When a new gradual dimming sequence is requested, the output current increases, according to the logarithmic curve, from the existing start value to the end value. The end current value is defined by the contain of the Upward or Downward register, the width of each step is defined by the third register, the number of step being in the 1 to 32 range ($00 to $1F). In the event of software error, the system checks that neither the maximum output current (25 mA), nor the zero level are forced out of their respective bounds. Similarly, software errors shall not force NCP5021 into an uncontrolled mode of operation.

The dimming is built with 32 steps and the time delay encoded into the third byte of the I2C transaction.

When the gradual dimming is not requested (register selection = $01), the output current is straightforwardly set up to the level defined by the contain of the related register upon acknowledge of the output current byte.

The gradual dimming sequence must be set up before a new output current data byte is send to NCP5021. At this point, the brightness sequence takes place when the new data byte is acknowledged by the internal I2C decoder. Since the six registers are loaded on independent byte flow associated to the I2C address, any parameter of the NCP5021 chip can be updated ahead of the next function.

Table 10. GDIMR[7..0] GRADUAL DIMMING TARGET

	B7	B6	B5	B4	B3	B2	B1	B0
ms	0	0	0	ILED5	ILED4	ILED3	ILED2	ILED1
RESET	0	0	0	0	0	0	0	0

Bits [B7:B5] : Reserved for future use
Bits [B4:B0] : ILED peak current setup or Gradual Dimming Timing

The number of step for a given sequence, depends upon the start and end output current range: since the IPEAK value is encoded in the ILEDREG [4:0] binary scale, a maximum of 31 steps is achievable during a gradual dimming operation.

To select the direction of the gradual dimming (either Upward or Downward), one shall send the appropriate register before to activate the sequence as depicted in the example here below:

First byte: = 0111 0000 → I2C address (assuming I2CADR = Low)
Second byte: = 0000 0010 → select an ILED target UPWARD sequence
Third byte: = 0000 1111 → set I−LED = 2.51% of the maximum range

First byte: = 0111 0000 → I2C address (assuming I2CADR = Low)
Second byte: = 0000 0100 → set Timing and start the sequence
Third byte: = 0000 0010 → set Timing per step = 20 ms / step

Table 11. TDIM[7.0] GRADUAL DIMMING TIME PER STEP

	B7	B6	B5	B4	B3	B2	B1	B0
ms	0	0	0	160	80	40	20	10
RESET	0	0	0	0	0	0	0	0

Bits [B7:B5] : Reserved for future use
Bits [B4:B0] : Gradual Dimming Timing

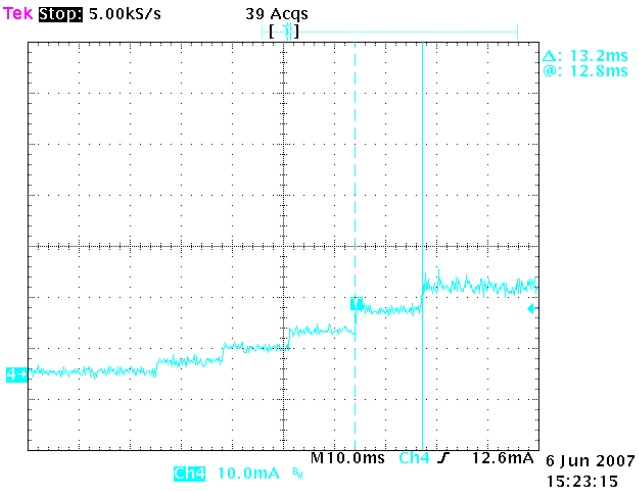


Figure 10. Typical Gradual Dimming UPWARD

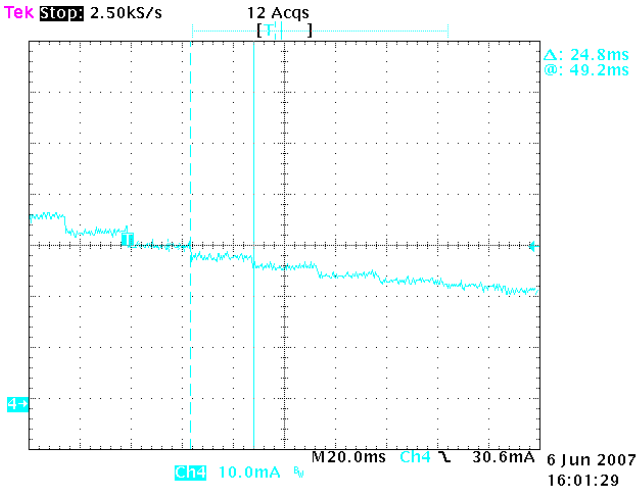


Figure 11. Typical Gradual Dimming DOWNWARD

Backlight Dimming

The built−in I2C interface provides a simple way to accurately control the output peak current flowing in the LED. The internal register ILEDREG[7:0] is set up by the content of the SDA byte send by the external MCU. For typical application, the 100 μA reference current forced by the external resistor yields a 25 mA maximum in the output LED. The waveforms given on illustrate a normal programming sequence.

Table 12. ILEDREG[0..7]

	B7	B6	B5	B4	B3	B2	B1	B0
step	0	0	0	ILED16	ILED8	ILED4	ILED2	ILED1
RESET	0	0	0	0	0	0	0	0

[B7:B6] = Reserved for future use
[B4..B0] = Output LED mA/step current. The content of these bits is latched to the current reference on the 8th SCL clock pulse.

Ambient Light Control

The ambient light can be monitored, by an extra photo diode, to automatically adjust the I−LED peak current as a function of the ambient light. A dedicated I2C command is used to activated or de−activated this function. On the other hand, the end user shall set up the maximum I−LED current by means of an I2C command. The photo sense is automatically de−activated when an I2C command is send through the port, and resume to the pre−programmed status when the I2C command is completed.

The concept is based on analog monitoring of the I−LED current and the photo sense feedback, associated to a Up/Down counter to properly setup the contrast at display level. The photo sense action is bounded by two limits:

1. upper I−LED as defined by the en user : the photo sense cannot increase the I−LED above such a limit
2. lower I−LED as defined by the en user : the photo sense cannot reduce the back light current to zero.

When the photo sense activates the counter (in either direction), a selectable low frequency clock drive the counter, yielding a smooth and slow brightness variation.

The 100 Hz noise, coming from the standard fluorescent tubes, is filter out by means of an external network built between the photo sensor and the AMBS pin. Generally speaking, such a filter is built with a RC network designed to cope with the electrical performances of the selected photo sense. As a consequence, the AMBS pin is biased by a low level voltage signal and processed accordingly the ambient light control structure: see Figure 15.

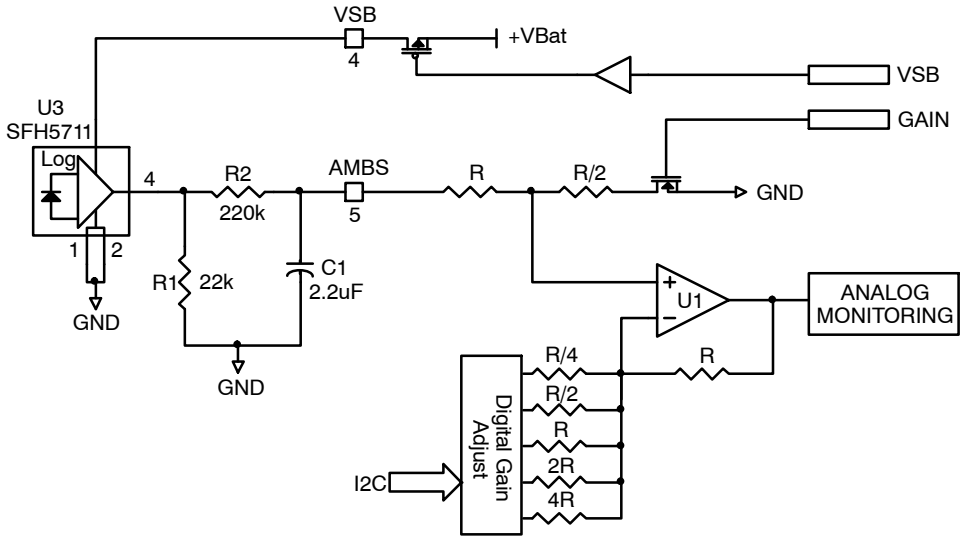


Figure 12. Basic Photo Sense Input Circuit

Since several type of photo sensor can be used in the final application, provisions have been taken into account to dynamically adjust the gain of the photo current. Such capability is carried out by the internal register loaded through the I2C port.

Table 13. PHGAIN[0..7]

	B7	B6	B5	B4	B3	B2	B1	B0
	VSD	0	0	PHG5	PHG4	PHG3	PHG2	PHG1
RESET	0	0	0	0	0	0	0	0

Bit [B7] : Photo sense VSD bias control
B7 = 0 → VSD disconnected, photo sense function de−activated
B7 = 1 → VSD connected, photo sense function activated
Bits [B6:B5] : RFU
Bits [B4:B0] : Photo sensor gain adjust

When the photo sense returns a lower ambient light level in comparison to the maximum level set up by the user, the I−LED decreases with a timing defined by an I2C command. Such a timing is derived from the Low Frequency clock and selected by the PHTIM register (see Figure 13).

Table 14. PHCLK[0..7]

	B7	B6	B5	B4	B3	B2	B1	B0
	PHTT	0	PHT6	PHT5	PHT4	PHT3	PHT2	PHT1
RESET	0	0	0	0	0	0	0	0

Bits [B7] : RFU
Bits [B6] : RFU
Bits [B5:B0] :

PHT1 = Photo sense clock = 25 Hz → T = 40 ms/step

PHT2 = Photo sense clock = 12 Hz → T = 80 ms/step

PHT3 = Photo sense clock = 6 Hz → T =160 ms/step

PHT4 = Photo sense clock = 3 Hz → T = 320 ms/step

PHT5 = Photo sense clock = 1.5 Hz → T = 640 ms/step

PHT6 = Photo sense clock = 0.7 MHz → T = 1280 ms/step

PHTT = Photo sense clock = 1.7 MHz → T = 560 ns/step → reserved for test purpose

NOTE: The bits cannot be combined to generate a different timing.

The PHTT bit is reserved for ON Semiconductor test purposes and shall not be asserted High by the end user outside the ON Semiconductor final test facilities. When the PHTT is asserted High, the I−LED jumps instantaneously from the previous level to the end value.

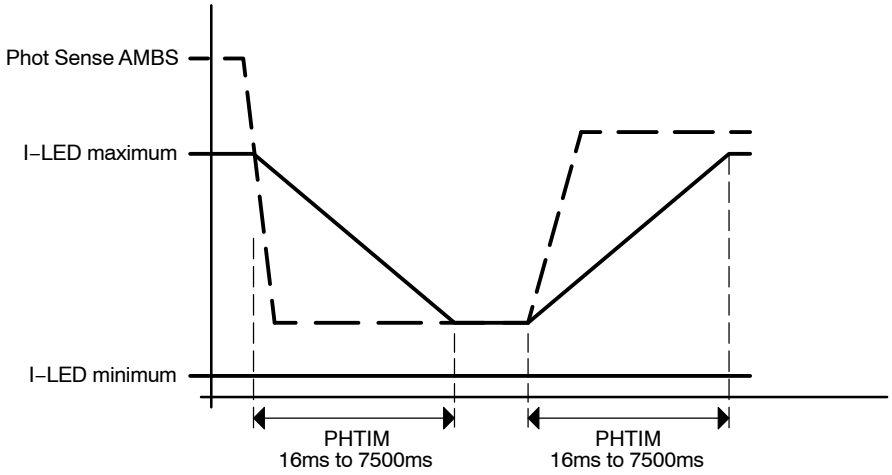


Figure 13. Basic Photo Sense Timing

The rise and fall time of the I−LED current are programmable (according to the PHTIM register contain) and identical. The timing is defined by the PHTIM[B4:B0] bits multiplied by the number of steps necessary to reduce / increase the I−LED form one value to the next limit.

On the other hand, the I−LED cannot be reduce to zero during the Photo sense operation: the contain of the PHMIN[B2:B0] register limits the low end current when the photo sensor is in a dark environment.

Table 15. PHMIM[0..7]

	B7	B6	B5	B4	B3	B2	B1	B0
	0	0	0	0	PHM4	PHM3	PHM2	PHM1
RESET	0	0	0	0	0	0	0	0

Bits [B7:B4] : RFU
Bits [B3:B0] : set up the I−LED minimum value, according to the logarithmic table.

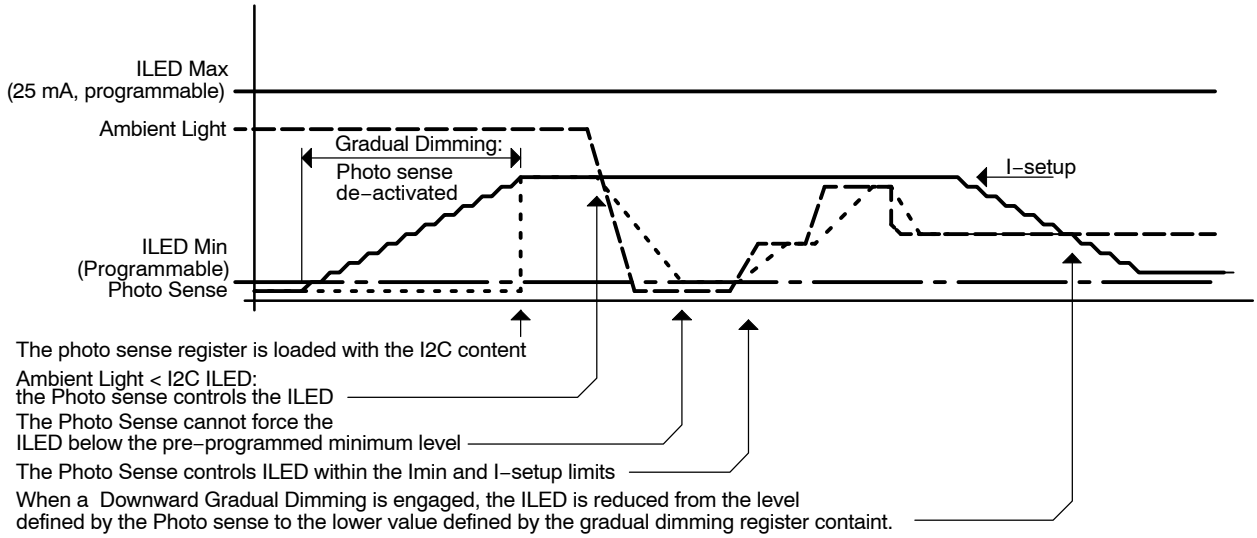


Figure 14. Basic Gradual Dimming and Photo Sense Operation Strategy

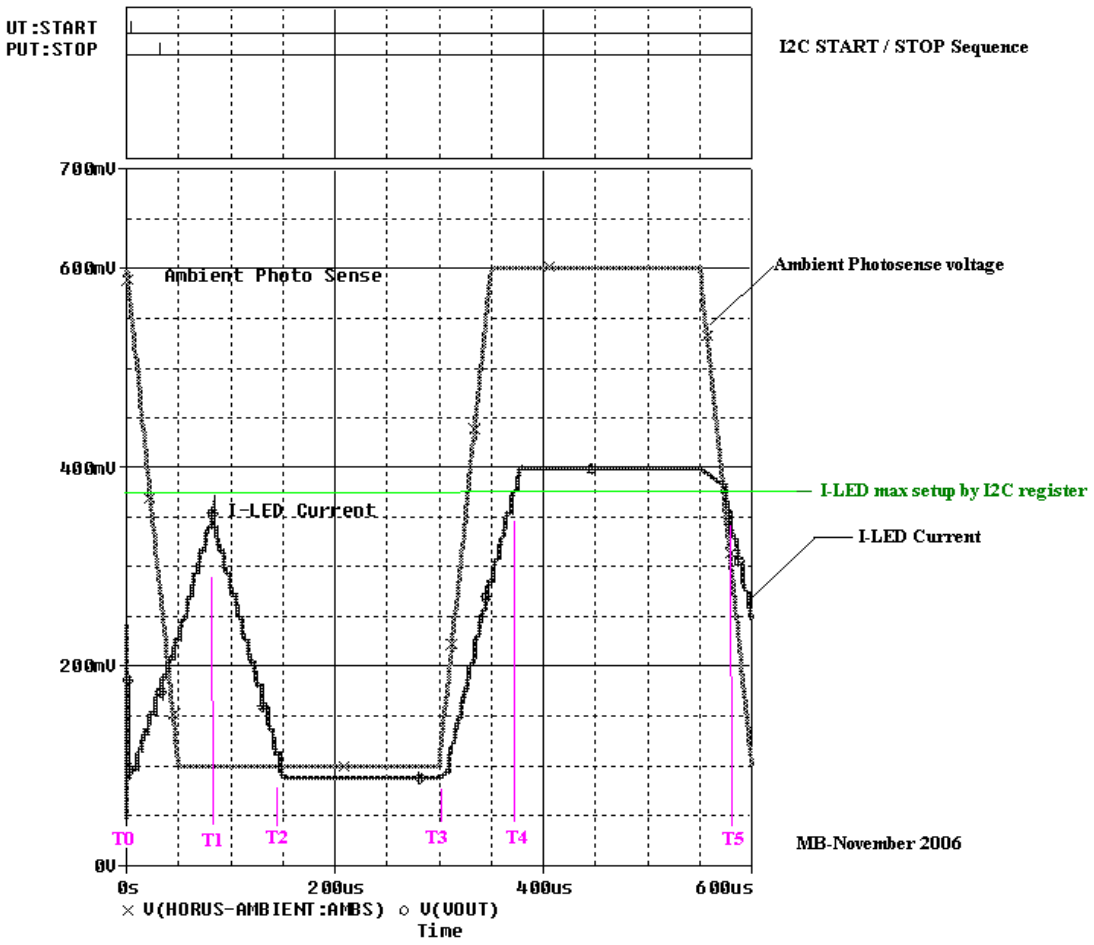
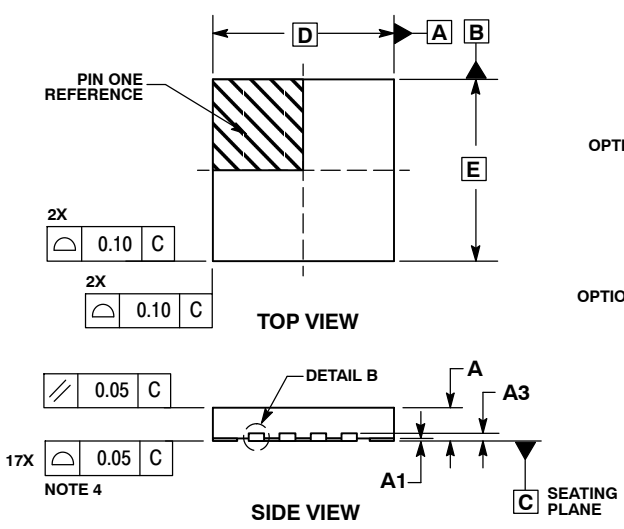


Figure 15. Basic Ambient Photo Sense Regulation (PSPICE Simulation)

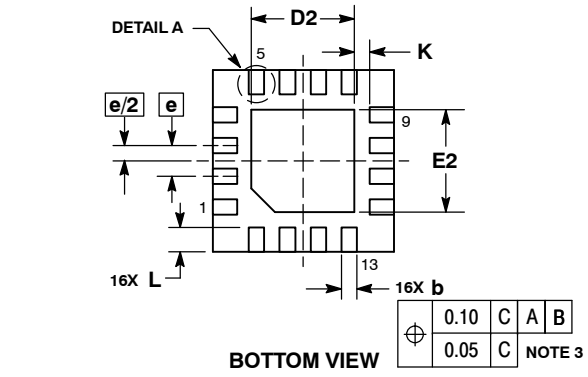
PACKAGE DIMENSIONS

UQFN16 3x3, 0.5P
CASE 523AF−01
ISSUE A

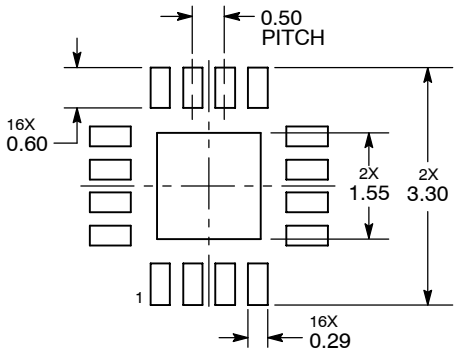


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.20	0.30
D	3.00 BSC	
D2	1.60	1.80
E	3.00 BSC	
E2	1.60	1.80
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50



SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your loca
Sales Representative