

# XPHASE™ VR 10/11 CONTROL IC

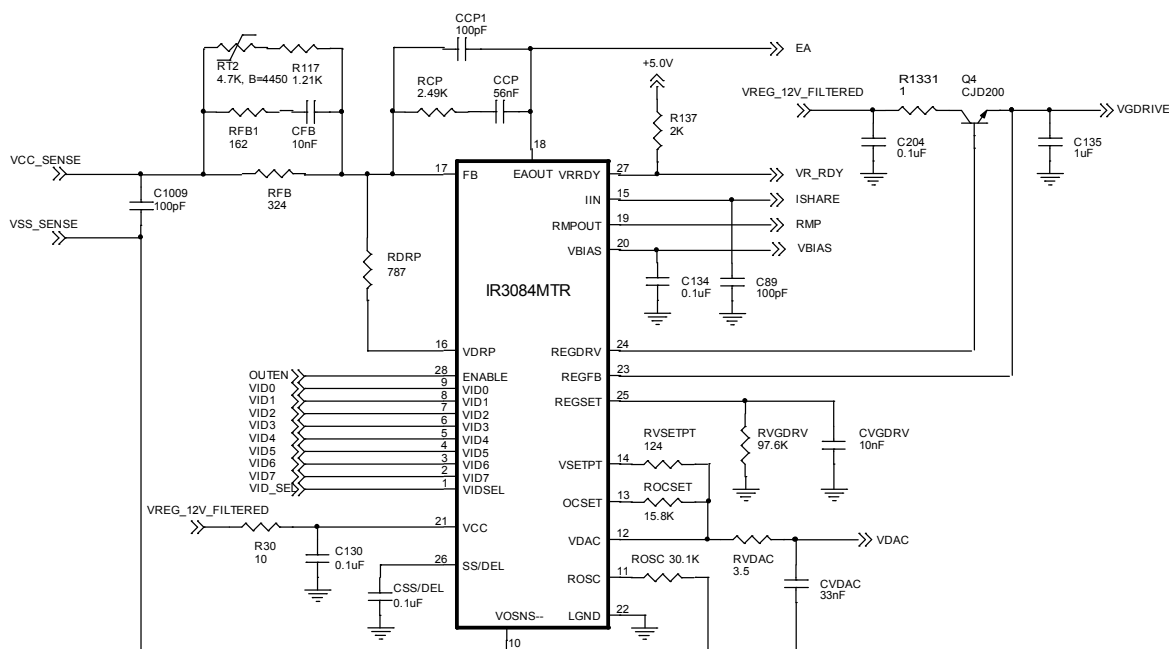
## DESCRIPTION

The IR3084 Control IC combined with an IR *XPhase*<sup>™</sup> Phase IC provides a full featured and flexible way to implement a complete VR10 or VR11 power solution. The “Control” IC provides overall system control and interfaces with any number of “Phase” ICs which each drive and monitor a single phase of a multiphase converter. The *XPhase*<sup>™</sup> architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

## FEATURES

- 1 to X phase operation with matching Phase IC
- Supports both VR11 8-bit VID code and extended VR10 7-bit VID code
- 0.5% Overall System Setpoint Accuracy
- VID Select pin sets the DAC to either VR10 or VR11
- VID Select pin selects either VR11 or legacy VR10 type startups
- Programmable VID offset and Load Line output impedance
- Programmable VID offset function at the Error Amp's non-inverting input allowing zero offset
- Programmable Dynamic VID Slew Rate
- $\pm 300\text{mV}$  Differential Remote Sense
- Programmable 150kHz to 1MHz oscillator
- Enable Input with 0.85V threshold and 100mV of hysteresis
- VR Ready output provides indication of proper operation and avoids false triggering
- Phase IC Gate Driver Bias Regulator / VRHOT Comparator
- Operates from 12V input with 9.9V Under-Voltage Lockout
- 6.9V/6mA Bias Regulator provides System Reference Voltage
- Programmable Hiccup Over-Current Protection with Delay to prevent false triggering
- Small thermally enhanced 5mm x 5mm, 28 pin MLPQ package

## TYPICAL APPLICATION CIRCUIT



## ORDERING INFORMATION

| DEVICE       | ORDER QUANTITY     |
|--------------|--------------------|
| IR3084MTRPBF | 3000 Tape and Reel |
| IR3084MPBF   | 100 Piece Strip    |

## ABSOLUTE MAXIMUM RATINGS

Operating Junction Temperature.....0 to 150°C  
Storage Temperature Range.....-65°C to 150°C  
ESD Rating.....HBM Class 1B JEDEC standard  
Moisture Sensitivity Level.....JEDEC Level 3 @ 260 °C

| PIN # | PIN NAME | V <sub>MAX</sub> | V <sub>MIN</sub> | I <sub>SOURCE</sub> | I <sub>SINK</sub> |
|-------|----------|------------------|------------------|---------------------|-------------------|
| 1     | VIDSEL   | 20V              | -0.3V            | 1mA                 | 1mA               |
| 2-9   | VID7-0   | 20V              | -0.3V            | 1mA                 | 1mA               |
| 10    | VOSNS-   | 0.5V             | -0.5V            | 10mA                | 10mA              |
| 11    | ROSC     | 20V              | -0.5V            | 1mA                 | 1mA               |
| 12    | VDAC     | 20V              | -0.3V            | 1mA                 | 1mA               |
| 13    | OCSET    | 20V              | -0.3V            | 1mA                 | 1mA               |
| 14    | VSETPT   | 20V              | -0.3V            | 1mA                 | 1mA               |
| 15    | IIN      | 20V              | -0.3V            | 1mA                 | 1mA               |
| 16    | VDRP     | 20V              | -0.3V            | 5mA                 | 5mA               |
| 17    | FB       | 20V              | -0.3V            | 1mA                 | 1mA               |
| 18    | EAOUT    | 10V              | -0.3V            | 20mA                | 20mA              |
| 19    | RMPOUT   | 20V              | -0.3V            | 5mA                 | 5mA               |
| 20    | VBIAS    | 20V              | -0.3V            | 50mA                | 10mA              |
| 21    | VCC      | 20V              | -0.3V            | 1mA                 | 50mA              |
| 22    | LGND     | n/a              | n/a              | 50mA                | 1mA               |
| 23    | REGFB    | 20V              | -0.3V            | 1mA                 | 1mA               |
| 24    | REGDRV   | 20V              | -0.3V            | 10mA                | 50mA              |
| 25    | REGSET   | 20V              | -0.3V            | 1mA                 | 1mA               |
| 26    | SS/DEL   | 20V              | -0.3V            | 1mA                 | 1mA               |
| 27    | VRRDY    | 20V              | -0.3V            | 1mA                 | 20mA              |
| 28    | ENABLE   | 20V              | -0.3V            | 1mA                 | 1mA               |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over:  $9.5V \leq V_{CC} \leq 16V$ ,  $-0.3V \leq V_{OSNS} \leq 0.3V$ ,  $0^\circ C \leq T_J \leq 100^\circ C$ ,  $ROSC = 24k\Omega$ ,  $CSS/DEL = 0.1\mu F \pm 10\%$

| PARAMETER                                                                                                              | TEST CONDITION                                                                                          | MIN  | TYP  | MAX   | UNIT       |
|------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|------|------|-------|------------|
| <b>VDAC REFERENCE</b>                                                                                                  |                                                                                                         |      |      |       |            |
| System Set-Point Accuracy<br>(Deviation from Tables 1 & 2 per test circuit in Figure 1 which emulates in-VR operation) | $VID \geq 1V$ , $10k\Omega \leq ROSC \leq 100k\Omega$ , $25^\circ C \leq T_J \leq 100^\circ C$          | -0.5 |      | 0.5   | %          |
|                                                                                                                        | $0.8V \leq VID < 1V$ , $10k\Omega \leq ROSC \leq 100k\Omega$ , $25^\circ C \leq T_J \leq 100^\circ C$   | -5   |      | +5    | mV         |
|                                                                                                                        | $0.5V \leq VID < 0.8V$ , $10k\Omega \leq ROSC \leq 100k\Omega$ , $25^\circ C \leq T_J \leq 100^\circ C$ | -8   |      | +8    | mV         |
| Source Current                                                                                                         | Includes OCSET and VSETPT currents                                                                      | 104  | 113  | 122   | $\mu A$    |
| Sink Current                                                                                                           | Includes OCSET and VSETPT currents                                                                      | 92   | 100  | 108   | $\mu A$    |
| VIDx Input Threshold                                                                                                   |                                                                                                         | 500  | 600  | 700   | mV         |
| VIDx & VIDSEL Input Bias Current                                                                                       | $0V \leq VIDx \leq V_{CC}$                                                                              | -5   | 0    | 5     | $\mu A$    |
| VIDx 11111x Blanking Delay                                                                                             | Measure Time till VRRDY drives low, Note 1                                                              | 0.5  | 1.3  | 2.1   | $\mu s$    |
| VIDSEL Pull-up Voltage                                                                                                 | VIDSEL FLOATING                                                                                         | 1.15 | 1.25 | 1.35  | V          |
| VIDSEL Pull-up Resistance                                                                                              |                                                                                                         | 5.0  | 12.5 | 20.0  | K $\Omega$ |
| VIDSEL VR10/VR11 Threshold                                                                                             |                                                                                                         | 0.55 | 0.62 | 0.69  | V          |
| VIDSEL VR11 No Boot Threshold                                                                                          |                                                                                                         | 3.0  | 3.5  | 4.0   | V          |
| VIDSEL VR10 No Boot Threshold                                                                                          |                                                                                                         | 7.0  | 7.5  | 8.0   | V          |
| <b>ERROR AMPLIFIER</b>                                                                                                 |                                                                                                         |      |      |       |            |
| Input Offset Voltage                                                                                                   | Measure $V(FB) - V(VSETPT)$ per test circuit in Figure 1. Applies to TBS VID codes. Note 2.             | -5   | 0.0  | 5     | mV         |
| FB Bias Current                                                                                                        |                                                                                                         | -1   | -0.3 | 0.5   | $\mu A$    |
| VSETPT Bias Current                                                                                                    |                                                                                                         | 48.5 | 51   | 53.5  | $\mu A$    |
| DC Gain                                                                                                                | Note 1                                                                                                  | 90   | 100  | 110   | dB         |
| Gain Bandwidth Product                                                                                                 | Note 1                                                                                                  | 6    | 10   |       | MHz        |
| Corner Frequency                                                                                                       | 45 deg Phase Shift, Note 1                                                                              |      | 200  | 400   | Hz         |
| Slew Rate                                                                                                              | Note 1                                                                                                  | 1.4  | 3.2  | 5     | V/ $\mu s$ |
| Source Current                                                                                                         |                                                                                                         | -1.2 | -0.8 | -0.35 | mA         |
| Sink Current                                                                                                           |                                                                                                         | 0.5  | 1.0  | 1.7   | mA         |
| Max Voltage                                                                                                            | VBIAS-VEAOUT (ref. to VBIAS)                                                                            | 150  | 375  | 600   | mV         |
| Min Voltage                                                                                                            | Normal operation or Fault mode                                                                          | 30   | 110  | 200   | mV         |
| <b>VDRP BUFFER AMPLIFIER</b>                                                                                           |                                                                                                         |      |      |       |            |
| Input Offset Voltage                                                                                                   | $V(VDRP) - V(IIN)$ , $0.5V \leq V(IIN) \leq 5V$                                                         | -10  | -1   | 6     | mV         |
| Source Current                                                                                                         | $0.5V \leq V(IIN) \leq 5V$                                                                              | -9   | -7.3 | -4    | mA         |
| Sink Current                                                                                                           | $0.5V \leq V(IIN) \leq 5V$                                                                              | 0.2  | 0.88 | 4.1   | mA         |
| Bandwidth (-3dB)                                                                                                       | Note 1                                                                                                  | 1    | 6    |       | MHz        |
| Slew Rate                                                                                                              | Note 1                                                                                                  | 5    | 10   |       | V/ $\mu s$ |

| PARAMETER                                | TEST CONDITION                                                       | MIN   | TYP  | MAX   | UNIT  |
|------------------------------------------|----------------------------------------------------------------------|-------|------|-------|-------|
| <b>CURRENT SENSE INPUT</b>               |                                                                      |       |      |       |       |
| IIN Bias Current                         | V(SS/DEL) > 0.85V, V(EAOUT) > 0.5V                                   | -2.0  | -0.2 | 1.0   | μA    |
| IIN Preconditioning Pull-Down Resistance | V(SS/DEL) < 0.35V                                                    | 5.6   | 12.5 | 19.4  | KΩ    |
| IIN Preconditioning RESET Threshold      | V(EAOUT)                                                             | 0.20  | 0.35 | 0.50  | V     |
| IIN Preconditioning SET Threshold        | V(SS/DEL)                                                            | 0.35  | 0.60 | 0.85  | V     |
| <b>VBIAS REGULATOR</b>                   |                                                                      |       |      |       |       |
| Output Voltage                           | -5mA ≤ I(VBIAS) ≤ 0mA                                                | 6.6   | 6.9  | 7.2   | V     |
| Current Limit                            |                                                                      | -35   | -20  | -6    | mA    |
| <b>Over-Current Comparator</b>           |                                                                      |       |      |       |       |
| Input Offset Voltage                     | 1V ≤ V(OCSET) ≤ 5V                                                   | -10   | -1   | 10    | mV    |
| OCSET Bias Current                       |                                                                      | -53.5 | -51  | -48.5 | μA    |
| <b>SOFT START AND DELAY</b>              |                                                                      |       |      |       |       |
| Start Delay (TD1)                        | RDRP = ∞                                                             | 1.2   | 1.8  | 2.6   | ms    |
| Soft Start Time (TD2)                    | RDRP = ∞                                                             | 0.8   | 1.6  | 2.8   | ms    |
| VID Sample Delay (TD3)                   |                                                                      | 0.2   | 1.0  | 2.5   | ms    |
| VRRDY Delay (TD4 + TD5)                  |                                                                      | 0.5   | 1.3  | 2.2   | ms    |
| OC Delay Time                            | Note 1                                                               | 150   | 250  | 350   | μs    |
| SS/DEL to FB Input Offset Voltage        | With FB = 0V, adjust V(SS/DEL) until EAOUT drives high               | 0.85  | 1.3  | 1.5   | V     |
| SS/DEL Charge Current                    |                                                                      | 40    | 70   | 100   | μA    |
| SS/DEL Discharge Current                 |                                                                      | 4     | 6.5  | 9     | μA    |
| Charge/Discharge Current Ratio           |                                                                      | 9.5   | 11.2 | 12.5  | μA/μA |
| OC Discharge Current                     | Note 1                                                               | 20    | 40   | 60    | μA    |
| Charge Voltage                           |                                                                      | 3.6   | 3.85 | 4.1   | V     |
| OC/VRRDY Delay Comparator Threshold      | Relative to Charge Voltage, SS/DEL rising                            |       | 80   |       | mV    |
| OC/VRRDY Delay Comparator Threshold      | Relative to Charge Voltage, SS/DEL falling                           |       | 100  |       | mV    |
| Delay Comparator Hysteresis              |                                                                      |       | 20   |       | mV    |
| VID Sample Delay Comparator Threshold    |                                                                      |       | 3.10 |       | V     |
| SS/DEL Discharge Comparator Threshold    |                                                                      |       | 215  |       | mV    |
| <b>ENABLE INPUT</b>                      |                                                                      |       |      |       |       |
| Threshold Voltage                        | ENABLE rising                                                        | 775   | 850  | 925   | mV    |
| Threshold Voltage                        | ENABLE falling                                                       | 675   | 750  | 825   | mV    |
| Threshold Hysteresis                     |                                                                      | 60    | 100  | 140   | mV    |
| Input Resistance                         |                                                                      | 50    | 100  | 200   | KΩ    |
| Blanking Time                            | Noise Pulse < 250ns will not register an ENABLE state change. Note 1 | 75    | 250  | 400   | ns    |



## PIN DESCRIPTIONS

| PIN# | PIN SYMBOL | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1    | VIDSEL     | Selects the DAC table and the type of Soft Start. There are 4 possible modes of operation: (1) GND selects VR10 DAC and VR11 type startup, (2) FLOAT (1.25V) selects VR11 DAC and VR11 type startup, (3) VBIAS (6.9V) selects VR11 DAC and legacy VR10 type startup, (4) VCC (12V) selects VR10 DAC and legacy VR10 type startup. Additional details are provided in the Theory of Operation section.                                           |
| 2-9  | VID7-0     | Inputs to the D to A Converter. Must be connected to an external pull-up resistor.                                                                                                                                                                                                                                                                                                                                                              |
| 10   | VOSNS-     | Remote Sense Input. Connect to ground at the Load.                                                                                                                                                                                                                                                                                                                                                                                              |
| 11   | ROSC       | Connect a resistor to VOSNS- to program oscillator frequency and OCSET, VSETPT, REGSET, and VDAC bias currents                                                                                                                                                                                                                                                                                                                                  |
| 12   | VDAC       | Regulated voltage programmed by the VID inputs. Connect an external RC network to VOSNS- to program Dynamic VID slew rate and provide compensation for the internal Buffer Amplifier.                                                                                                                                                                                                                                                           |
| 13   | OCSET      | Programs the hiccup over-current threshold through an external resistor tied to VDAC and an internal current source. Over-current protection can be disabled by connecting a resistor from this pin to VDAC to program the threshold higher than the possible signal into the IIN pin from the Phase ICs but no greater than 5V (do not float this pin as improper operation will occur).                                                       |
| 14   | VSETPT     | Error Amp non-inverting input. Converter output voltage can be decreased from the VDAC (VID) voltage with an external resistor connected to VDAC and an internal current sink. Current sensing and PWM operation are referenced to this pin.                                                                                                                                                                                                    |
| 15   | IIN        | Current Sense input from the Phase ICs. Prior to startup, SS/DEL<0.6V, this pin is pulled low by a 12.5K resistor to disable current balancing in the Phase ICs. When SS/DEL>0.6V and EAOOUT>0.35V, this pin is released and current balancing is enabled. If current feedback from the Phase ICs is not required for implementing droop or over-current protection connect this pin to LGND. To ensure proper operation do not float this pin. |
| 16   | VDRP       | Buffered IIN signal. Connect an external RC network to FB to program converter output impedance                                                                                                                                                                                                                                                                                                                                                 |
| 17   | FB         | Inverting input to the Error Amplifier.                                                                                                                                                                                                                                                                                                                                                                                                         |
| 18   | EAOOUT     | Output of the Error Amplifier. When Low, provides UVL function to the Phase ICs.                                                                                                                                                                                                                                                                                                                                                                |
| 19   | RMPOUT     | Oscillator Output voltage. Used by Phase ICs to program Phase Delay                                                                                                                                                                                                                                                                                                                                                                             |
| 20   | VBIAS      | 6.9V/6mA Regulated output used as a system reference voltage for internal circuitry and the Phase ICs.                                                                                                                                                                                                                                                                                                                                          |
| 21   | VCC        | Power Input for internal circuitry                                                                                                                                                                                                                                                                                                                                                                                                              |
| 22   | LGND       | Local Ground for internal circuitry and IC substrate connection                                                                                                                                                                                                                                                                                                                                                                                 |
| 23   | REGFB      | Inverting input of the Bias Regulator Error Amp. Connect to the out put of the Phase IC Gate Driver Bias Regulator.                                                                                                                                                                                                                                                                                                                             |
| 24   | REGDRV     | Output of the Bias Regulator Error Amp.                                                                                                                                                                                                                                                                                                                                                                                                         |
| 25   | REGSET     | Non-inverting input of the Bias Regulator Error Amp. Output Voltage of the Phase IC Gate Driver Bias Regulator is set by an internal current source flowing into an external resistor connected between this pin and ground.                                                                                                                                                                                                                    |
| 26   | SS/DEL     | Controls Converter Start-up and Over-Current Timing. Connect an external capacitor to LGND to program.                                                                                                                                                                                                                                                                                                                                          |
| 27   | VRRDY      | Open Collector output that drives low during Start-Up and any external fault condition. Connect external pull-up.                                                                                                                                                                                                                                                                                                                               |
| 28   | ENABLE     | Enable Input. A logic low applied to this pin puts the IC into Fault mode. This pin has a 100K pull-down resistor to GND.                                                                                                                                                                                                                                                                                                                       |



## PWM Control Method

The PWM block diagram of the *XPhase*<sup>TM</sup> architecture is shown in Figure 3. Feed-forward voltage mode control with trailing edge modulation is used. A high-gain wide-bandwidth voltage type error amplifier in the Control IC is used for the voltage control loop. An external RC circuit connected to the input voltage and ground is used to program the slope of the PWM ramp and to provide the feed-forward control at each phase. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to drops in the PCB related to changes in load current.

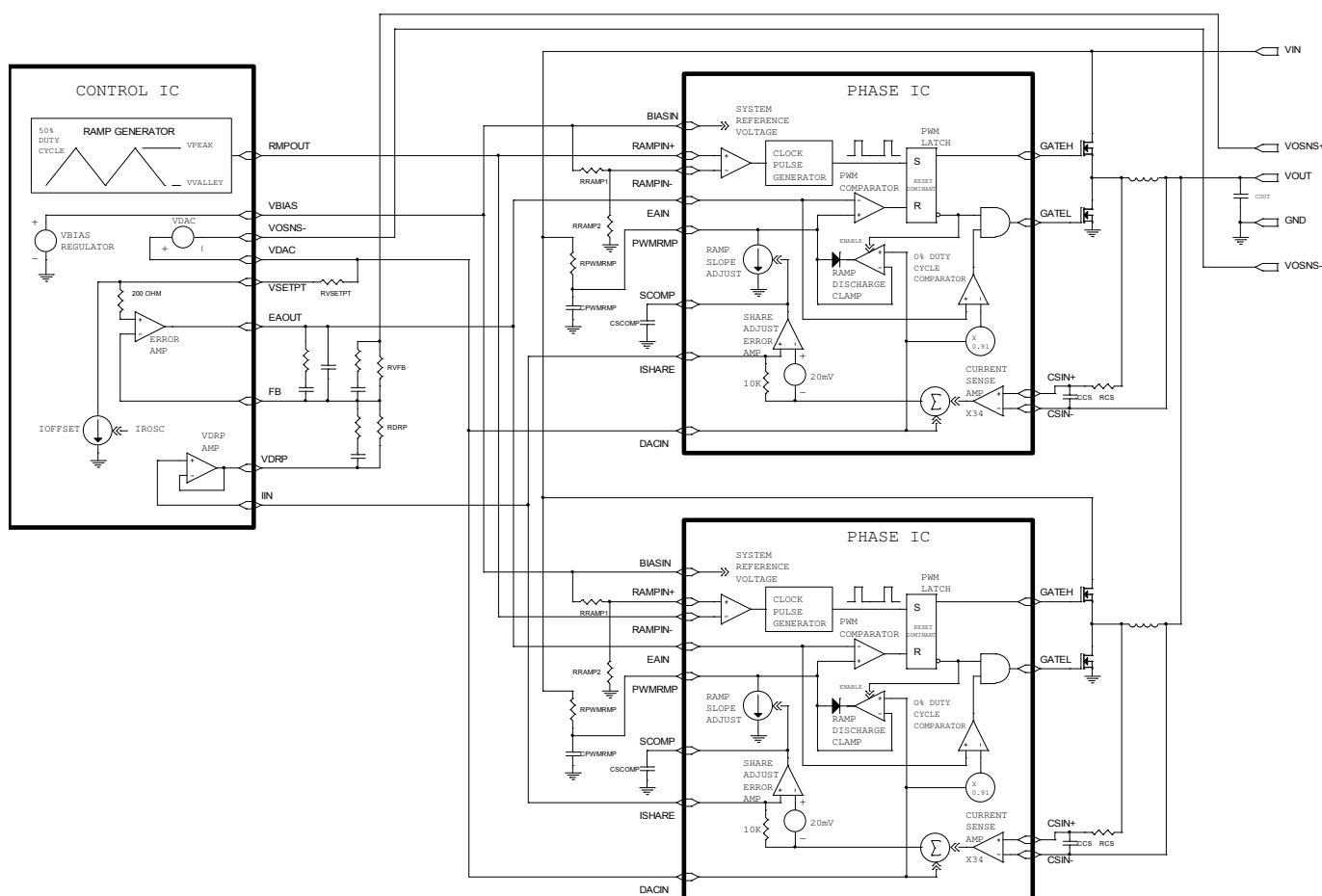


Figure 3 – IR3084 PWM Block Diagram

## Frequency and Phase Timing Control

The oscillator is located in the Control IC and its frequency is programmable from 150kHz to 1MHz by an external resistor. The output of the oscillator is a 50% duty cycle triangle waveform with peak and valley voltages of approximately 4.8V and 0.9V. This signal is used to program both the switching frequency and phase timing of the Phase ICs. The Phase IC is programmed by resistor divider RRAMP1 and RRAMP2 connected between the VBIAS reference voltage and the Phase IC LGND pin. A comparator in the Phase ICs detects the crossing of the oscillator waveform with the voltage generated by the resistor divider and triggers a clock pulse that starts the PWM cycle. The peak and valley voltages track the VBIAS voltage reducing potential Phase IC timing errors. Figure 4 shows the Phase timing for an 8 phase converter. Note that both slopes of the triangle waveform can be used for synchronization by swapping the RAMP + and – pins.

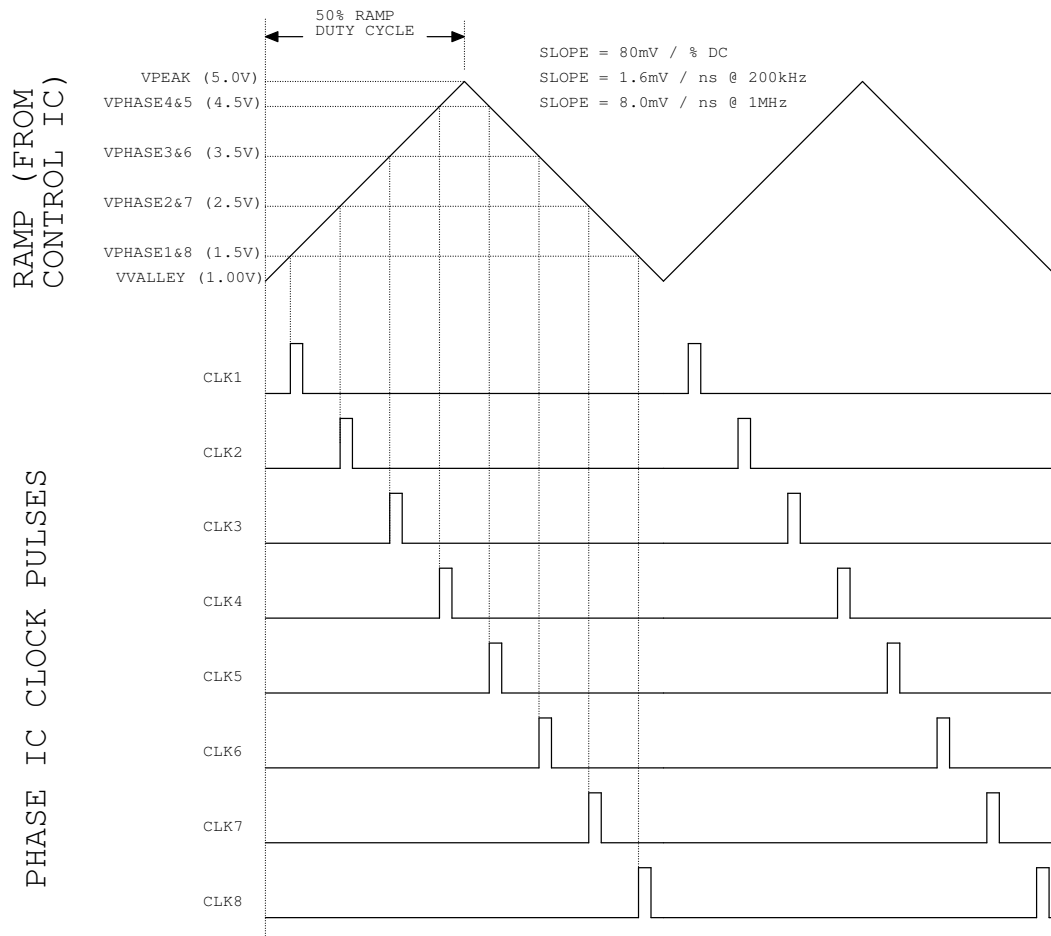


Figure 4 – 8 Phase Oscillator Waveforms

## PWM Operation

The PWM comparator is located in the Phase IC. Upon receiving a clock pulse, the PWM latch is set, the PWMRMP voltage begins to increase, the low side driver is turned off, and the high side driver is then turned on. When the PWMRMP voltage exceeds the Error Amp's output voltage the PWM latch is reset. This turns off the high side driver, turns on the low side driver, and activates the Ramp Discharge Clamp. The clamp quickly discharges the PWMRMP capacitor to the VDAC voltage of the Control IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An Error Amp output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the Error Amp is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide "single cycle transient response" where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC.

### Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / V_{out}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from  $V_{out}$  to  $V_{out} + V_{BODY DIODE}$ . The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / (V_{out} + V_{BODY DIODE})$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as “body braking” and is accomplished through the “0% Duty Cycle Comparator” located in the Phase IC. If the Error Amp's output voltage drops below 91% of the VDACC voltage this comparator turns off the low side gate driver.

Figure 5 depicts PWM operating waveforms under various conditions

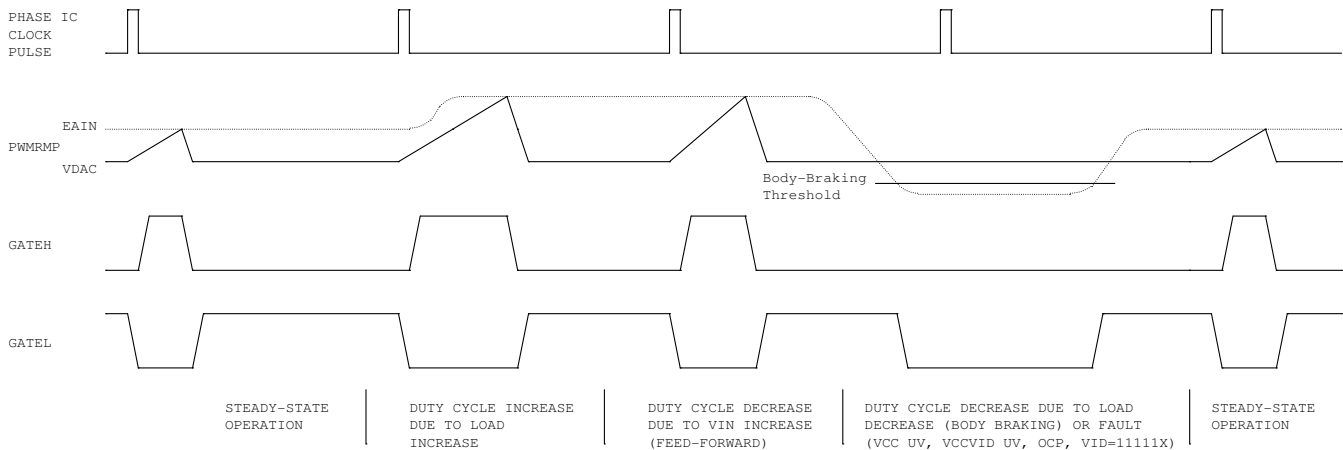


Figure 5 – PWM Operating Waveforms

### Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor. The equation of the sensing network is,

$$v_C(s) = v_L(s) \frac{1}{1 + sR_S C_S} = i_L(s) \frac{R_L + sL}{1 + sR_S C_S}$$

Usually the resistor  $R_S$  and capacitor  $C_S$  are chosen so that the time constant of  $R_S$  and  $C_S$  equals the time constant of the inductor which is the inductance  $L$  over the inductor DCR. If the two time constants match, the voltage across  $C_S$  is proportional to the current through  $L$ , and the sense circuit can be treated as if only a sense resistor with the value of  $R_L$  was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

### Current Sense Amplifier

A high speed differential current sense amplifier is located in the Phase IC, as shown in Figure 6. Its gain decreases with increasing temperature and is nominally 34 at 25°C and 29 at 125°C (–1470 ppm/°C). This reduction of gain tends to compensate the 3850 ppm/°C increase in inductor DCR. Since in most designs the Phase IC junction is hotter than the inductor these two effects tend to cancel such that no additional temperature compensation of the load line is required.

The current sense amplifier can accept positive differential input up to 100mV and negative up to –20mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the Control IC and other Phases through an on-chip 10KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the average inductor current through all the inductors and is used by the Control IC for voltage positioning and current limit protection.

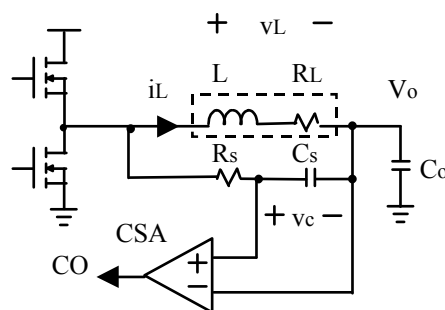


Figure 6 – Inductor Current Sensing and Current Sense Amplifier

### Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each Phase IC. The output of the current sense amplifier is compared with the share bus less a nominal 20mV offset. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will activate a current source that reduces the slope of its PWM ramp thereby increasing its duty cycle and output current. The crossover frequency of the current share loop can be programmed with a capacitor at the SCOMP pin so that the share loop does not interact with the output voltage loop.

## IR3084 THEORY OF OPERATION

### Block Diagram

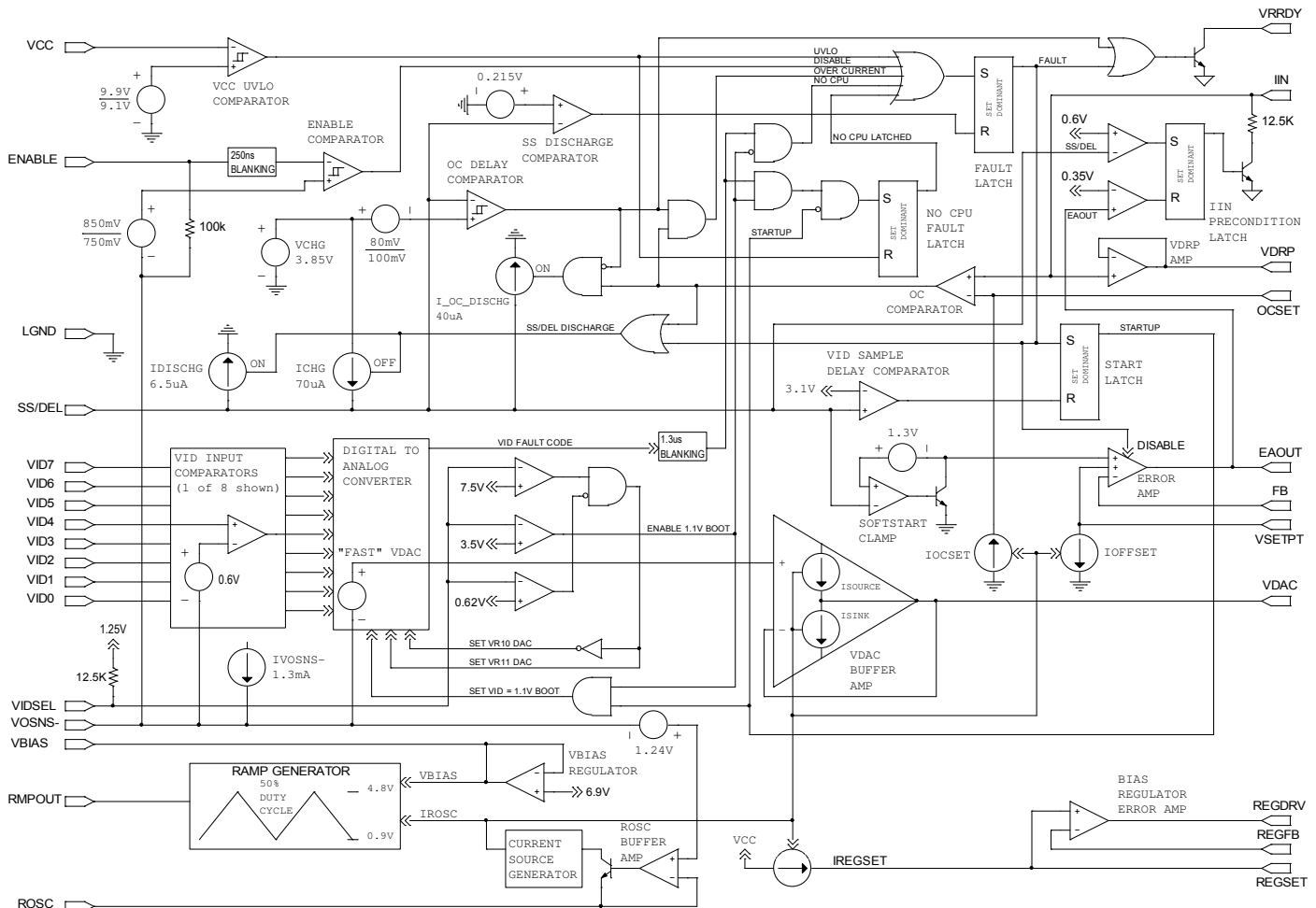


Figure 7 – IR3084 Block Diagram

### VID Control

An 8-bit VID voltage compatible with VR 10 (see Table 1) and VR11 (see Table 2) is available at the VDAC pin. The VIDSEL pin configures the DAC for VR10 if grounded or connected to VCC (12V) and for VR11 if floated or connected to VBIAS (6.9V). The VIDSEL pin is internally pulled-up to 1.25V through a 12.5Kohm resistor. The VID pins require an external bias voltage and should not be floated. The VID input comparators, with 0.6V threshold, monitor the VID pins and control the 8 bit Digital-to-Analog Converter (DAC) whose output is sent to the VDAC buffer amplifier. The output of the buffer amp is the VDAC pin. The VDAC voltage is post-package trimmed to compensate for the input offsets of the Error Amp to provide a 0.5% system accuracy. The actual VDAC voltage does not represent the system set point and has a wider tolerance.

| VID4 | VID3 | VID2 | VID1 | VID0 | VID5 | VID6 | Voltage |
|------|------|------|------|------|------|------|---------|
| 0    | 1    | 0    | 1    | 0    | 1    | 1    | 1.60000 |
| 0    | 1    | 0    | 1    | 0    | 1    | 0    | 1.59375 |
| 0    | 1    | 0    | 1    | 1    | 0    | 1    | 1.58750 |
| 0    | 1    | 0    | 1    | 1    | 0    | 0    | 1.58125 |
| 0    | 1    | 0    | 1    | 1    | 1    | 1    | 1.57500 |
| 0    | 1    | 0    | 1    | 1    | 1    | 0    | 1.56875 |
| 0    | 1    | 1    | 0    | 0    | 0    | 1    | 1.56250 |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 1.55625 |
| 0    | 1    | 1    | 0    | 0    | 1    | 1    | 1.55000 |
| 0    | 1    | 1    | 0    | 0    | 1    | 0    | 1.54375 |
| 0    | 1    | 1    | 0    | 1    | 0    | 1    | 1.53750 |
| 0    | 1    | 1    | 0    | 1    | 0    | 0    | 1.53125 |
| 0    | 1    | 1    | 0    | 1    | 1    | 1    | 1.52500 |
| 0    | 1    | 1    | 0    | 1    | 1    | 0    | 1.51875 |
| 0    | 1    | 1    | 1    | 0    | 0    | 1    | 1.51250 |
| 0    | 1    | 1    | 1    | 0    | 0    | 0    | 1.50625 |
| 0    | 1    | 1    | 1    | 0    | 1    | 1    | 1.50000 |
| 0    | 1    | 1    | 1    | 0    | 1    | 0    | 1.49375 |
| 0    | 1    | 1    | 1    | 1    | 0    | 1    | 1.48750 |
| 0    | 1    | 1    | 1    | 1    | 0    | 0    | 1.48125 |
| 0    | 1    | 1    | 1    | 1    | 1    | 1    | 1.47500 |
| 0    | 1    | 1    | 1    | 1    | 1    | 0    | 1.46875 |
| 1    | 0    | 0    | 0    | 0    | 0    | 1    | 1.46250 |
| 1    | 0    | 0    | 0    | 0    | 0    | 0    | 1.45625 |
| 1    | 0    | 0    | 0    | 0    | 1    | 1    | 1.45000 |
| 1    | 0    | 0    | 0    | 0    | 1    | 0    | 1.44375 |
| 1    | 0    | 0    | 0    | 1    | 0    | 1    | 1.43750 |
| 1    | 0    | 0    | 0    | 1    | 0    | 0    | 1.43125 |
| 1    | 0    | 0    | 0    | 1    | 1    | 1    | 1.42500 |
| 1    | 0    | 0    | 0    | 1    | 1    | 0    | 1.41875 |
| 1    | 0    | 0    | 1    | 0    | 0    | 1    | 1.41250 |
| 1    | 0    | 0    | 1    | 0    | 0    | 0    | 1.40625 |
| 1    | 0    | 0    | 1    | 0    | 1    | 1    | 1.40000 |
| 1    | 0    | 0    | 1    | 0    | 1    | 0    | 1.39375 |
| 1    | 0    | 0    | 1    | 1    | 0    | 1    | 1.38750 |
| 1    | 0    | 0    | 1    | 1    | 0    | 0    | 1.38125 |
| 1    | 0    | 0    | 1    | 1    | 1    | 1    | 1.37500 |
| 1    | 0    | 0    | 1    | 1    | 1    | 0    | 1.36875 |
| 1    | 0    | 1    | 0    | 0    | 0    | 1    | 1.36250 |
| 1    | 0    | 1    | 0    | 0    | 0    | 0    | 1.35625 |
| 1    | 0    | 1    | 0    | 0    | 1    | 1    | 1.35000 |
| 1    | 0    | 1    | 0    | 0    | 1    | 0    | 1.34375 |
| 1    | 0    | 1    | 0    | 1    | 0    | 1    | 1.33750 |
| 1    | 0    | 1    | 0    | 1    | 0    | 0    | 1.33125 |
| 1    | 0    | 1    | 0    | 1    | 1    | 1    | 1.32500 |
| 1    | 0    | 1    | 0    | 1    | 1    | 0    | 1.31875 |
| 1    | 0    | 1    | 1    | 0    | 0    | 1    | 1.31250 |
| 1    | 0    | 1    | 1    | 0    | 0    | 0    | 1.30625 |
| 1    | 0    | 1    | 1    | 0    | 1    | 1    | 1.30000 |
| 1    | 0    | 1    | 1    | 0    | 1    | 0    | 1.29375 |
| 1    | 0    | 1    | 1    | 1    | 0    | 1    | 1.28750 |
| 1    | 0    | 1    | 1    | 1    | 0    | 0    | 1.28125 |
| 1    | 0    | 1    | 1    | 1    | 1    | 1    | 1.27500 |
| 1    | 0    | 1    | 1    | 1    | 1    | 0    | 1.26875 |
| 1    | 1    | 0    | 0    | 0    | 0    | 1    | 1.26250 |
| 1    | 1    | 0    | 0    | 0    | 0    | 0    | 1.25625 |
| 1    | 1    | 0    | 0    | 0    | 1    | 1    | 1.25000 |
| 1    | 1    | 0    | 0    | 0    | 1    | 0    | 1.24375 |
| 1    | 1    | 0    | 0    | 1    | 0    | 1    | 1.23750 |
| 1    | 1    | 0    | 0    | 1    | 0    | 0    | 1.23125 |
| 1    | 1    | 0    | 0    | 1    | 1    | 1    | 1.22500 |
| 1    | 1    | 0    | 0    | 1    | 1    | 0    | 1.21875 |
| 1    | 1    | 0    | 1    | 0    | 0    | 1    | 1.21250 |
| 1    | 1    | 0    | 1    | 0    | 0    | 0    | 1.20625 |
| 1    | 1    | 1    | 0    | 1    | 0    | 1    | 1.20000 |
| 1    | 1    | 1    | 0    | 1    | 0    | 0    | 1.19375 |
| 1    | 1    | 1    | 0    | 1    | 1    | 0    | 1.18750 |
| 1    | 1    | 1    | 0    | 1    | 1    | 0    | 1.18125 |
| 1    | 1    | 1    | 0    | 1    | 1    | 1    | 1.17500 |
| 1    | 1    | 1    | 0    | 1    | 1    | 0    | 1.16875 |
| 1    | 1    | 1    | 1    | 0    | 0    | 1    | 1.16250 |
| 1    | 1    | 1    | 1    | 0    | 0    | 0    | 1.15625 |
| 1    | 1    | 1    | 1    | 0    | 1    | 1    | 1.15000 |
| 1    | 1    | 1    | 1    | 0    | 1    | 0    | 1.14375 |
| 1    | 1    | 1    | 1    | 0    | 1    | 0    | 1.13750 |
| 1    | 1    | 1    | 1    | 0    | 1    | 0    | 1.13125 |
| 1    | 1    | 1    | 1    | 0    | 1    | 1    | 1.12500 |
| 1    | 1    | 1    | 1    | 0    | 1    | 0    | 1.11875 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 1.11250 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 1.10625 |
| 1    | 1    | 1    | 1    | 1    | 0    | 1    | 1.10000 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 1.09375 |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 1.08750 |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 1.08125 |
| 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1.07500 |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 1.06875 |
| 1    | 1    | 1    | 1    | 1    | 0    | 1    | 1.06250 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 1.05625 |
| 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1.05000 |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 1.04375 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 1.03750 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 1.03125 |
| 1    | 1    | 1    | 1    | 1    | 0    | 1    | 1.02500 |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 1.01875 |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 1.01250 |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 1.00625 |
| 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1.00000 |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 0.99375 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.98750 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.98125 |
| 1    | 1    | 1    | 1    | 1    | 0    | 1    | 0.97500 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.96875 |
| 1    | 1    | 1    | 1    | 1    | 0    | 1    | 0.96250 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.95625 |
| 1    | 1    | 1    | 1    | 1    | 1    | 1    | 0.95000 |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 0.94375 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.93750 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.93125 |
| 1    | 1    | 1    | 1    | 1    | 0    | 1    | 0.92500 |
| 1    | 1    | 1    | 1    | 1    | 0    | 1    | 0.91875 |
| 1    | 1    | 1    | 1    | 1    | 0    | 1    | 0.91250 |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 0.90625 |
| 1    | 1    | 1    | 1    | 1    | 1    | 1    | 0.90000 |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 0.89375 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.88750 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.88125 |
| 1    | 1    | 1    | 1    | 1    | 0    | 1    | 0.87500 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.86875 |
| 1    | 1    | 1    | 1    | 1    | 0    | 1    | 0.86250 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.85625 |
| 1    | 1    | 1    | 1    | 1    | 1    | 1    | 0.85000 |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 0.84375 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.83750 |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.83125 |

Table 1 – VR10 VID Table with 6.25mV extension

| Hex (VID7:VID0) | Dec (VID7:VID0) | Voltage |
|-----------------|-----------------|---------|
| 00              | 00000000        | Fault   |
| 01              | 00000001        | Fault   |
| 02              | 00000010        | 1.60000 |
| 03              | 00000011        | 1.59375 |
| 04              | 00000100        | 1.58750 |
| 05              | 00000101        | 1.58125 |
| 06              | 00000110        | 1.57500 |
| 07              | 00000111        | 1.56875 |
| 08              | 00001000        | 1.56250 |
| 09              | 00001001        | 1.55625 |
| 0A              | 00001010        | 1.55000 |
| 0B              | 00001011        | 1.54375 |
| 0C              | 00001100        | 1.53750 |
| 0D              | 00001101        | 1.53125 |
| 0E              | 00001110        | 1.52500 |
| 0F              | 00001111        | 1.51875 |
| 10              | 00010000        | 1.51250 |
| 11              | 00010001        | 1.50625 |
| 12              | 00010010        | 1.50000 |
| 13              | 00010011        | 1.49375 |
| 14              | 00010100        | 1.48750 |
| 15              | 00010101        | 1.48125 |
| 16              | 00010110        | 1.47500 |
| 17              | 00010111        | 1.46875 |
| 18              | 00011000        | 1.46250 |
| 19              | 00011001        | 1.45625 |
| 1A              | 00011010        | 1.45000 |
| 1B              | 00011011        | 1.44375 |
| 1C              | 00011100        | 1.43750 |
| 1D              | 00011101        | 1.43125 |
| 1E              | 00011110        | 1.42500 |
| 1F              | 00011111        | 1.41875 |
| 20              | 00100000        | 1.41250 |
| 21              | 00100001        | 1.40625 |
| 22              | 00100010        | 1.40000 |
| 23              | 00100011        | 1.39375 |
| 24              | 00100100        | 1.38750 |
| 25              | 00100101        | 1.38125 |
| 26              | 00100110        | 1.37500 |
| 27              | 00100111        | 1.36875 |
| 28              | 00101000        | 1.36250 |
| 29              | 00101001        | 1.35625 |
| 2A              | 00101010        | 1.35000 |
| 2B              | 00101011        | 1.34375 |
| 2C              | 00101100        | 1.33750 |
| 2D              | 00101101        | 1.33125 |
| 2E              | 00101110        | 1.32500 |
| 2F              | 00101111        | 1.31875 |
| 30              | 00110000        | 1.31250 |
| 31              | 00110001        | 1.30625 |
| 32              | 00110010        | 1.30000 |
| 33              | 00110011        | 1.29375 |
| 34              | 00110100        | 1.28750 |
| 35              | 00110101        | 1.28125 |
| 36              | 00110110        | 1.27500 |
| 37              | 00110111        | 1.26875 |
| 38              | 00111000        | 1.26250 |
| 39              | 00111001        | 1.25625 |
| 3A              | 00111010        | 1.25000 |
| 3B              | 00111011        | 1.24375 |
| 3C              | 00111100        | 1.23750 |
| 3D              | 00111101        | 1.23125 |
| 3E              | 00111110        | 1.22500 |
| 3F              | 00111111        | 1.21875 |

| Hex (VID7:VID0) | Dec (VID7:VID0) | Voltage |
|-----------------|-----------------|---------|
| 40              | 01000000        | 1.21250 |
| 41              | 01000001        | 1.20625 |
| 42              | 01000010        | 1.20000 |
| 43              | 01000011        | 1.19375 |
| 44              | 01000100        | 1.18750 |
| 45              | 01000101        | 1.18125 |
| 46              | 01000110        | 1.17500 |
| 47              | 01000111        | 1.16875 |
| 48              | 01001000        | 1.16250 |
| 49              | 01001001        | 1.15625 |
| 4A              | 01001010        | 1.15000 |
| 4B              | 01001011        | 1.14375 |
| 4C              | 01001100        | 1.13750 |
| 4D              | 01001101        | 1.13125 |
| 4E              | 01001110        | 1.12500 |
| 4F              | 01001111        | 1.11875 |
| 50              | 01010000        | 1.11250 |
| 51              | 01010001        | 1.10625 |
| 52              | 01010010        | 1.10000 |
| 53              | 01010011        | 1.09375 |
| 54              | 01010100        | 1.08750 |
| 55              | 01010101        | 1.08125 |
| 56              | 01010110        | 1.07500 |
| 57              | 01010111        | 1.06875 |
| 58              | 01011000        | 1.06250 |
| 59              | 01011001        | 1.05625 |
| 5A              | 01011010        | 1.05000 |
| 5B              | 01011011        | 1.04375 |
| 5C              | 01011100        | 1.03750 |
| 5D              | 01011101        | 1.03125 |
| 5E              | 01011110        | 1.02500 |
| 5F              | 01011111        | 1.01875 |
| 60              | 01100000        | 1.01250 |
| 61              | 01100001        | 1.00625 |
| 62              | 01100010        | 1.00000 |
| 63              | 01100011        | 0.99375 |
| 64              | 01100100        | 0.98750 |
| 65              | 01100101        | 0.98125 |
| 66              | 01100110        | 0.97500 |
| 67              | 01100111        | 0.96875 |
| 68              | 01101000        | 0.96250 |
| 69              | 01101001        | 0.95625 |
| 6A              | 01101010        | 0.95000 |
| 6B              | 01101011        | 0.94375 |
| 6C              | 01101100        | 0.93750 |
| 6D              | 01101101        | 0.93125 |
| 6E              | 01101110        | 0.92500 |
| 6F              | 01101111        | 0.91875 |
| 70              | 01110000        | 0.91250 |
| 71              | 01110001        | 0.90625 |
| 72              | 01110010        | 0.90000 |
| 73              | 01110011        | 0.89375 |
| 74              | 01110100        | 0.88750 |
| 75              | 01110101        | 0.88125 |
| 76              | 01110110        | 0.87500 |
| 77              | 01110111        | 0.86875 |
| 78              | 01111000        | 0.86250 |
| 79              | 01111001        | 0.85625 |
| 7A              | 01111010        | 0.85000 |
| 7B              | 01111011        | 0.84375 |
| 7C              | 01111100        | 0.83750 |
| 7D              | 01111101        | 0.83125 |
| 7E              | 01111110        | 0.82500 |
| 7F              | 01111111        | 0.81875 |

Table 2 – VR11 VID Table (Part 1)

| Hex (VID7:VID0) | Dec (VID7:VID0) | Voltage |
|-----------------|-----------------|---------|
| 80              | 10000000        | 0.81250 |
| 81              | 10000001        | 0.80625 |
| 82              | 10000010        | 0.80000 |
| 83              | 10000011        | 0.79375 |
| 84              | 10000100        | 0.78750 |
| 85              | 10000101        | 0.78125 |
| 86              | 10000110        | 0.77500 |
| 87              | 10000111        | 0.76875 |
| 88              | 10001000        | 0.76250 |
| 89              | 10001001        | 0.75625 |
| 8A              | 10001010        | 0.75000 |
| 8B              | 10001011        | 0.74375 |
| 8C              | 10001100        | 0.73750 |
| 8D              | 10001101        | 0.73125 |
| 8E              | 10001110        | 0.72500 |
| 8F              | 10001111        | 0.71875 |
| 90              | 10010000        | 0.71250 |
| 91              | 10010001        | 0.70625 |
| 92              | 10010010        | 0.70000 |
| 93              | 10010011        | 0.69375 |
| 94              | 10010100        | 0.68750 |
| 95              | 10010101        | 0.68125 |
| 96              | 10010110        | 0.67500 |
| 97              | 10010111        | 0.66875 |
| 98              | 10011000        | 0.66250 |
| 99              | 10011001        | 0.65625 |
| 9A              | 10011010        | 0.65000 |
| 9B              | 10011011        | 0.64375 |
| 9C              | 10011100        | 0.63750 |
| 9D              | 10011101        | 0.63125 |
| 9E              | 10011110        | 0.62500 |
| 9F              | 10011111        | 0.61875 |
| A0              | 10100000        | 0.61250 |
| A1              | 10100001        | 0.60625 |
| A2              | 10100010        | 0.60000 |
| A3              | 10100011        | 0.59375 |
| A4              | 10100100        | 0.58750 |
| A5              | 10100101        | 0.58125 |
| A6              | 10100110        | 0.57500 |
| A7              | 10100111        | 0.56875 |
| A8              | 10101000        | 0.56250 |
| A9              | 10101001        | 0.55625 |
| AA              | 10101010        | 0.55000 |
| AB              | 10101011        | 0.54375 |
| AC              | 10101100        | 0.53750 |
| AD              | 10101101        | 0.53125 |
| AE              | 10101110        | 0.52500 |
| AF              | 10101111        | 0.51875 |
| B0              | 10110000        | 0.51250 |
| B1              | 10110001        | 0.50625 |
| B2              | 10110010        | 0.50000 |
| B3              | 10110011        | 0.49375 |
| B4              | 10110100        | 0.48750 |
| B5              | 10110101        | 0.48125 |
| B6              | 10110110        | 0.47500 |
| B7              | 10110111        | 0.46875 |
| B8              | 10111000        | 0.46250 |
| B9              | 10111001        | 0.45625 |
| BA              | 10111010        | 0.45000 |
| BB              | 10111011        | 0.44375 |
| BC              | 10111100        | 0.43750 |
| BD              | 10111101        | 0.43125 |
| BE              | 10111110        | 0.42500 |
| BF              | 10111111        | 0.41875 |

| Hex (VID7:VID0) | Dec (VID7:VID0) | Voltage |
|-----------------|-----------------|---------|
| C0              | 11000000        | 0.41250 |
| C1              | 11000001        | 0.40625 |
| C2              | 11000010        | 0.40000 |
| C3              | 11000011        | 0.39375 |
| C4              | 11000100        | 0.38750 |
| C5              | 11000101        | 0.38125 |
| C6              | 11000110        | 0.37500 |
| C7              | 11000111        | 0.36875 |
| C8              | 11001000        | 0.36250 |
| C9              | 11001001        | 0.35625 |
| CA              | 11001010        | 0.35000 |
| CB              | 11001011        | 0.34375 |
| CC              | 11001100        | 0.33750 |
| CD              | 11001101        | 0.33125 |
| CE              | 11001110        | 0.32500 |
| CF              | 11001111        | 0.31875 |
| D0              | 11010000        | 0.31250 |
| D1              | 11010001        | 0.30625 |
| D2              | 11010010        | 0.30000 |
| D3              | 11010011        | 0.29375 |
| D4              | 11010100        | 0.28750 |
| D5              | 11010101        | 0.28125 |
| D6              | 11010110        | 0.27500 |
| D7              | 11010111        | 0.26875 |
| D8              | 11011000        | 0.26250 |
| D9              | 11011001        | 0.25625 |
| DA              | 11011010        | 0.25000 |
| DB              | 11011011        | 0.24375 |
| DC              | 11011100        | 0.23750 |
| DD              | 11011101        | 0.23125 |
| DE              | 11011110        | 0.22500 |
| DF              | 11011111        | 0.21875 |
| E0              | 11100000        | 0.21250 |
| E1              | 11100001        | 0.20625 |
| E2              | 11100010        | 0.20000 |
| E3              | 11100011        | 0.19375 |
| E4              | 11100100        | 0.18750 |
| E5              | 11100101        | 0.18125 |
| E6              | 11100110        | 0.17500 |
| E7              | 11100111        | 0.16875 |
| E8              | 11101000        | 0.16250 |
| E9              | 11101001        | 0.15625 |
| EA              | 11101010        | 0.15000 |
| EB              | 11101011        | 0.14375 |
| EC              | 11101100        | 0.13750 |
| ED              | 11101101        | 0.13125 |
| EE              | 11101110        | 0.12500 |
| EF              | 11101111        | 0.11875 |
| F0              | 11110000        | 0.11250 |
| F1              | 11110001        | 0.10625 |
| F2              | 11110010        | 0.10000 |
| F3              | 11110011        | 0.10000 |
| F4              | 11110100        | 0.10000 |
| F5              | 11110101        | 0.10000 |
| F6              | 11110110        | 0.10000 |
| F7              | 11110111        | 0.10000 |
| F8              | 11111000        | 0.10000 |
| F9              | 11111001        | 0.10000 |
| FA              | 11111010        | 0.10000 |
| FB              | 11111011        | 0.10000 |
| FC              | 11111100        | 0.10000 |
| FD              | 11111101        | 0.10000 |
| FE              | 11111110        | FAULT   |
| FF              | 11111111        | FAULT   |

Table 2 – VR11 VID Table (Part 2)

The IR3084 can accept changes in the VID code while operating and vary the DAC voltage accordingly. The sink/source capability of the VDAC buffer amp is programmed by the same external resistor that sets the oscillator frequency. The slew rate of the voltage at the VDAC pin can be adjusted by an external capacitor between VDAC pin and the VOSNS- pin. A resistor connected in series with this capacitor is required to compensate the VDAC buffer amplifier. Digital VID transitions result in a smooth analog transition of the VDAC voltage and converter output voltage minimizing inrush currents in the input and output capacitors and overshoot of the output voltage.

### Adaptive Voltage Positioning

Adaptive Voltage Positioning (AVP) is needed to reduce the output voltage deviations during load transients and the power dissipation of the load when it is drawing high current. The circuitry related to the voltage positioning is shown in Figure 8.

Resistor RSETPT is connected between the VDAC pin and VSETPT pin to set the desired amount of fixed offset voltage below the DAC voltage. The VSETPT is internally connected to the non-inverting input of the voltage error amplifier and an internal current source  $I_{\text{OFFSET}}$ , whose value is programmed by the same external resistor that programs the oscillator frequency. The voltage drop across RSETPT caused by  $I_{\text{OFFSET}}$  sets the no-load  $I$  offset voltage below the nominal DAC setting.

The voltage at the VDRP pin is a buffered version of the share bus and represents the sum of the DAC voltage and the average inductor current of all the phases. The VDRP pin is connected to the FB pin through the resistor RDRP. Since the Error Amp will force the loop to maintain FB to be equal to the VSETPT reference voltage, a current will flow into the FB pin equal to  $(\text{VDRP} - \text{VSETPT}) / \text{RDRP}$ . When the load current increases, the VDRP voltage increases accordingly. More current flows through the feedback resistor RFB, and makes the output voltage lower proportional to the load current. The positioning voltage can be programmed by the resistor RDRP so that the droop impedance produces the desired converter output impedance. The offset and slope of the converter output impedance are referenced to and therefore independent of the VDAC voltage.

Due to the difference between VDAC and VSETPT, the VDRP will cause extra offset voltage through RDRP and RFB. The total offset voltage is the sum of voltage across RVSETPT and the voltage drop on the RFB at no load.

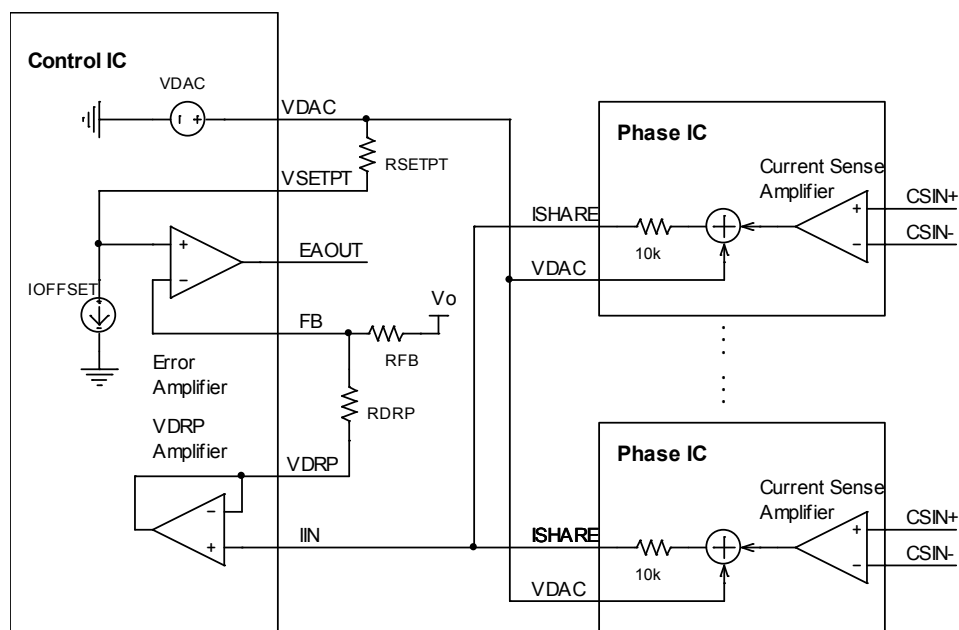


Figure 8 – Adaptive voltage positioning

### Inductor DCR Temperature Correction

If the thermal compensation of the inductor DCR provided by the temperature dependent gain of the current sense amplifier is not adequate, a negative temperature coefficient (NTC) thermistor can be used for additional correction. The thermistor should be placed close to the inductor and connected in parallel with the feedback resistor, as shown in Figure 9. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor.

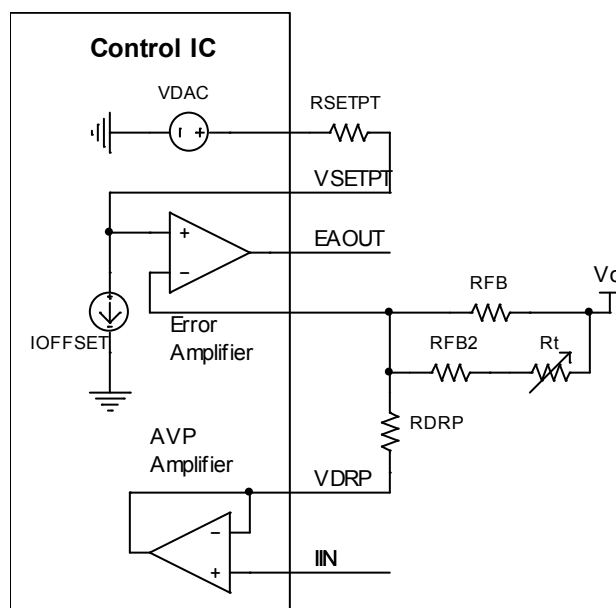


Figure 9 – Temperature compensation of inductor DCR

### Remote Voltage Sensing

To compensate for impedance in the ground plane, the VOSNS- pin is used for remote sensing and connects directly to the load. The VDAC voltage is referenced to VOSNS- to avoid additional error terms or delay related to a separate differential amplifier. The capacitor connecting the VDAC and VOSNS- pins ensure that high speed transients are fed directly into the error amp without delay.

### Start-up Modes

The IR3084 has a programmable soft-start function to limit the surge current during the converter start-up. A capacitor connected between the SS/DEL and LGND pins controls soft start as well as over-current protection delay and hiccup mode timing. A charge current of 70uA controls the positive slope of the voltage at the SS/DEL pin.

There are two types of start-up possible: Boot Mode (VR11) and Non-Boot Mode (legacy VR10). In Boot Mode, the soft start circuitry will initially set the voltage at the VDAC pin to 1.1V and the converter's output will slowly rise, using the slew rate set by the capacitor at the SS/DEL pin, until it's equal to 1.1V. After Vcore achieves the 1.1V Boot voltage, there will be a short delay, the VID pins will be sampled, and the voltage at the VDAC pin and the converter's output will increase or decrease to the desired VID setting using the dynamic VID slew rate. In Non-Boot Mode, the soft start sequence will ramp the voltage at the VDAC pin directly to the external VID setting using the slew rate set by the capacitor at the SS/DEL pin without pausing at the 1.1V Boot voltage.

Figure 10a depicts the start-up sequence without AVP in Boot Mode (VRM11) – VIDSEL is either floating or grounded. First, the VDAC pin is charged to the 1.1V Boot voltage. Then, if there are no fault conditions, the SS/DEL capacitor will begin to be charged. Initially, the error amplifier's output will be clamped low until the voltage at the SS/DEL pin reaches 1.3V. After the voltage at the SS/DEL pin rises to 1.3V, the error amplifier's output will begin to rise and the converter's output voltage will be regulated 1.3V below the voltage at the SS/DEL pin. The converter's output voltage will slowly ramp to the 1.1V Boot voltage. The SS/DEL pin's voltage will continue to increase until it rises above the 3.1V threshold of the VID delay comparator. When the SS/DEL voltage exceeds 3.1V, the VID inputs will be sampled and the VDAC pin will transition to the level determined by the VID inputs at the dynamic VID slew rate. When the voltage on the SS/DEL pin rises above 3.77V the VRRDY Delay Comparator will allow the VRRDY signal to be asserted. SS/DEL will continue to rise until finally settling at 3.85V, indicating the end of the start-up sequence.

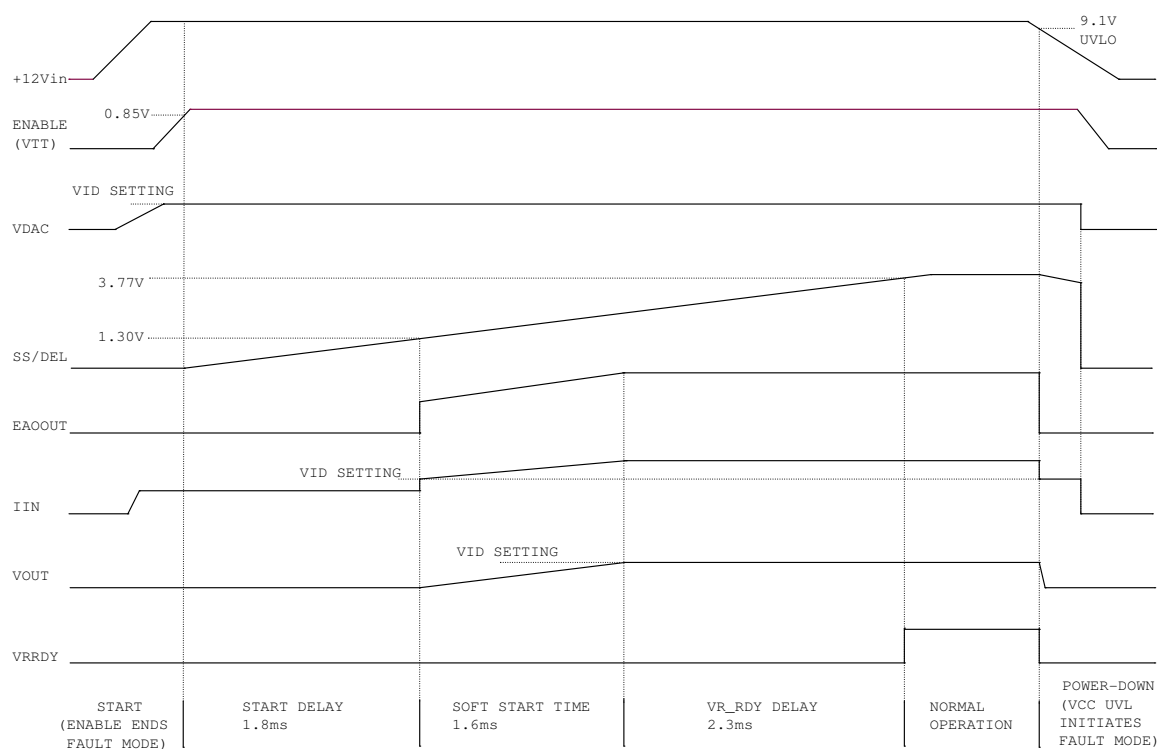
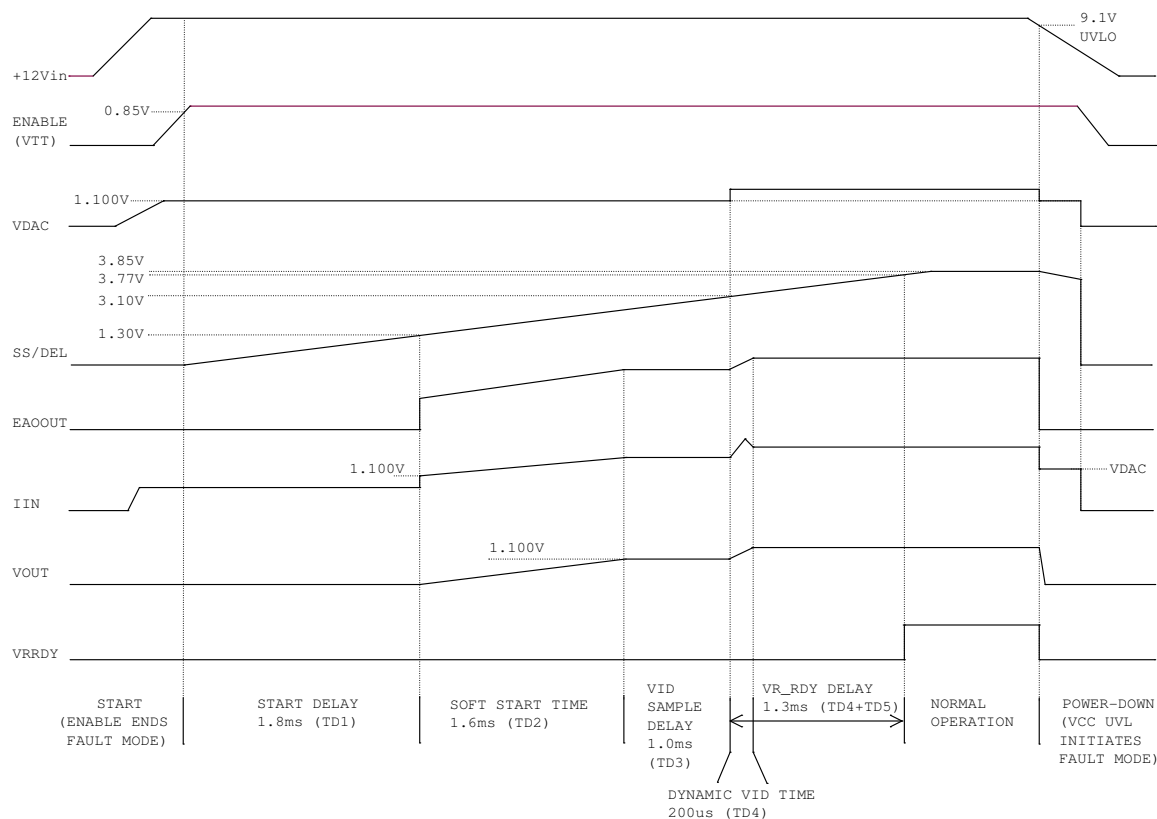
Figure 10b depicts the start-up sequence in Non-Boot Mode – VIDSEL is connected to VBIAS (6.9V) or to VCC (12V). First, the external VID setting is sampled and the VDAC pin is set to the desired VID voltage. Then, if there are no fault conditions, the SS/DEL capacitor will begin to charge. Initially, the error amplifier's output will be clamped low until the voltage at the SS/DEL rises to 1.3V. After the voltage at the SS/DEL pin reaches 1.3V, the error amplifier's output will begin to rise and the converter's output voltage will be regulated 1.3V below the voltage at the SS/DEL pin. As the voltage at the SS/DEL pin continues to rise, the converter's output voltage will slowly increase until it is equal to the voltage at the VDAC pin. When the voltage on the SS/DEL pin rises above 3.77V the VRRDY Delay Comparator will allow the VRRDY signal to be asserted. SS/DEL will continue to rise until finally settling at 3.85V, indicating the end of the start-up sequence.

If AVP is used ( $R_{DRP} \neq \infty$ ), the soft start timing will change slightly because of the resistor from the VDRP amplifier to the Error Amplifier's FB pin. During startup with AVP, the VDRP amplifier will produce a voltage at the FB pin equal to VDAC times the resistor divider formed by the droop resistor and the feedback resistor from Vcore to the FB pin. To offset the contribution from the VDRP amplifier, the voltage at the SS/DEL pin will have to rise to beyond 1.3V before the Error Amplifier's output and Vcore begin to rise. For a DAC setting of 1.3V with typical load line slope, the Error Amplifier's output will begin to rise when the voltage at the SS/DEL pin reaches approximately 1.6V. The effect of this offset will be to slightly lengthen the Start Delay (TD1) and shorten the Soft Start Ramp Time (TD2).

The following table summarizes the differences between the 4 modes associated with setting the VIDSEL pin. In addition to changing the soft start sequence, the NO\_CPU code may or may not be ignored during startup and the NO\_CPU code may or may not be latched.

| VIDSEL Voltage | VID Table | 1.1V Boot Voltage During Startup? | Ignore NO CPU Codes During Startup? | Latch NO CPU Fault Code? |
|----------------|-----------|-----------------------------------|-------------------------------------|--------------------------|
| GND            | VR10      | YES                               | YES                                 | YES                      |
| FLOAT (1.2V)   | VR11      | YES                               | YES                                 | YES                      |
| VBIAS (6.9V)   | VR11      | NO                                | NO                                  | NO                       |
| VCC (12V)      | VR10      | NO                                | NO                                  | NO                       |

Table 3: 3084 Controller Functionality versus VIDSEL Voltages



## Fault Modes

Under Voltage Lock Out, VID = FAULT, as well as a low signal on the ENABLE input immediately sets the fault latch. This causes the EAOUT pin to drive low turning off the Phase IC drivers. The VRRDY pin also drives low. The SS/DEL capacitor will discharge down to 0.215V through a 6.5uA current source. If the fault has cleared the fault latch will be reset by the discharge comparator allowing a normal start-up sequence to occur. If a VID = FAULT condition is latched it can only be cleared by cycling power to the IR3084 on and off.

## Over-Current Protection Delay and Hiccup Mode

Figure 11 depicts the operating waveforms of the Over-Current protection. A delay is included if an over-current condition occurs after a successful soft start sequence. This is required because over-current conditions can occur as part of normal operation due to load transients or VID transitions. If an over-current fault occurs during normal operation it will activate the SS/DEL discharge current of 40uA but will not set the fault latch immediately. If the over-current condition persists long enough for the SS/DEL capacitor to discharge below the 100mV offset of the delay comparator, the Fault latch will be set pulling the error amp's output low inhibiting switching in the phase ICs and de-asserting the VRRDY signal.

The SS/DEL capacitor will continue to discharge until it reaches 0.215V and the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle the fault latch will be set without any delay and hiccup mode will begin. During hiccup mode the 10.8 to 1 charge to discharge current ratio results in a 9% hiccup mode duty cycle regardless of at what point the over-current condition occurs.

If the voltage at the SS/DEL pin is pulled below the SS/DEL to FB Input Offset Voltage (0.85V min), the converter can be disabled.

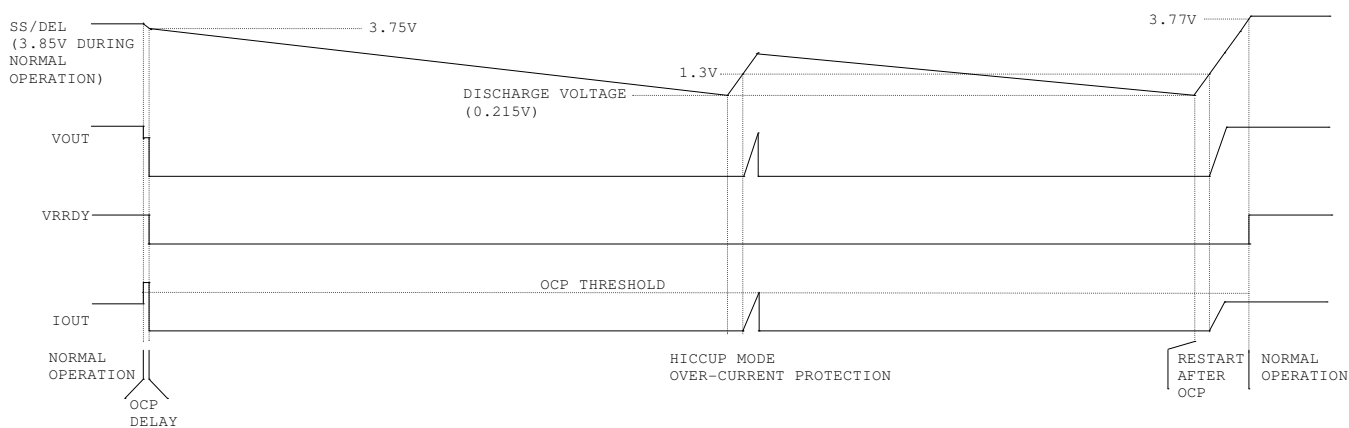


Figure 11 – Over-Current Protection Waveforms (VID = 1.1V for simplicity)

**Under Voltage Lockout (UVLO)**

The UVLO function monitors the IR3084's VCC supply pin and ensures that there is adequate voltage to safely power the internal circuitry. The IR3084's UVLO threshold is set higher than the minimum operating voltage of compatible Phase ICs thus providing UVLO protection for them as well. UVLO at the Phase ICs is a function of the Error Amplifier's output voltage. When the IR3084 is in UVLO, the Error Amplifier is disabled and EAOUT is at a very low voltage (<200mV) thus preventing the Phase ICs from becoming active.

During power-up, the IR3084's fault latch is reset when VCC exceeds 9.9V if there are no other faults. If the VCC voltage drops below 9.1V the fault latch will be set.

**Over Current Protection (OCP)**

The current limit threshold is set by a resistor connected between the OCSET and VDAC pins. If the IIN pin voltage, which is proportional to the average phase current plus DAC voltage, exceeds the OCSET voltage, the over-current protection is triggered.

**VID = Fault Code (NO\_CPU)**

When VIDSEL is grounded or left floating, NO\_CPU VID codes of 11111XX for VR10 and 0000000X, 1111111X for VR11 will set both the VID Fault Latch and the Fault Latch to disable the error amplifier. The controller will be latched OFF and a power-on reset (POR) will be required to produce a new soft start sequence. In these 2 modes, the NO\_CPU codes are ignored during startup. See Table 1 for further details.

When VIDSEL is set to VBIAS (6.9V) or VCC (12V), NO\_CPU VID codes of 11111XX for VR10 and 0000000X, 1111111X for VR11 will set the Fault Latch to disable the error amplifier but the VID Fault Latch will not be set. The controller will not be latched OFF and a soft start sequence will be produced when the NO\_CPU code is removed and the SS/DEL voltage falls below 0.215V. In these 2 modes, the NO\_CPU codes will be not be ignored during startup. See Table 1 for further details.

A 1.3μs delay is provided to prevent a NO\_CPU fault condition from occurring during Dynamic VID changes.

**VRRDY (Power Good) Output**

The VRRDY pin is an open-collector output and should be pulled up to a voltage source through a resistor. During soft-start, the VRRDY output remains low until the converter's output voltage is in regulation and SS/DEL is above 3.77V. The VRRDY pin transitions low if the fault latch is set. A high level at the VRRDY pin indicates that the converter is in operation and has no fault, but does not ensure the output voltage is within the specification. Output voltage regulation within the design limits can logically be assured however, assuming no component failure in the system.

**Load Current Indicator Output**

The VDRP pin voltage represents the average phase current of the converter plus the DAC voltage. The load current can be retrieved by subtracting the VDAC voltage from the VDRP voltage.

## System Reference Voltage (VBIAS)

The IR3084 supplies a 6.9V/6mA precision reference voltage from the VBIAS pin. The oscillator ramp trip points are based on the VBIAS voltage so it should be used to program the Phase ICs phase delay to minimize phase errors.

## Phase IC Gate Driver Bias Regulator / VRHOT Comparator

An internal amplifier can be configured as a gate driver bias regulator to provide programmable gate driver voltage for phase ICs (Figure 12a), or a thermal monitor to provide VRHOT/VRFAN signal as required in VR11 (Figure 12b).

The internal current source IREGSET whose value is programmed by the switching frequency going through the external RSET resistor sets the gate driver voltage or the VRHOT/VRFAN threshold voltage. An NTC thermistor is used to monitor the temperature on the VRM/VRD.

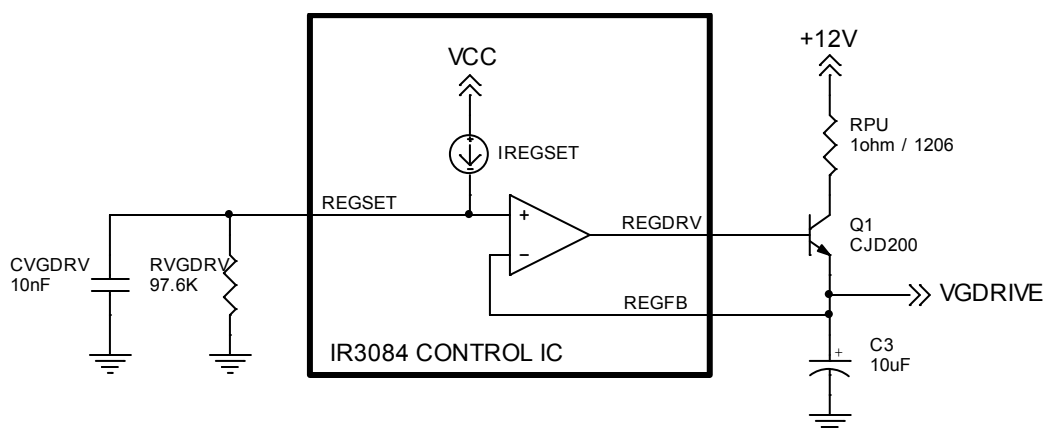


Figure 12a – IR3084 Bias Regulator configured for Gate Driver Bias Regulator

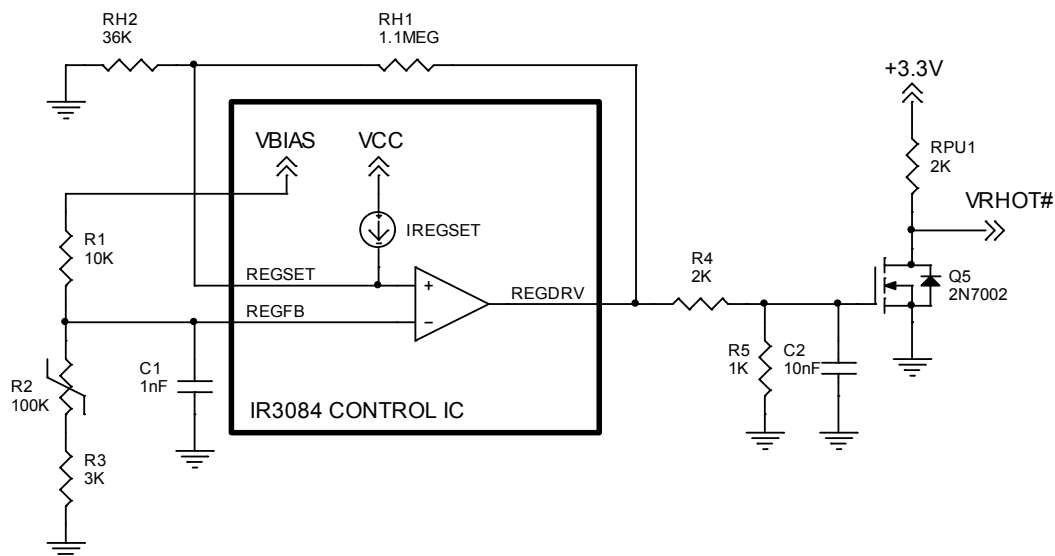


Figure 12b – IR3084 Bias Regulator configured for VRHOT# Function

## PERFORMANCE CHARACTERISTICS

Figure 13: Oscillator Frequency versus ROSC

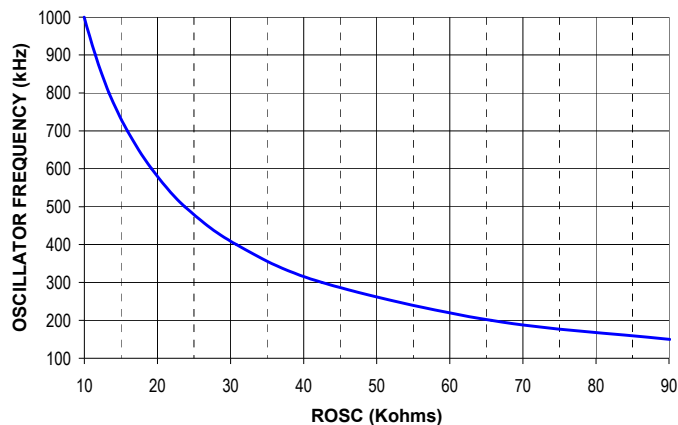


Figure 14: I(OCSET) versus ROSC

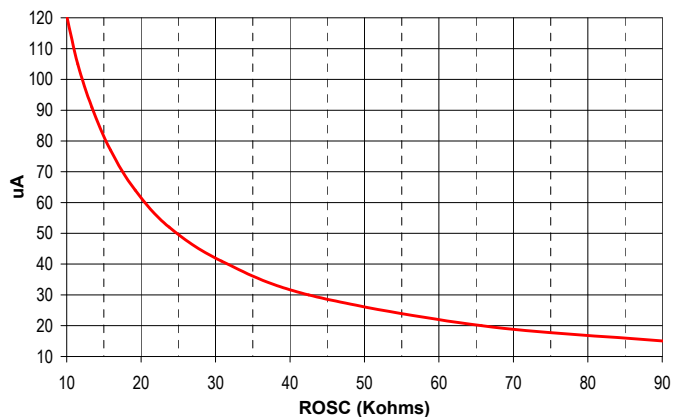


Figure 15: I(VSETPT) versus ROSC

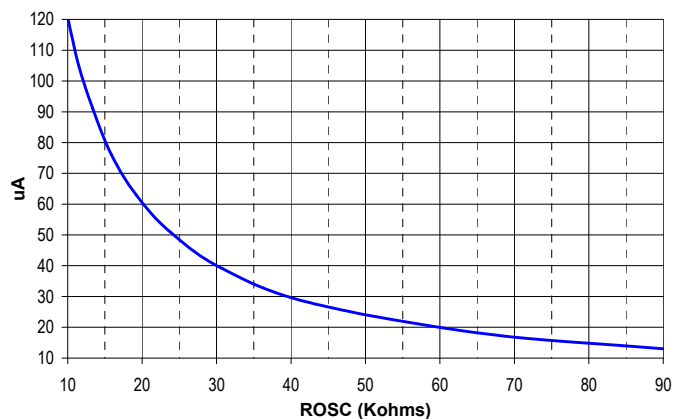


Figure 16: I(REGSET) CURRENT versus ROSC

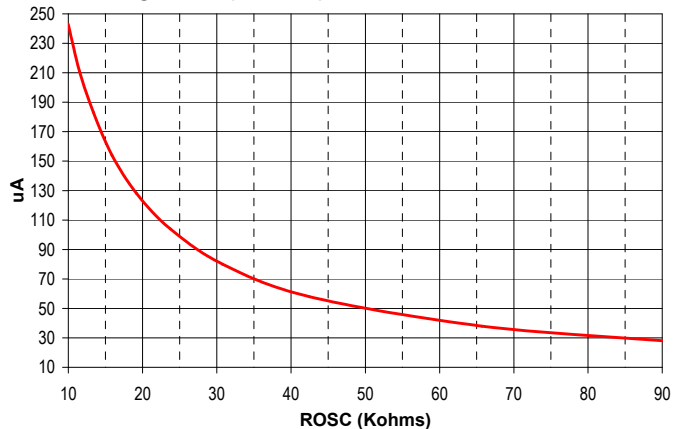


Figure 17: VDACC SINK & SOURCE CURRENT vs. ROSC

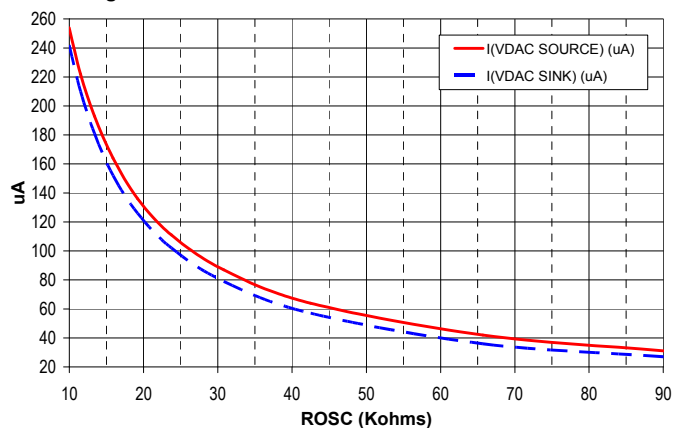
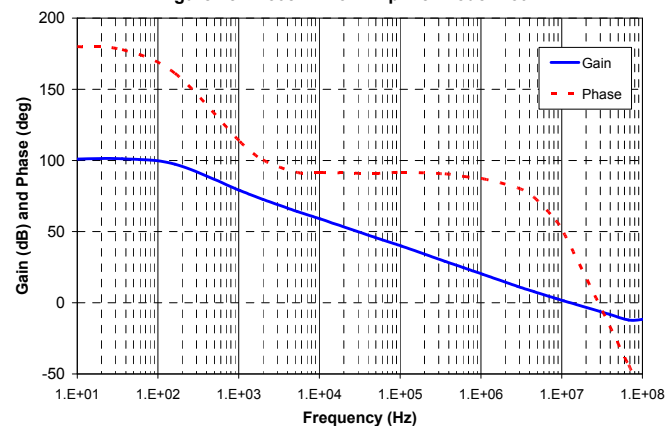


Figure 18: IR3084 Error Amplifier Bode Plot



**APPLICATIONS INFORMATION**

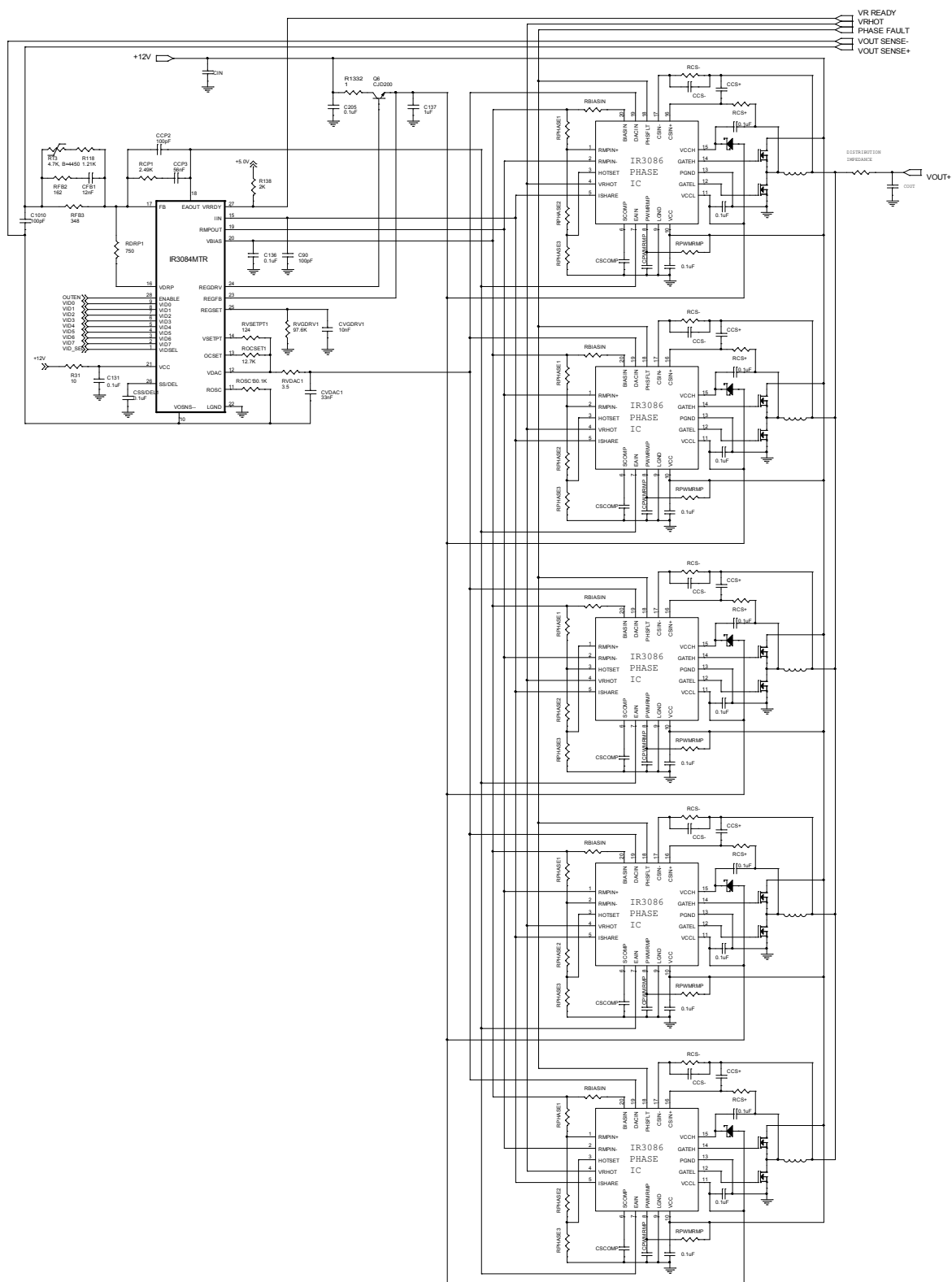


Figure 19 – IR3084/3086 5 Phase VRM/EVRD 11 Converter

## DESIGN PROCEDURES – IR3084 and IR3086 Chipset

### IR3084 EXTERNAL COMPONENTS

#### Oscillator Resistor $R_{osc}$

The oscillator of IR3084 generates a triangle waveform to synchronize the phase ICs, and the switching frequency of the each phase converter equals the oscillator frequency, which is set by the external resistor  $R_{osc}$  according to the curve in Figure 13 on page 6.

#### VDAC Slew Rate Programming Capacitor $C_{VDAC}$ and Resistor $R_{VDAC}$

The sink and source currents of the VDAC pin are set by the value of  $R_{osc}$ . The sink current capability of the VDAC pin is slightly less than the source current. Therefore, the VDAC sink current ( $I_{SINK}$ ) should be used to calculate  $C_{VDAC}$  to insure that the dynamic VID slew rate when  $V_{core}$  decreases is not too slow.

The negative slew rate of VDAC ( $SR_{DOWN}$ ) is programmed by the external capacitor  $C_{VDAC}$  as shown in Equation (1). The resistor  $R_{VDAC}$  is used to compensate/stabilize the VDAC circuit and is determined by Equation (2). The positive slew rate of the VDAC voltage ( $SR_{UP}$ ) is proportional to the negative slew rate of VDAC and can be calculated using Equation (3).

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} \quad (1)$$

Where:  $I_{SINK}$  is the sink current of the VDAC pin at the chosen value of  $R_{osc}$  as shown in Figure 17 on page 6.

$$R_{VDAC} = 0.5\Omega + \frac{3.2 * 10^{-15}}{C_{VDAC}^2} \quad (2)$$

$$SR_{UP} = \frac{I_{SOURCE}}{C_{VDAC}} \quad (3)$$

Where:  $I_{SOURCE}$  is the source current of the VDAC pin at the chosen value of  $R_{osc}$  as shown in Figure 17 on page 6.

The VID voltage rise or fall time during startup with Boot Mode (TD4) can be calculated using either Equation (4a) or (4b).

$$TD4 = \frac{C_{VDAC}}{I_{SOURCE}} * (VDAC - 1.1V) \quad \text{if } VDAC > 1.1V \quad (4a)$$

$$TD4 = \frac{C_{VDAC}}{I_{SINK}} * (1.1V - VDAC) \quad \text{if } VDAC < 1.1V \quad (4b)$$

Where: VDAC is the DAC voltage set by the VID pins.

$I_{SOURCE}$  and  $I_{SINK}$  are the source and sink currents of the VDAC pin.

If Boot Mode is not used then  $TD4 = 0$ .

### No Load Output Voltage Setting Resistor RVSETPT, Feedback Resistor RFB, and AVP Resistor RDRP

An external resistor,  $R_{VSETPT}$ , connected between the VDAC pin and the VSETPT pin is used to set the no load output voltage offset,  $V_{O\_NLOFST}$ , which is the difference between the VDAC voltage and output voltage at no load. However, the converter's output voltage will be set by the combination of VSETPT plus some contribution from the VDRP pin. At no load, both pins of the Error Amplifier are at  $VDAC - VSETPT$  while the VDRP pin is at  $VDAC + V_{OS} \cdot G_{CSA}$  ( $V_{OS}$  and  $G_{CSA}$  are the input offset and gain of the current sense amplifiers). Because the VDRP pin is at a higher voltage than the FB pin of the Error Amplifier, VDRP will contribute to the no load offset through the RDRP and RFB resistors. The design approach is to choose a value for the feedback resistor, RFB, from 100 to 2K and then calculate RDRP and  $R_{VSETPT}$  to provide the required no load offset voltage.

$$VSETPT = \frac{A * D - C * B}{(A + B - C - D)} \quad (5)$$

$$A = \frac{I_O * R_L * G_{CSA}}{n} + V_{CS\_TOFST} * G_{CSA} + V_{OS\_EA} \quad C = V_{CS\_TOFST} * G_{CSA} + V_{OS\_EA}$$

$$B = V_{O\_NLOFST} + I_O * R_o - V_{OS\_EA} \quad D = V_{O\_NLOFST} - V_{OS\_EA}$$

**Where:**  $I_O$  is the full load output current of the converter  
 $R_L$  is the ESR of the output inductor  
 $G_{CSA}$  is the gain of the current sense amplifiers  
 $n$  is the number of phases  
 $V_{OS\_EA}$  is the offset voltage of the error amplifier (- to + pin)  
 $V_{O\_NLOFST}$  is the desired no load offset voltage below the DAC setting  
 $R_o$  is the desired load line resistance  
 $V_{CS\_TOFST}$  is the total offset voltage of the current sense amplifiers, see below.

The **total** input offset voltage ( $V_{CS\_TOFST}$ ) of the current sense amplifier in the phase IC is the sum of input offset ( $V_{CS\_OFST}$ ) of the amplifier itself plus that created by the amplifier input bias currents flowing through the current sense resistors  $R_{CS+}$  and  $R_{CS-}$  as shown in Equation (6).

$$V_{CS\_TOFST} = V_{CS\_OFST} + (I_{CSIN+} * R_{CS+}) - (I_{CSIN-} * R_{CS-}) \quad (6)$$

Finally, calculate the no-load setpoint resistor using Equation (7) and the droop resistor using Equation (8);

$$RVSETPT = \frac{VSETPT}{I_{VSETPT}} \quad (7)$$

**Where:**  $I_{VSETPT}$  is the current into the VSETPT pin at the switching frequency which is a function of  $R_{OSC}$ , see Figure 15 on page 6.  
 $VSETPT$  is calculated by Equation (5).

$$RDRP = RFB \cdot \frac{VSETPT + C}{D - VSETPT} \quad (8)$$

### Soft Start Capacitor $C_{SS/DEL}$ and Resistor $R_{SS/DEL}$

Because the capacitor  $C_{SS/DEL}$  programs three different time parameters, i.e. soft start time, over current latch delay time, and the frequency of hiccup mode, they should be considered together while choosing  $C_{SS/DEL}$ .

The soft-start ramp time (TD2) is the time required for the converter's output voltage to rise from 0V to the DAC voltage (VDAC). Given a desired soft-start ramp time (TD2) and the soft-start charge current ( $I_{CHG}$ ) from the data sheet, the value of the external capacitor ( $C_{SS/DEL}$ ) can be calculated using Equation (9).

$$C_{SS/DEL} = \frac{I_{CHG} * TD2}{VDAC * \left(1 - \frac{RFB}{RFB + RDRP}\right)} = \frac{70 * 10^{-6} * TD2}{VDAC * \left(1 - \frac{RFB}{RFB + RDRP}\right)} \quad (9)$$

Where: VDAC = 1.1V in Boot Mode or the DAC voltage set by the VID pins without Boot Mode.

RFB is the resistor from Vcore to the FB pin of the controller.

RDRP is the resistor from VDRP to FB.

If droop is not used, set the second term within the parenthesis to zero ( $RDRP = \infty$ ).

Once  $C_{SS/DEL}$  is determined, the soft start delay time TD1, the VID sample time TD3, the VRRDY delay time TD5, and the over-current fault latch delay time  $T_{OCDEL}$  are determined and can be calculated using Equations (10), (11), (12), and (13) respectively.

$$TD1 = \frac{C_{SS/DEL}}{I_{CHG}} * \left(1.3V + VDAC * \frac{RFB}{RFB + RDRP}\right) \quad (10)$$

Where: VDAC = 1.1V in Boot Mode or the DAC voltage set by the VID pins without Boot Mode.

ICHG is the soft-start charge current, nominally 70μA.

RFB is the resistor from Vcore to the FB pin of the controller.

RDRP is the resistor from VDRP to FB.

If droop is not used, set the second term within the parenthesis to zero ( $RDRP = \infty$ ).

$$TD3 = \frac{C_{SS/DEL}}{I_{CHG}} * (3.1V - 1.3V - 1.1V) = \frac{C_{SS/DEL}}{70 * 10^{-6}} * 0.7V \quad (11)$$

If Boot Mode is not used, then TD3 is zero.

$$TD5 = \frac{C_{SS/DEL} * (3.85V - 3.1V)}{I_{CHG}} - TD4 = \frac{C_{SS/DEL} * 0.75V}{70 * 10^{-6}} - TD4 \quad (12)$$

Where: TD4 is the VID voltage rise time calculated from Equation 4.

$$T_{OCDEL} = \frac{C_{SS/DEL} * 100mV}{I_{OC\_DISCHG}} = \frac{C_{SS/DEL} * 100mV}{40 * 10^{-6}} \quad (13)$$

Where:  $I_{OC\_DISCHG}$  is the over-current discharge current of the SS/DEL pin from the data sheet.

### Over Current Setting Resistor $R_{OCSET}$

The inductor DC resistance is utilized to sense the inductor current. The copper wire of the inductor has a constant temperature coefficient of 3850 PPM, and therefore the maximum inductor DCR can be calculated from Equation (14), where  $R_{L\_MAX}$  and  $R_{L\_ROOM}$  are the inductor DCR at maximum temperature  $T_{L\_MAX}$  and room temperature  $T_{ROOM}$  respectively.

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850 * 10^{-6} * (T_{L\_MAX} - T_{ROOM})] \quad (14)$$

The current sense amplifier gain of the IR3086A decreases with temperature at the rate of 1470 PPM, which compensates part of the inductor DCR increase. The phase IC die temperature is only a couple of degrees Celsius higher than the PCB temperature due to the low thermal impedance of MLPQ package. The minimum current sense amplifier gain at the maximum phase IC temperature  $T_{IC\_MAX}$  is calculated from Equation (15).

$$G_{CS\_MIN} = G_{CS\_ROOM} * [1 - 1470 * 10^{-6} * (T_{IC\_MAX} - T_{ROOM})] \quad (15)$$

The over-current limit is set by the external resistor  $R_{OCSET}$  as defined in Equation (16), where  $I_{LIMIT}$  is the required over current limit.  $I_{OCSET}$ , the bias current of the OCSET pin, changes with switching frequency setting resistor  $R_{OSC}$  and is determined by the curve in Figure 14 on page 6.  $K_P$  is the ratio of inductor peak current to average current in each phase and is calculated from Equation (17).

$$R_{OCSET} = \left[ \frac{I_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST} \right] * \frac{G_{CS\_MIN}}{I_{OCSET}} \quad (16)$$

$$K_P = \frac{(V_I - V_{O\_FL}) * V_{O\_FL} / (L * V_I * f_{SW} * 2)}{I_{LIMIT} / n} \quad (17)$$

Where:  $V_I$  is the input voltage to the converter (nominally 12V).

$V_{O\_FL}$  is the output voltage of the converter with droop at the over-current threshold.

$L$  is the value of the output inductors.

$f_{SW}$  is the switching frequency.

$I_{LIMIT}$  is the DC output current of the converter when the over-current fault occurs.

$n$  is the number of phases.

## IR3086 EXTERNAL COMPONENTS

### PWM Ramp Resistor $R_{PWMRMP}$ and Capacitor $C_{PWMRMP}$

PWM ramp is generated by connecting the resistor  $R_{PWMRMP}$  between a voltage source and  $PWMRMP$  pin as well as the capacitor  $C_{PWMRMP}$  between  $PWMRMP$  and  $LGND$ . Choose the desired PWM ramp magnitude  $V_{RAMP}$  and the capacitor  $C_{PWMRMP}$  in the range of 100pF and 470pF, and then calculate the resistor  $R_{PWMRMP}$  from Equation (18). To achieve feed-forward voltage mode control, the resistor  $R_{RAMP}$  should be connected to the input of the converter.

$$R_{PWMRMP} = \frac{V_O}{V_{IN} * f_{SW} * C_{PWMRMP} * [\ln(V_{IN} - V_{DAC}) - \ln(V_{IN} - V_{DAC} - V_{PWMRMP})]} \quad (18)$$

### Inductor Current Sensing Capacitor $C_{CS+}$ and Resistors $R_{CS+}$ and $R_{CS-}$

The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor  $R_{CS+}$  and capacitor  $C_{CS+}$  in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor  $C_{CS+}$  represents the inductor current. If the two time constants are not the same, the AC component of the capacitor voltage is different from that of the real inductor current. The time constant mismatch does not affect the average current sharing among the multiple phases, but affect the current signal  $ISHARE$  as well as the output voltage during the load current transient if adaptive voltage positioning is adopted.

Measure the inductance  $L$  and the inductor DC resistance  $R_L$ . Pre-select the capacitor  $C_{CS+}$  and calculate  $R_{CS+}$  as follows.

$$R_{CS+} = \frac{L/R_L}{C_{CS+}} \quad (19)$$

The bias current flowing out of the non-inverting input of the current sense amplifier creates a voltage drop across  $R_{CS+}$ , which is equivalent to an input offset voltage of the current sense amplifier. The offset affects the accuracy of converter current signal  $ISHARE$  as well as the accuracy of the converter output voltage if adaptive voltage positioning is adopted. To reduce the offset voltage, a resistor  $R_{CS-}$  should be added between the amplifier inverting input and the converter output. The resistor  $R_{CS-}$  is determined by the ratio of the bias current from the non-inverting input and the bias current from the inverting input.

$$R_{CS-} = \frac{I_{CSIN+}}{I_{CSIN-}} * R_{CS+} \quad (20)$$

If  $R_{CS-}$  is not used,  $R_{CS+}$  should be chosen so that the offset voltage is small enough. Usually  $R_{CS+}$  should be less than 2 kΩ and therefore a larger  $C_{CS+}$  value is needed.

### Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2*

The threshold voltage of VRHOT comparator is proportional to the die temperature  $T_J$  (°C) of phase IC. Determine the relationship between the die temperature of phase IC and the temperature of the power converter according to the power loss, PCB layout and airflow etc, and then calculate HOTSET threshold voltage corresponding to the allowed maximum temperature from Equation (21).

$$V_{HOTSET} = 4.73 * 10^{-3} * T_J + 1.241 \quad (21)$$

There are two ways to set the over temperature threshold, central setting and local setting. In the central setting, only one resistor divider is used, and the setting voltage is connected to HOTSET pins of all the phase ICs. To reduce the influence of noise on the accuracy of over temperature setting, a 0.1uF capacitor should be placed next to HOTSET pin of each phase IC. In the local setting, a resistor divider per phase is needed, and the setting voltage is connected to HOTSET pin of each phase. The 0.1uF decoupling capacitor is not necessary. Use VBIAS as the reference voltage. If RHOTSET1 is pre-selected, RHOTSET2 can be calculated as follows.

$$R_{HOTSET2} = \frac{R_{HOTSET1} * V_{HOTSET}}{V_{BIAS} - V_{HOTSET}} \quad (22)$$

### Phase Delay Timing Resistors *RPHASE1* and *RPHASE2*

The phase delay of the interleaved multiphase converter is programmed by the resistor divider connected at RMPIN+ or RMPIN- depending on which slope of the oscillator ramp is used for the phase delay programming of phase IC, as shown in Figure 4.

If the positive slope is used, RMPIN+ pin of the phase IC should be connected to RMPOUT pin of the control IC and RMPIN- pin should be connected to the resistor divider. When RMPOUT voltage is above the trip voltage at RMPIN- pin, the PWM latch is set. GATEL becomes low, and GATEH becomes high after the non-overlap time.

If the negative slope is used, RMPIN- pin of the phase IC should be connected to RMPOUT pin of the control IC and RMPIN+ pin should be connected to the resistor divider. When RMPOUT voltage is below the trip voltage at RMPIN- pin, the PWM latch is set. GATEL becomes low, and GATEH becomes high after the non-overlap time.

It is best to use the VBIAS voltage as the reference for the resistor dividers because the oscillator ramp magnitude from the control IC will track the VBIAS voltage. It is best to avoid the peak and valley of the oscillator ramp for better noise immunity. Determine the ratio of the programming resistors corresponding to the desired switching frequencies and phase numbers. If the resistor RPHASEx1 is pre-selected, the resistor RPHASEx2 is determined as:

$$R_{PHASEx2} = \frac{RA_{PHASEx} * R_{PHASEx1}}{1 - RA_{PHASEx}} \quad (23)$$

### Combining the Over Temperature and Phase Delay Setting Resistors $R_{PHASE1}$ , $R_{PHASE2}$ and $R_{PHASE3}$

The over temperature setting resistor divider can be combined with the phase delay resistor divider to save one resistor per phase.

Calculate the HOTSET threshold voltage  $V_{HOTSET}$  corresponding to the allowed maximum temperature from Equation (20). If the over temperature setting voltage is lower than the phase delay setting voltage,  $V_{BIAS} * R_{PHASEx}$ , connect RMPIN+ or RMPIN- pin between  $R_{PHASEx1}$  and  $R_{PHASEx2}$  and connect HOTSET pin between  $R_{PHASEx2}$  and  $R_{PHASEx3}$  respectively. Pre-select  $R_{PHASEx1}$ , then calculate  $R_{PHASEx2}$  and  $R_{PHASEx3}$ ,

$$R_{PHASEx2} = \frac{(R_{PHASEx} * V_{BIAS} - V_{HOTSET}) * R_{PHASEx1}}{V_{BIAS} * (1 - R_{PHASEx})} \quad (24)$$

$$R_{PHASEx3} = \frac{V_{HOTSET} * R_{PHASEx1}}{V_{BIAS} * (1 - R_{PHASEx})} \quad (25)$$

If the over temperature setting voltage is higher than the phase delay setting voltage,  $V_{BIAS} * R_{PHASEx}$ , connect HOTSET pin between  $R_{PHASEx1}$  and  $R_{PHASEx2}$  and connect RMPIN+ or RMPIN- between  $R_{PHASEx2}$  and  $R_{PHASEx3}$  respectively. Pre-select  $R_{PHASEx1}$ ,

$$R_{PHASEx2} = \frac{(V_{HOTSET} - R_{PHASEx} * V_{BIAS}) * R_{PHASEx1}}{V_{BIAS} - V_{HOTSET}} \quad (26)$$

$$R_{PHASEx3} = \frac{R_{PHASEx} * V_{BIAS} * R_{PHASEx1}}{V_{BIAS} - V_{HOTSET}} \quad (27)$$

### Bootstrap Capacitor $C_{BST}$

Depending on the duty cycle and gate drive current of the phase IC, a 0.1uF to 1uF capacitor is needed for the bootstrap circuit.

### Decoupling Capacitors for Phase IC

0.1uF–1uF decoupling capacitors are required at VCC and VCCL pins of phase ICs.

## VOLTAGE LOOP COMPENSATION

The adaptive voltage positioning is used in the computer applications to meet the load line requirements. Like current mode control, the adaptive voltage positioning loop introduces extra zero to the voltage loop and splits the double poles of the power stage, which make the voltage loop compensation much easier.

Resistors  $R_{FB}$  and  $R_{DRP}$  are chosen according to Equations (15) and (16), and the selection of compensation type depends on the capacitors used. For the applications using Electrolytic, Polymer or AL-Polymer capacitors, type II compensation shown in Figure 20 (a) is usually enough. While for the applications with only ceramic capacitors, type III compensation shown in Figure 20 (b) is preferred.

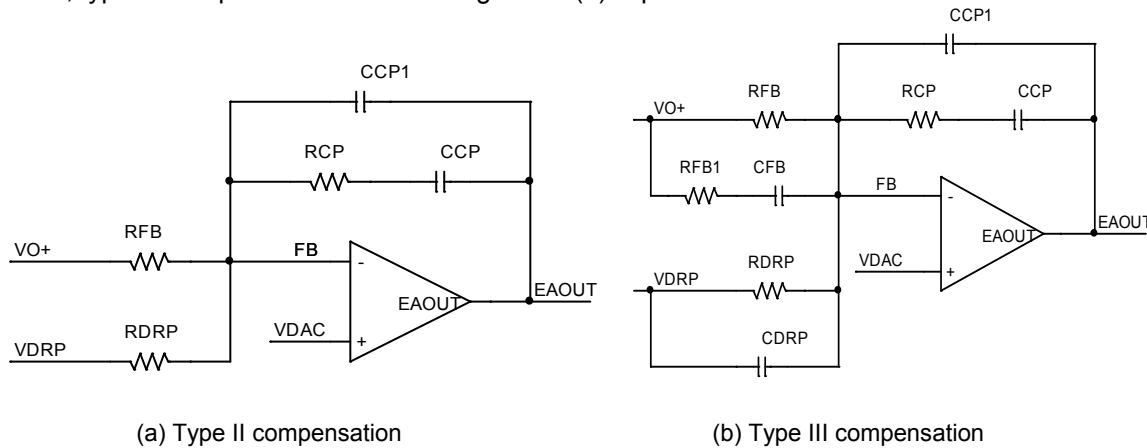


Figure 20: Voltage Loop Compensation Networks

### Type II Compensation

Determine the compensation at no load, the worst case condition. Choose the crossover frequency  $f_c$  between 1/10 and 1/5 of the switching frequency per phase. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor,  $R_{CP}$  and  $C_{CP}$  can be determined by Equations (28) and (29).

$$R_{CP} = \frac{(2\pi * f_c)^2 * L_E * C_E * R_{FB} * V_{PWMRMP}}{V_O * \sqrt{1 + (2\pi * f_c * C_E * R_{CE})^2}} \quad (28)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (29)$$

Where  $L_E$  and  $R_{CE}$  are the equivalent output inductance and ESR of the output capacitors, respectively.  $CCP1$  is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

### Type III Compensation

Determine the compensation at no load, the worst case condition. Choose the crossover frequency  $f_c$  between 1/10 and 1/5 of the switching frequency per phase. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor,  $R_{CP}$  and  $C_{CP}$  can be determined by Equations (30) and (31), where  $C_E$  is equivalent output capacitance.

$$R_{CP} = \frac{(2\pi * f_c)^2 * L_E * C_E * V_{PWMRMP}}{V_o} \quad (30)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (31)$$

Choose resistor  $R_{FB1}$  according to Equation (33), and determine  $C_{FB}$  and  $R_{DRP}$  from Equations (32) and (33).

$$R_{FB1} = \frac{1}{2} * R_{FB} \quad \text{to} \quad R_{FB1} = \frac{2}{3} * R_{FB} \quad (32)$$

$$C_{FB} = \frac{1}{4\pi * f_{CI} * R_{FB1}} \quad (33)$$

$CCP1$  is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

### CURRENT SHARE LOOP COMPENSATION

The crossover frequency of the current share loop should be at least one decade lower than that of the voltage loop in order to eliminate the interaction between the two loops. A capacitor from  $SCOMP$  to  $LGND$  is usually enough for most of the applications. Choose the crossover frequency of current share loop ( $f_{CI}$ ) based on the crossover frequency of voltage loop ( $f_c$ ), and determine the  $C_{SCOMP}$ ,

$$C_{SCOMP} = \frac{0.65 * R_{PWMRMP} * V_I * I_O * G_{CS\_ROOM} * R_{LE} * [1 + 2\pi * f_{CI} * C_E * (V_O / I_O)] * F_{MI}}{V_O * 2\pi * f_{CI} * 1.05 * 10^6} \quad (34)$$

Where  $F_{MI}$  is the PWM gain in the current share loop,

$$F_{MI} = \frac{R_{PWMRMP} * C_{PWMRMP} * f_{SW} * V_{PWMRMP}}{(V_O - V_{PWMRMP} - V_{DAC}) * (V_I - V_{DAC})} \quad (35)$$

## DESIGN EXAMPLE: VRM 11 7-PHASE CONVERTER

### SPECIFICATIONS

Input Voltage:  $V_I = 12V$   
 DAC Voltage:  $V_{DAC} = 1.3V$   
 No Load Output Voltage Offset:  $V_{O\_NLOFST} = 15mV$   
 Output Current:  $I_O = 130\text{ ADC}$   
 Maximum Output Current:  $I_{OMAX} = 150\text{ ADC}$   
 Load Line Slope:  $R_O = 1.20\text{ m}\Omega$   
 VRM11 Startup Boot Voltage =  $1.100V$   
 Soft Start Time:  $TD2 = 1.1ms$   
 VCC Ready to VCC Power Good Delay:  $TD5 = 1.0ms$   
 Over Current Delay:  $TOCDEL = 250\mu s$   
 Dynamic VID Negative Slew Rate:  $SR_{DOWN} = 2.5mV/\mu s$   
 Over Temperature Threshold:  $TPCB = 115\text{ }^\circ C$

### POWER STAGE

Phase Number:  $n = 7$   
 Switching Frequency:  $f_{sw} = 400\text{ kHz}$   
 Output Inductors:  $L = 220\text{ nH}$ ,  $R_L = 0.60\text{ m}\Omega$   
 Output Capacitors:  $C = 560\mu F$ ,  $R_C = 7m\Omega$ , Number  $C_n = 10$

## IR3084 EXTERNAL COMPONENTS

### Oscillator Resistor $R_{osc}$

The switching frequency sets the value of  $R_{OSC}$  as shown by the curve in Figure 13 on page 6. In this design, the switching frequency of 400kHz per phase requires  $R_{OSC}$  to be 30.1k $\Omega$ .

### VDAC Slew Rate Programming Capacitor $C_{VDAC}$ and Resistor $R_{VDAC}$

From Figure 17 on page 6, the sink current of the VDAC pin at 400kHz ( $R_{OSC} = 30.1k\Omega$ ) is 80uA. Calculate the VDAC slew-rate programming capacitor from the specified negative slew rate using Equation (1).

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{80 * 10^{-6}}{2.5 * 10^{-3} / 10^{-6}} = 32.0nF, \quad \text{Choose } C_{VDAC} = 33nF$$

Calculate the VDAC compensation resistor from Equation (2);

$$R_{VDAC} = 0.5 + \frac{3.2 * 10^{-15}}{C_{VDAC}^2} = 0.5 + \frac{3.2 * 10^{-15}}{(33 * 10^{-9})^2} = 3.5\Omega$$

From Figure 17 on page 6, the source current of the VDAC pin is 90uA at  $R_{OSC} = 30.1K\Omega$ . The VDAC positive slew rate is can be calculated using Equation (3);

$$SR_{UP} = \frac{I_{SOURCE}}{C_{VDAC}} = \frac{90 * 10^{-6}}{33 * 10^{-9}} = 2.7mV/\mu S$$

Using the calculated value of  $C_{VDAC}$ , find the positive VID voltage rise time (TD4) to the specified nominal DAC voltage of 1.300V during startup with Boot Mode using Equation 4a;

$$TD4 = \frac{C_{VDAC}}{I_{SOURCE}} * (VDAC - 1.1V) = \frac{33nF}{90uA} * (1.300V - 1.1V) = 73.3us$$

#### No Load Output Voltage Setting Resistor RVSETPT, RFB and Adaptive Voltage Positioning Resistor RDRP

First, use Equations (19) and (20) to calculate the current sense resistors  $R_{CS+}$  and  $R_{CS-}$ , respectively. For this design, in the next section,  $R_{CS+}$  is determined to be 10KΩ and  $R_{CS-}$  is found to be 6.19KΩ.

Second, calculate the total input offset voltage ( $V_{CS\_TOFST}$ ) of the current sense amplifiers using Equation (6). From the IR3086A data sheet, typical values for the  $I_{CSIN+}$  and  $I_{CSIN-}$  bias currents are determined to be 0.25μA and 0.40μA, respectively.

$$\begin{aligned} V_{CS\_TOFST} &= V_{CS\_OFST} + (I_{CSIN+} * R_{CS+}) - (I_{CSIN-} * R_{CS-}) \\ &= 0.55mV + (0.25 * 10^{-6} * 10K\Omega) - (0.40 * 10^{-6} * 6.19K\Omega) = 0.574mV \end{aligned}$$

Next, derive the intermediate calculations (A,B,C,D) as shown below before finally calculating  $R_{VSETPT}$  and RDRP using Equations (7) and (8). From Figure 15 on page 6, the  $I_{VSETPT}$  bias current is determined to be 40μA at  $R_{OSC}=30.1k\Omega$  and a typical value for the offset voltage of the error amplifier is 0.0mV.

$$\begin{aligned} A &= \frac{I_o * R_L * G_{CSA}}{n} + V_{CS\_TOFST} * G_{CSA} + V_{OS\_EA} = \frac{130 * 0.60 * 10^{-3} * 34}{7} + 0.574 * 10^{-3} * 34 + 0.0mV \\ &= 0.3984 \end{aligned}$$

$$B = V_{O\_NLOFST} + I_o * R_o - V_{OS\_EA} = 15 * 10^{-3} + 130 * 1.20 * 10^{-3} - 0.0mV = 0.1710$$

$$C = V_{CS\_TOFST} * G_{CSA} + V_{OS\_EA} = 0.574 * 10^{-3} * 34 + 0.0mV = 0.0195$$

$$D = V_{O\_NLOFST} - V_{OS\_EA} = 15 * 10^{-3} - 0.0mV = 0.015$$

$$V_{SETPT} = \frac{A * D - C * B}{(A + B - C - D)} = \frac{0.3984 * 0.015 - 0.0195 * 0.1710}{0.3984 + 0.1710 - 0.0195 - 0.015} = 0.00494V$$

$$RV_{SETPT} = \frac{V_{SETPT}}{I_{VSETPT}} = \frac{0.00494}{40 * 10^{-6}} = 123.5ohms$$

Choose the closest standard resistor value to this with 1% tolerance or RVESTPT = 124ohms.

Select  $RFB = 324$  ohms and then calculate the droop resistor,

$$RDRP = RFB \cdot \frac{VSETPT + C}{D - VSETPT} = 324 \cdot \frac{0.00494 + 0.0195}{0.015 - 0.00494} = 787.1ohms$$

Choose the next standard value higher than this with 1% tolerance or  $RDRP = 787ohms$ .

### Soft Start Capacitor $C_{SS/DEL}$ and Startup Times

Calculate the soft start capacitor from the required soft start time using Equation (9) with Boot Mode;

$$C_{SS/DEL} = \frac{70 * 10^{-6} * TD2}{VDAC * \left(1 - \frac{RFB}{RFB + RDRP}\right)} = \frac{70 * 10^{-6} * 1.1 * 10^{-3}}{1.1V * \left(1 - \frac{324}{324 + 787}\right)} = 0.0988uF \text{ or } 0.1uF$$

The soft start delay time can be calculated using Equation (10) with Boot Mode;

$$TD1 = \frac{C_{SS/DEL}}{I_{CHG}} * \left(1.3V + VDAC * \frac{RFB}{RFB + RDRP}\right) = \frac{0.1 * 10^{-6}}{70 * 10^{-6}} * \left(1.3V + 1.1V * \frac{324}{324 + 787}\right) \\ = 2.31ms$$

The VID sample time can be found using Equation (11);

$$TD3 = \frac{C_{SS/DEL} * 0.7V}{I_{CHG}} = \frac{0.1 * 10^{-6} * 0.7}{70 * 10^{-6}} = 1.00mS$$

The power good delay time can be found using Equation (12);

$$TD5 = \frac{C_{SS/DEL} * 0.75V}{I_{CHG}} - TD4 = \frac{0.1 * 10^{-6} * 0.75V}{70 * 10^{-6}} - 73us = 0.998ms$$

Finally, use Equation (13) to calculate the over-current fault latch delay time;

$$T_{OCDEL} = \frac{C_{SS/DEL} * 100mV}{40 * 10^{-6}} = \frac{0.1 * 10^{-6} * 100 * 10^{-3}}{40 * 10^{-6}} = 250us$$

### Over Current Setting Resistor $R_{OCSET}$

Assume that room temperature is 25°C and the target PCB temperature is 100 °C. The phase IC die temperature is usually about 1 °C higher than that of phase IC and the inductor temperature is close to PCB temperature.

Calculate the Inductor's DC resistance at 100 °C using Equation (14);

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850 * 10^{-6} * (T_{L\_MAX} - T_{ROOM})] = 0.60 * 10^{-3} * [1 + 3850 * 10^{-6} * (100 - 25)] = 0.77 m\Omega$$

The current sense amplifier gain is 34 at 25°C, and its gain at 101°C is calculated using Equation (15),

$$G_{CS\_MIN} = G_{CS\_ROOM} * [1 - 1470 * 10^{-6} * (T_{IC\_MAX} - T_{ROOM})] = 34 * [1 - 1470 * 10^{-6} * (101 - 25)] = 30.2$$

Here we will set the over current shutdown threshold to 155A at maximum operating temperature. From Figure 14 on page 6, the bias current of the OCSET pin (IOCSET) is 42.5µA with ROSC=30.1kΩ. The total current sense amplifier input offset voltage calculated previously is 0.574mV, which includes the offset created by the current sense amplifier input resistor mismatch.

Calculate the constant  $K_P$ , the ratio of inductor peak current over average current in each phase using Equation (17);

$$K_P = \frac{(V_I - V_O) * V_O / (L * V_I * f_{SW} * 2)}{I_{LIMIT} / n} = \frac{(12 - 1.18) * 1.18 / (220 * 10^{-9} * 12 * 400 * 10^3 * 2)}{155 / 7} = 0.273$$

Finally, calculate the over-current setting resistor using Equation (16);

$$R_{OCSET} = \left[ \frac{R_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST} \right] * \frac{G_{CS\_MIN}}{I_{OCSET}}$$

$$= \left( \frac{155}{7} * 0.77 * 10^{-3} * (1 + 0.273) + 0.574 * 10^{-3} \right) * \frac{30.2}{42.5 * 10^{-6}} = 15.8 K\Omega$$

## IR3086 PHASE IC COMPONENTS

### PWM Ramp Resistor $R_{RAMP}$ and Capacitor $C_{RAMP}$

Set the PWM ramp magnitude  $V_{PWRMP}$  to 0.8V. Choose 220pF for the PWM ramp capacitor  $C_{PWRMP}$  and calculate the resistor  $R_{PWRMP}$  using Equation (18);

$$R_{PWRMP} = \frac{V_o}{V_{IN} * f_{SW} * C_{PWRMP} * [\ln(V_{IN} - V_{DAC}) - \ln(V_{IN} - V_{DAC} - V_{PWRMP})]}$$

$$= \frac{1.30}{12 * 400 * 10^3 * 220 * 10^{-12} * [\ln(12 - 1.30) - \ln(12 - 1.30 - 0.8)]} = 15.8k\Omega ,$$

Choose a standard resistor value,  $R_{PWRMP}=15.8k\Omega$ .

### Inductor Current Sensing Capacitor $C_{CS+}$ and Resistors $R_{CS+}$ and $R_{CS-}$

Choose  $C_{CS+}=47nF$  and calculate  $R_{CS+}$  using Equation (19);

$$R_{CS+} = \frac{L/R_L}{C_{CS+}} = \frac{220 * 10^{-9} / (0.47 * 10^{-3})}{47 * 10^{-9}} = 10.0k\Omega$$

The bias currents of  $CSIN+$  and  $CSIN-$  are 0.25uA and 0.4uA respectively. Calculate resistor  $R_{CS-}$  using Equation (20);

$$R_{CS-} = \frac{0.25}{0.4} * R_{CS+} = \frac{0.25}{0.4} * 10.0 * 10^3 = 6.2k\Omega , \quad \text{choose } R_{CS-} = 6.19k\Omega$$

### Over Temperature Setting Resistors $R_{HOTSET1}$ and $R_{HOTSET2}$

Use central over temperature setting and set the temperature threshold at 115 °C, which corresponds the IC die temperature of 116 °C. Calculate the HOTSET threshold voltage corresponding to the temperature thresholds using Equations (21) and (22);

$$V_{HOTSET} = 4.73 * 10^{-3} * T_J + 1.241 = 4.73 * 10^{-3} * 116 + 1.241 = 1.79V , \text{ choose } R_{HOTSET1}=20.0k\Omega ,$$

$$R_{HOTSET2} = \frac{R_{HOTSET1} * V_{HOTSET}}{V_{BIAS} - V_{HOTSET}} = \frac{20 * 10^3 * 1.79}{6.8 - 1.79} = 7.14k\Omega$$

### Phase Delay Timing Resistors $R_{PHASEx1}$ to $R_{PHASEx2}$ ( $x=1,2,\dots,7$ )

The phase delay resistor ratios for phases 1 to 7 at 400kHz are (from the X-Phase Excel based design spreadsheet); RAPHASE1=0.580, RAPHASE2=0.397, RAPHASE3=0.215, RAPHASE4=0.206, RAPHASE5=0.353 RAPHASE6=0.5 and RAPHASE7=0.647.

Pre-select  $R_{PHASE11}=R_{PHASE21}=R_{PHASE31}=R_{PHASE41}=R_{PHASE51}=R_{PHASE61}=R_{PHASE71}=20k\Omega$ ,

$$R_{PHASE12} = \frac{RA_{PHASE1}}{1 - RA_{PHASE1}} * R_{PHASE11} = \frac{0.58}{1 - 0.58} * 20 * 10^3 = 27.6k\Omega$$

Calculating the other resistors from the same formula results in;  $R_{PHASE22}=13.2k\Omega$ ,  $R_{PHASE32}=5.48k\Omega$ ,  $R_{PHASE42}=5.2k\Omega$ ,  $R_{PHASE52}=10.9k\Omega$ ,  $R_{PHASE62}=20k\Omega$ ,  $R_{PHASE72}=36.6k\Omega$ .

Phase ICs 1–3 should have the RMPOUT voltage from the 3084 controller connected to their RMPIN– pin so they will trigger on the negative slope of the RMPOUT waveform. Phase ICs 4–7 should have the RMPOUT voltage from the 3084 controller connected to their RMPIN+ pin so they will trigger on the positive slope of the RMPOUT waveform.

### Bootstrap Capacitor CBST

Choose  $CBST=0.1\mu F$ .

### Decoupling Capacitors for Phase IC and Power Stage

Choose  $CVCC=0.1\mu F$ ,  $CVCCCL=0.1\mu F$

## VOLTAGE LOOP COMPENSATION

AL-Polymer output capacitors are used in the design, for instructional purposes Type III compensation as shown in Figure 18(b) will be demonstrated here. First, choose the desired crossover frequency as 1/10 of the switching frequency,  $f_c = 40$  kHz, and determine  $R_{CP}$  and  $C_{CP}$  using Equations (30) and (31):

$$R_{CP} = \frac{(2\pi * f_c)^2 * L_E * C_E * R_{FB} * V_{PWMRMP}}{V_o} = \frac{(2\pi * 40 * 10^3)^2 * (220 * 10^{-9} / 7) * (560 * 10^{-6} * 10) * 324 * 0.8}{1.30 - 0.015 - 130 * 1 * 10^{-3}} = 2.49K\Omega$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} = \frac{10 * \sqrt{(220 * 10^{-9} / 7) * (560 * 10^{-6} * 10)}}{2.49 * 10^3} = 53nF, \quad \text{Choose } C_{CP}=56nF$$

$$R_{FB1} = \frac{1}{2} * R_{FB} = \frac{1}{2} * 324 = 162\Omega \quad \text{Choose } R_{FB1}=162\Omega$$

$$C_{FB} = \frac{1}{4\pi * f_c * R_{FB1}} = \frac{1}{4\pi * 40 * 10^3 * 162} = 12.3nF \quad \text{Choose } C_{FB}=10nF$$

Choose  $CCP1=100pF$  to reduce high frequency noise.

## CURRENT SHARE LOOP COMPENSATION

The crossover frequency of the current share loop ( $f_{CI}$ ) should be at least one decade lower than that of the voltage loop  $f_C$ . Choose the crossover frequency of current share loop  $f_{CI}$  =4kHz, and calculate FMI and CCOMP using Equations (34) and (35);

$$F_{MI} = \frac{R_{PWRMP} * C_{PWRMP} * f_{SW} * V_{PWRMP}}{(V_I - V_{PWRMP} - V_{DAC}) * (V_I - V_{DAC})} = \frac{15.8 * 10^3 * 220 * 10^{-12} * 400 * 10^3 * 0.8}{(12 - 0.8 - 1.30) * (12 - 1.30)} = 0.0105$$

$$C_{SCOMP} = \frac{0.65 * R_{PWRMP} * V_I * I_O * G_{CS\_ROOM} * R_{LE} * [1 + 2\pi * f_{CI} * C_E * (V_O / I_O)] * F_{MI}}{V_O * 2\pi * f_{CI} * 1.05 * 10^6}$$

$$= \frac{0.65 * 15.8 * 10^3 * 12 * 130 * 34 * (0.47 * 10^{-3} / 7) * [1 + 2\pi * 4 * 10^3 * 5600 * 10^{-6} * (1.30 - 130 * 1.0 * 10^{-3}) / 130] * 0.0105}{(1.30 - 130 * 1.0 * 10^{-3}) * 2\pi * 4 * 10^3 * 1.05 * 10^6}$$

$$= \frac{36574 * [2.266] * 0.0105}{30.859 * 10^9}$$

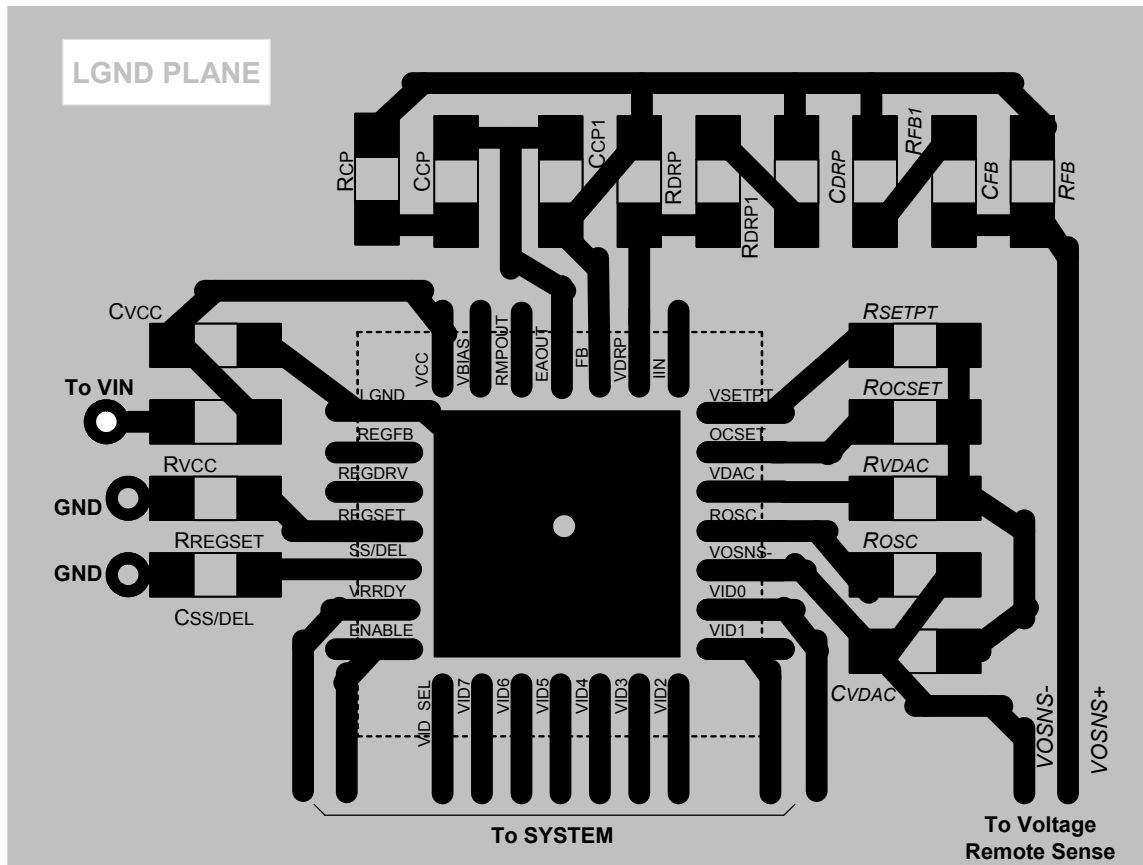
$$= 28.2nF$$

Choose CCOMP=22nF with 5% tolerance for best current sharing between phases.

## LAYOUT GUIDELINES

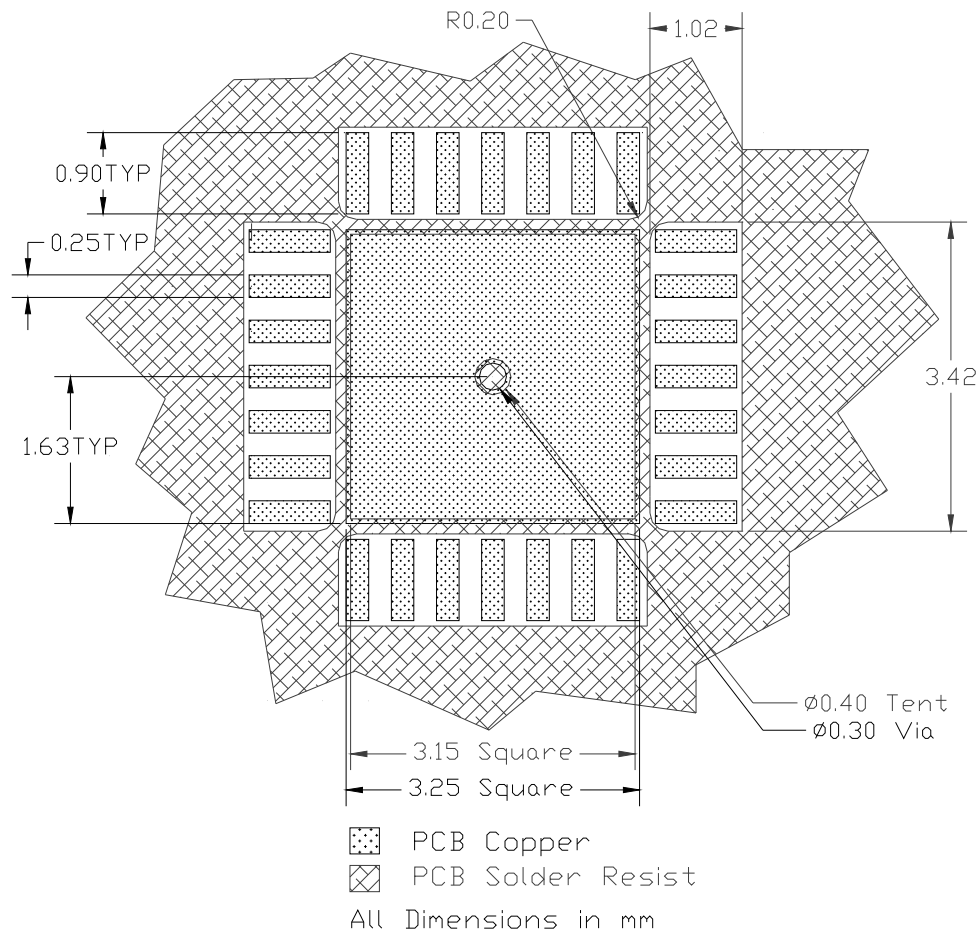
The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout, therefore minimizing the noise coupled to the IC.

- Dedicate at least one middle layer for a ground plane LGND.
- Connect the ground tab under the control IC to LGND plane through a via.
- Place the following critical components on the same layer as control IC and position them as close as possible to the respective pins, ROSC, ROCSET, RVDAC, CVDAC, CVCC, CSS/DEL and RCC/DEL. Avoid using any via for the connection.
- Place the compensation components on the same layer as control IC and position them as close as possible to EAOUT, FB and VDRP pins. Avoid using any via for the connection.
- Use Kelvin connections for the remote voltage sense signals, VOSNS+ and VOSNS-, and avoid crossing over the fast transition nodes, i.e. switching nodes, gate drive signals and bootstrap nodes.
- Control bus signals, VDAC, RMPOUT, IIN, VBIAS, and especially EAOUT, should not cross over the fast transition nodes.



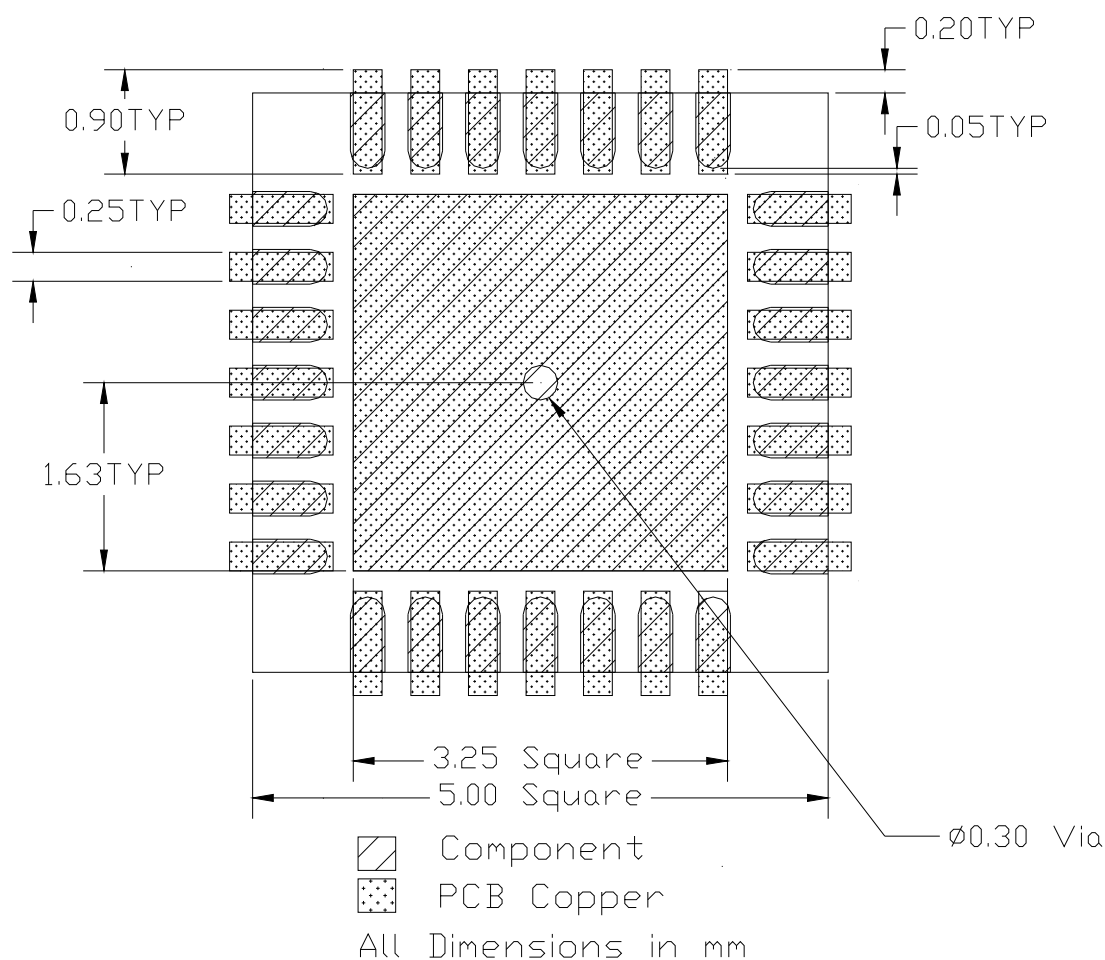
## METAL AND SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm, therefore it is recommended that the solder resist is completely removed from between the lead lands forming a single opening for each “group” of lead lands.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of  $\geq 0.17\text{mm}$  remains.
- The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist mis-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
- Ensure that the solder resist in-between the lead lands and the pad land is  $\geq 0.15\text{mm}$  due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The single via in the land pad should be tented with solder resist 0.4mm diameter, or 0.1mm larger than the diameter of the via.



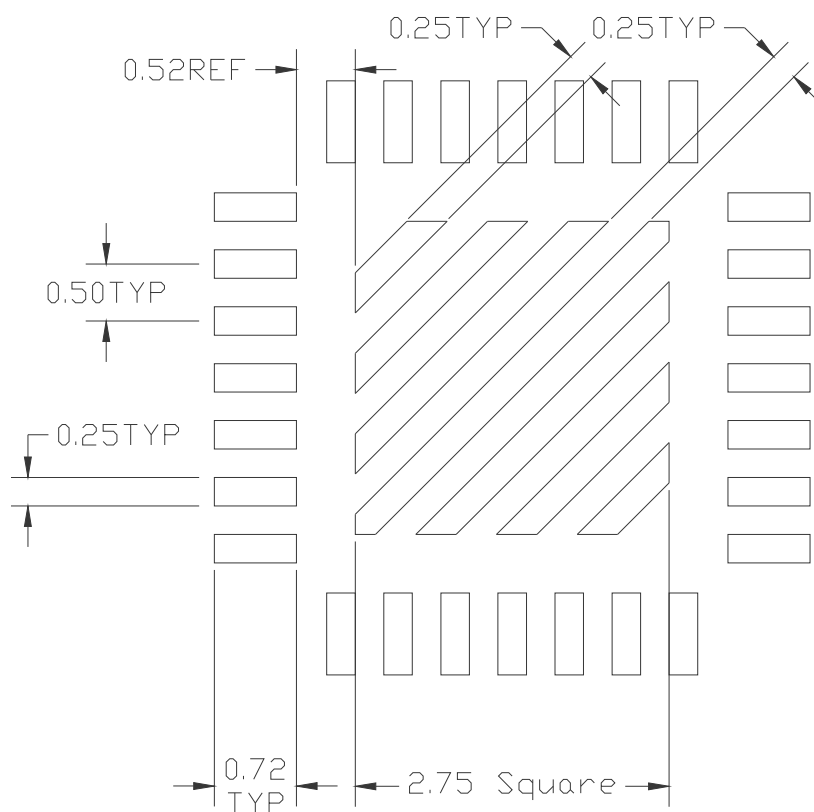
## PCB METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be  $\geq 0.2\text{mm}$  to minimize shorting.
- Lead land length should be equal to maximum part lead length + 0.2 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be  $\geq 0.17\text{mm}$  for 2 oz. Copper ( $\geq 0.1\text{mm}$  for 1 oz. Copper and  $\geq 0.23\text{mm}$  for 3 oz. Copper)
- A single 0.30mm diameter via shall be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.



## STENCIL DESIGN

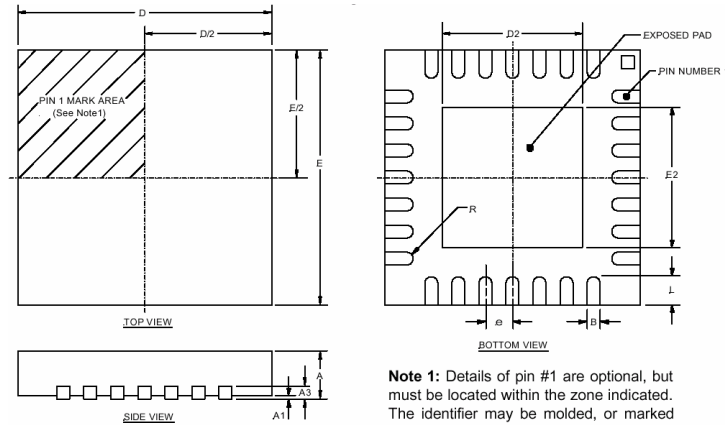
- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture  
All Dimensions in mm

## PACKAGE INFORMATION

28L MLPQ (5 x 5 mm Body) –  $\theta_{JA} = 30^{\circ}\text{C/W}$ ,  $\theta_{JC} = 3^{\circ}\text{C/W}$



| SYMBOL<br>DESIG | 28-PIN 5x5 |      |      |
|-----------------|------------|------|------|
|                 | MIN        | NOM  | MAX  |
| A               | 0.80       | 0.90 | 1.00 |
| A1              | 0.00       | 0.02 | 0.05 |
| A3              | 0.20 REF   |      |      |
| B               | 0.18       | 0.23 | 0.30 |
| D               | 5.00 BSC   |      |      |
| D2              | 3.00       | 3.15 | 3.25 |
| E               | 5.00 BSC   |      |      |
| E2              | 3.00       | 3.15 | 3.25 |
| e               | 0.50 BSC   |      |      |
| L               | 0.45       | 0.55 | 0.65 |
| R               | 0.09       | ---  | ---  |

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Consumer market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

Visit us at [www.irf.com](http://www.irf.com) for sales contact information.