



N-Channel JFET Switch

2N5432 - 2N5434

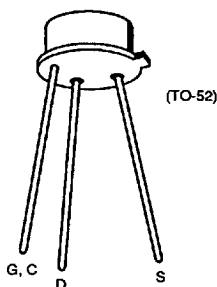
T-35-25

2N5432 - 2N5434

FEATURES

- Low $r_{ds(on)}$
- Excellent Switching
- Low Cutoff Current

PIN CONFIGURATION



5018

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source Voltage	-25V
Gate-Drain Voltage	-25V
Gate Current	100mA
Drain Current	400mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
2N5432	Hermetic TO-52	-55°C to +150°C
X2N5432	Sorted Chips in Carriers	-55°C to +150°C
2N5433	Hermetic TO-52	-55°C to +150°C
X2N5433	Sorted Chips in Carriers	-55°C to +150°C
2N5434	Hermetic TO-52	-55°C to +150°C
X2N5434	Sorted Chips in Carriers	-55°C to +150°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	2N5432		2N5433		2N5434		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
I _{gss}	Gate Reverse Current		-200		-200		-200	pA	V _{GS} = -15V, V _{DS} = 0
			-200		-200		-200	nA	T _A = 150°C
BV _{GSS}	Gate-Source Breakdown Voltage	-25		-25		-25		V	I _G = -1μA, V _{DS} = 0
I _{D(off)}	Drain Cutoff Current		200		200		200	pA	V _{DS} = 5V, V _{GS} = -10V
			200		200		200	nA	T _A = 150°C
V _{GS(off)}	Gate-Source Cutoff Voltage	-4	-10	-3	-9	-1	-4	V	V _{DS} = 5V, I _D = 3nA
I _{DSS}	Saturation Drain Current (Note 1)	150		100		30		mA	V _{DS} = 15V, V _{GS} = 0
r _{DS(on)}	Static Drain-Source ON Resistance	2	5		7		10	ohm	V _{GS} = 0, I _D = 10mA
V _{DS(on)}	Drain-Source ON Voltage		50		70		100	mV	
r _{DS(on)}	Drain-Source ON Resistance		5		7		10	ohm	V _{GS} = 0, I _D = 0 f = 1kHz
C _{iss}	Common-Source Input Capacitance (Note2)	30		30		30		pF	V _{DS} = 0, V _{GS} = -10 V f = 1MHz
C _{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	15		15		15			
t _d	Turn-ON Delay Time (Note 2)		4		4		4	ns	V _{DD} = 15V, V _{GS(on)} = 0, V _{GS(off)} = -12V, I _{D(on)} = 10mA
t _r	Rise Time (Note 2)		1		1		1		
t _{off}	Turn-OFF Delay Time (Note 2)		6		6		6		
t _f	Fall Time (Note 2)		30		30		30		

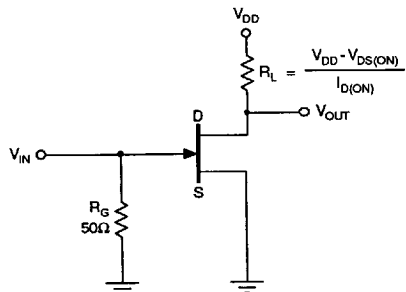
NOTES: 1. Pulse test required, pulsewidth 300μs, duty cycle ≤3%.

2. For design reference only, not 100% tested.

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calogic
 CORPORATION

T-31-25

SWITCHING TIME, TEST CIRCUIT**INPUT PULSE**

RISE TIME 0.25ns
 FALL TIME 0.75ns
 PULSE WIDTH 200ns
 PULSE RATE 550pps

SAMPLING SCOPE

RISE TIME 0.4ns
 INPUT RESISTANCE 10MΩ
 INPUT CAPACITANCE 1.5pF

0090