OBSOLETE

MICRON TECHNOLOGY, INC.

4 MEG x 1 FPM DRAM

DRAM

MT4C1004J

FEATURES

- 1,024-cycle refresh distributed across 16ms (MT4C1004J) or 128ms (MT4C1004J L only)
- Industry-standard pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR), HIDDEN; optional Extended
- FAST PAGE MODE access cycle

OPTIONS — MARKING

- Timing
  60ns access — -6
- Packages
  Plastic SOJ (300 mil) — DJ
  Plastic TSOP (300 mil) — TG
- Refresh Rate
  Standard 16ms period — None
  Extended 128ms period — L
- Part Number Example: MT4C1004JDJ-6 L

KEY TIMING PARAMETERS

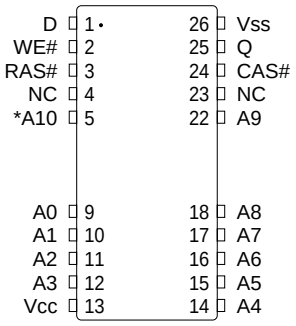
SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns

GENERAL DESCRIPTION

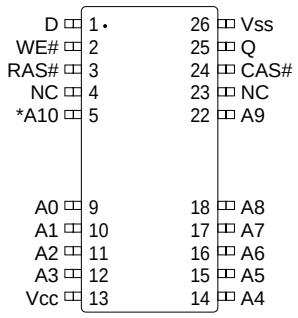
The MT4C1004J(L) is a randomly accessed, solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS# is used to latch the first 11 bits and CAS# the latter 11 bits. READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates READ mode while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. If WE# goes LOW prior to CAS# going LOW, the output pin remains open (High-Z) until the next CAS# cycle. If WE# goes LOW after data reaches the output pin, data-out (Q) is activated and retains the selected cell data as long as CAS# remains LOW (regardless of WE# or RAS#). This late WE# pulse results in a READ WRITE cycle.

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ (DA-1)



20/26-Pin TSOP (DB-1)



*Address not used for RAS#-ONLY REFRESH

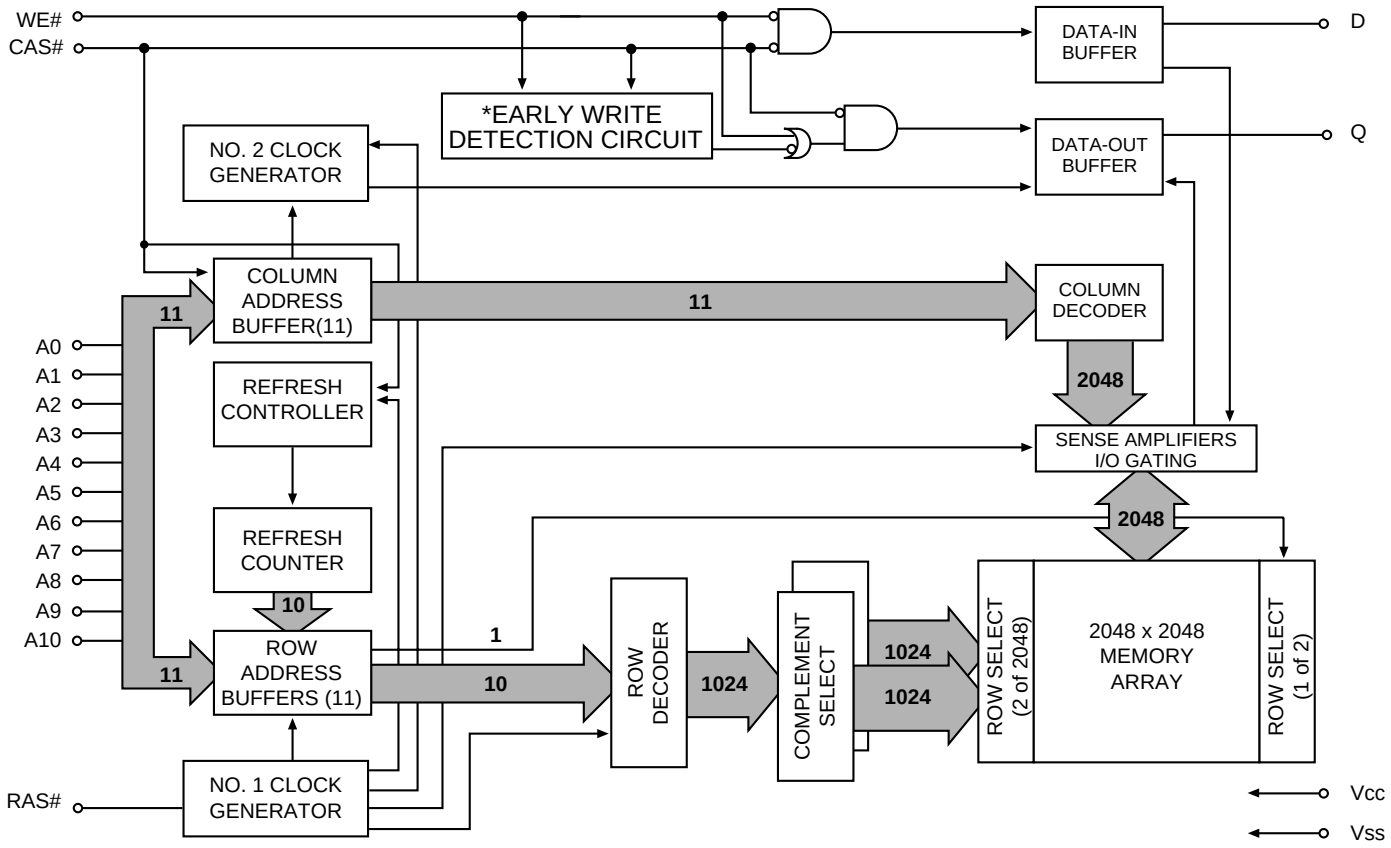
Note: The # symbol indicates signal is active LOW.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS# followed by a column address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS# ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS# addresses (A0-A9) are executed at least every 16ms for the MT4C1004J and every 128ms for the MT4C1004J L, regardless of sequence. The CBR and extended refresh cycles will invoke the internal refresh counter for automatic RAS# addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If WE# goes LOW prior to CAS# going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If CAS# goes LOW prior to WE# going LOW, EW detection circuit output is a LOW (LATE WRITE).

TRUTH TABLE

FUNCTION		RAS#	CAS#	WE#	ADDRESSES		DATA	
					^{t}R	^{t}C	D (Data-In)	Q (Data-Out)
Standby		H	H→X	X	X	X	“don’t care”	High-Z
READ		L	L	H	ROW	COL	“don’t care”	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In	High-Z
READ WRITE		L	L	H→L	ROW	COL	Data-In	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	“don’t care”	Data-Out
READ	2nd Cycle	L	H→L	H	n/a	COL	“don’t care”	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data-In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data-In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data-In	Data-Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data-In	Data-Out
RAS#-ONLY REFRESH		L	H	X	ROW	n/a	“don’t care”	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	“don’t care”	Data-Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data-In	High-Z
CBR REFRESH		H→L	L	H	X	X	“don’t care”	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic)..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 3, 5, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC} +1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC} +1V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (DQ is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS# = CAS# = V_{IH})	I_{CC1}	2	mA	
STANDBY CURRENT: (CMOS) (RAS# = CAS# = V_{CC} -0.2V)	I_{CC2}	1	mA	
	I_{CC2} (L only)	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, single address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	110	mA	3, 23
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^tPC = ^tPC [MIN])	I_{CC4}	80	mA	3, 23
REFRESH CURRENT: RAS# ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	110	mA	3, 23
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC6}	110	mA	3, 4
REFRESH CURRENT: Extended (L version only) Average power supply current during Extended Refresh: CAS# = 0.2V or CBR cycling; RAS# = ^tRAS (MIN); WE# = V_{CC} -0.2V; A0-A10 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7} (L only)	300	µA	3, 4, 6, 21

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	C_{I1}	5	pF	2
Input Capacitance: RAS#, CAS#, WE#	C_{I2}	7	pF	2
Output Capacitance: DQ	C_O	7	pF	2

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6			
PARAMETER	SYM	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	45		ns	
Column-address setup time	^tASC	0		ns	
Row-address setup time	^tASR	0		ns	
Column-address to WE# delay time	^tAWD	30		ns	18
Access time from CAS#	^tCAC		15	ns	
Column-address hold time	^tCAH	10		ns	
CAS# pulse width	^tCAS	15	10,000	ns	
CAS# hold time (CBR REFRESH)	^tCHR	10		ns	4
CAS# to output in Low-Z	^tCLZ	0		ns	
CAS# precharge time	^tCP	10		ns	13
Access time from CAS# precharge	^tCPA		35	ns	
CAS# to RAS# precharge time	^tCRP	10		ns	
CAS# hold time	^tCSH	60		ns	
CAS# setup time (CBR REFRESH)	^tCSR	10		ns	4
CAS# to WE# delay time	^tCWD	15		ns	18
Write command to CAS# lead time	^tCWL	15		ns	
Data-in hold time	^tDH	10		ns	19
Data-in setup time	^tDS	0		ns	19
Output buffer turn-off delay	^tOFF	3	15	ns	17, 23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	60		ns	
Access time from RAS#	^tRAC		60	ns	
RAS# to column-address delay time	^tRAD	15		ns	15
Row-address hold time	^tRAH	10		ns	
RAS# pulse width	^tRAS	60	10,000	ns	21
RAS# pulse width (FAST PAGE MODE)	^tRASP	60	100,000	ns	21
Random READ or WRITE cycle time	^tRC	110		ns	
RAS# to CAS# delay time	^tRCD	20		ns	14
Read command hold time (referenced to CAS#)	^tRCH	0		ns	16
Read command setup time	^tRCS	0		ns	
Refresh period (1,024 cycles)	^tREF		16	ms	
Refresh period (1,024 cycles) L version	^tREF		128	ms	
RAS# precharge time	^tRP	40		ns	
RAS# to CAS# precharge time	^tRPC	0		ns	

AC ELECTRICAL CHARACTERISTICS

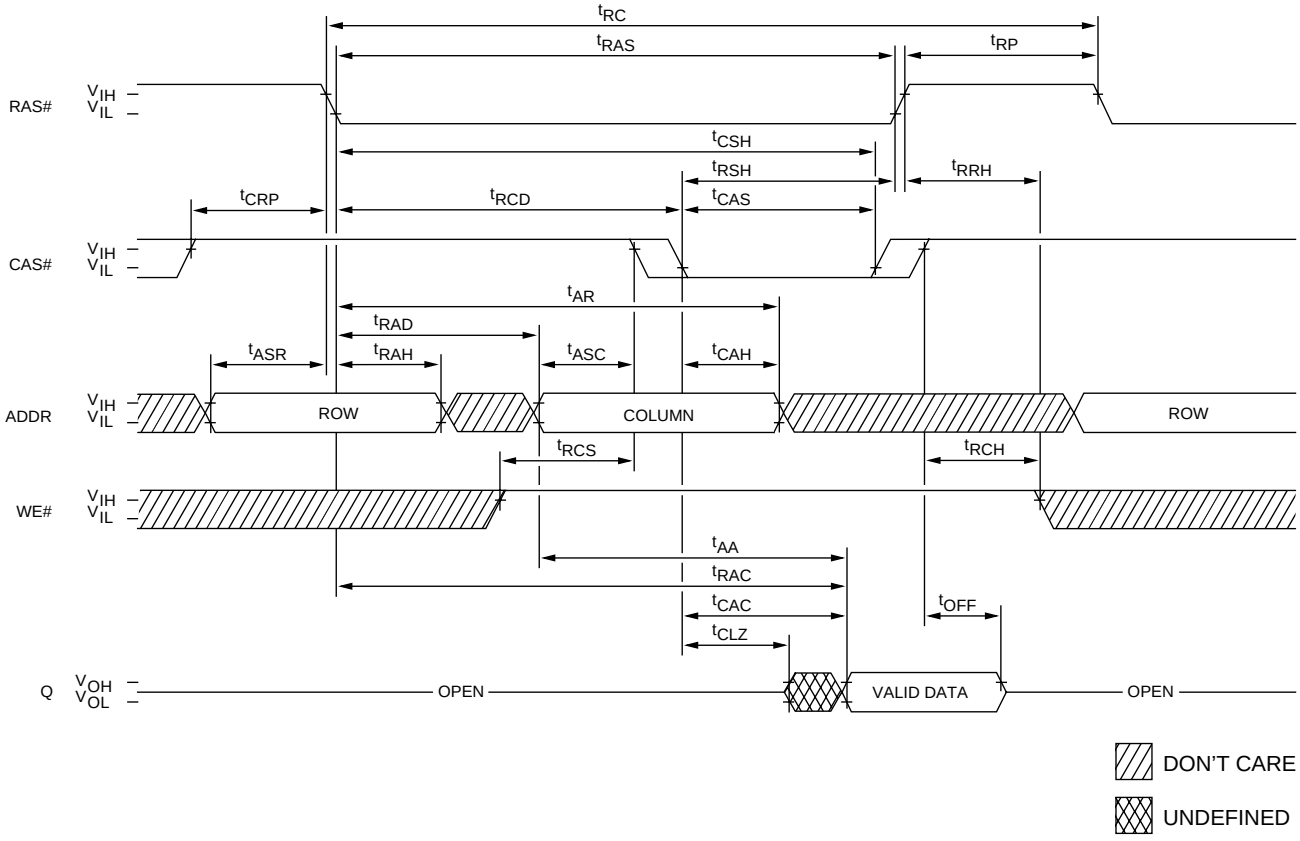
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read command hold time (referenced to RAS#)	^{t}RRH	0		ns	16
RAS# hold time	^{t}RSH	15		ns	
READ WRITE cycle time	^{t}RWC	130		ns	
RAS# to WE# delay time	^{t}RWD	60		ns	18
Write command to RAS# lead time	^{t}RWL	15		ns	
Transition time (rise or fall)	^{t}T	2	50	ns	
Write command hold time	^{t}WCH	10		ns	
Write command hold time (referenced to RAS#)	^{t}WCR	45		ns	
WE# command setup time	^{t}WCS	0		ns	18
Write command pulse width	^{t}WP	10		ns	
WE# hold time (CBR REFRESH)	^{t}WRH	10		ns	
WE# setup time (CBR REFRESH)	^{t}WRP	10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 4.5V; f = 1 MHz.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS# ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
14. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD limit, ^{t}AA and ^{t}CAC must always be met.
15. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
16. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
17. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
18. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE, READ WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit through-out the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE WRITE and the state of data-out is indeterminate (at access time and until CAS# goes back to V_{IH}).
19. These parameters are referenced to CAS# leading edge in early WRITE cycles and WE# leading edge in late WRITE or READ WRITE cycles.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW.
21. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.
22. The 3ns minimum is a parameter guaranteed by design.
23. Column address changed once each cycle.

READ CYCLE

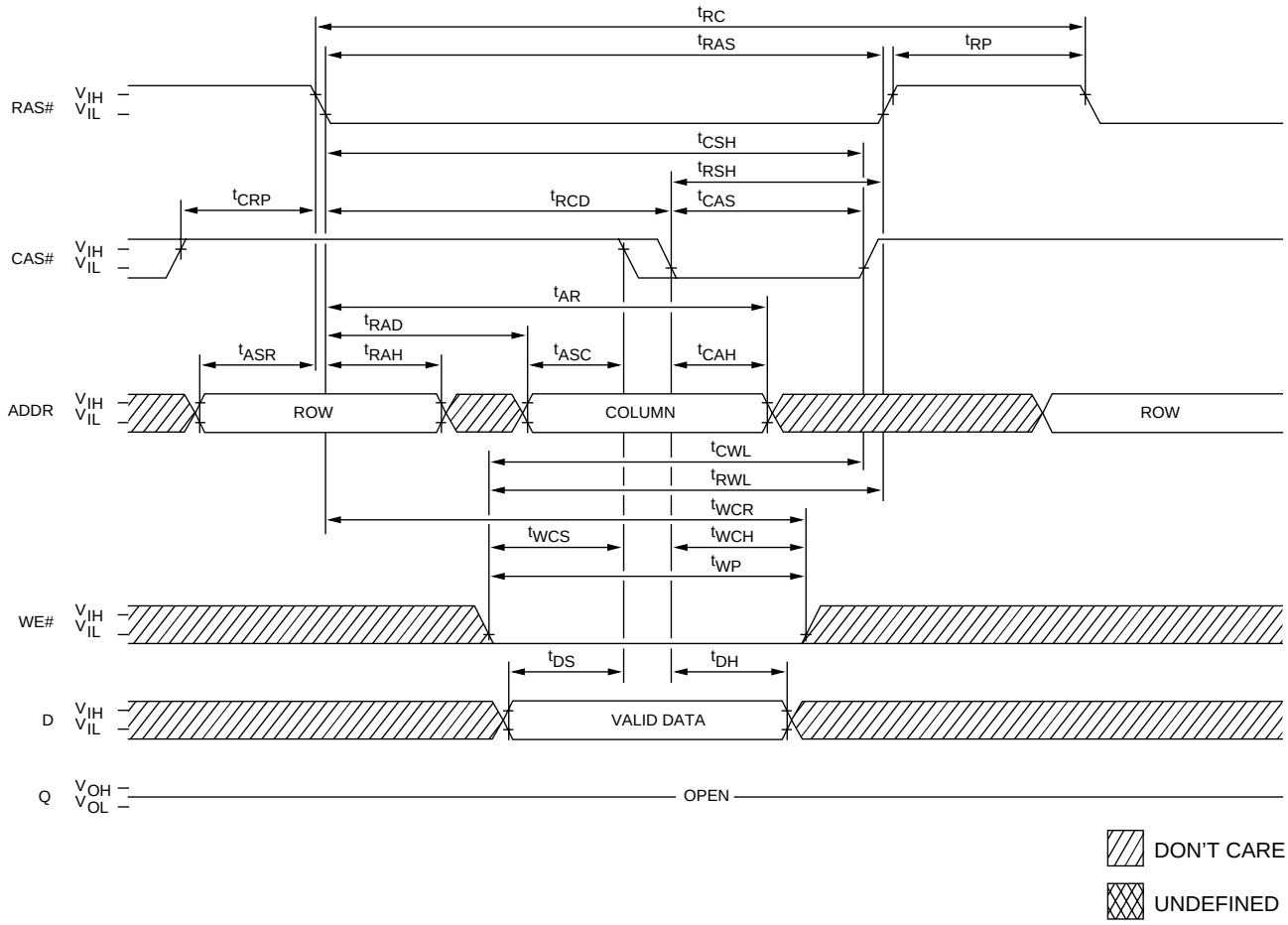


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	0		ns
tCRP	10		ns
tCSH	60		ns
tOFF	3	15	ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRC	110		ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

EARLY WRITE CYCLE

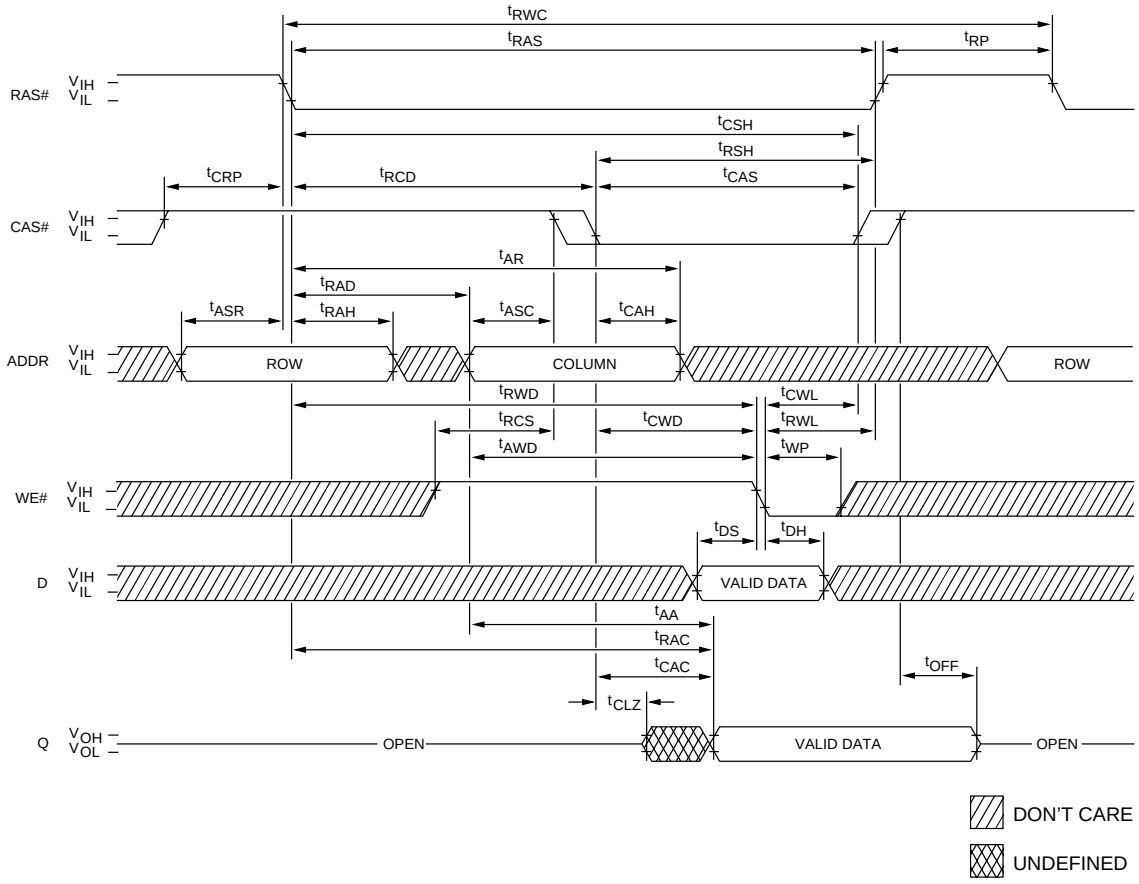


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAH	10		ns
tCAS	15	10,000	ns
tCRP	10		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns
tRAD	15		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAH	10		ns
tRAS	60	10,000	ns
tRC	110		ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCR	45		ns
tWCS	0		ns
tWP	10		ns

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

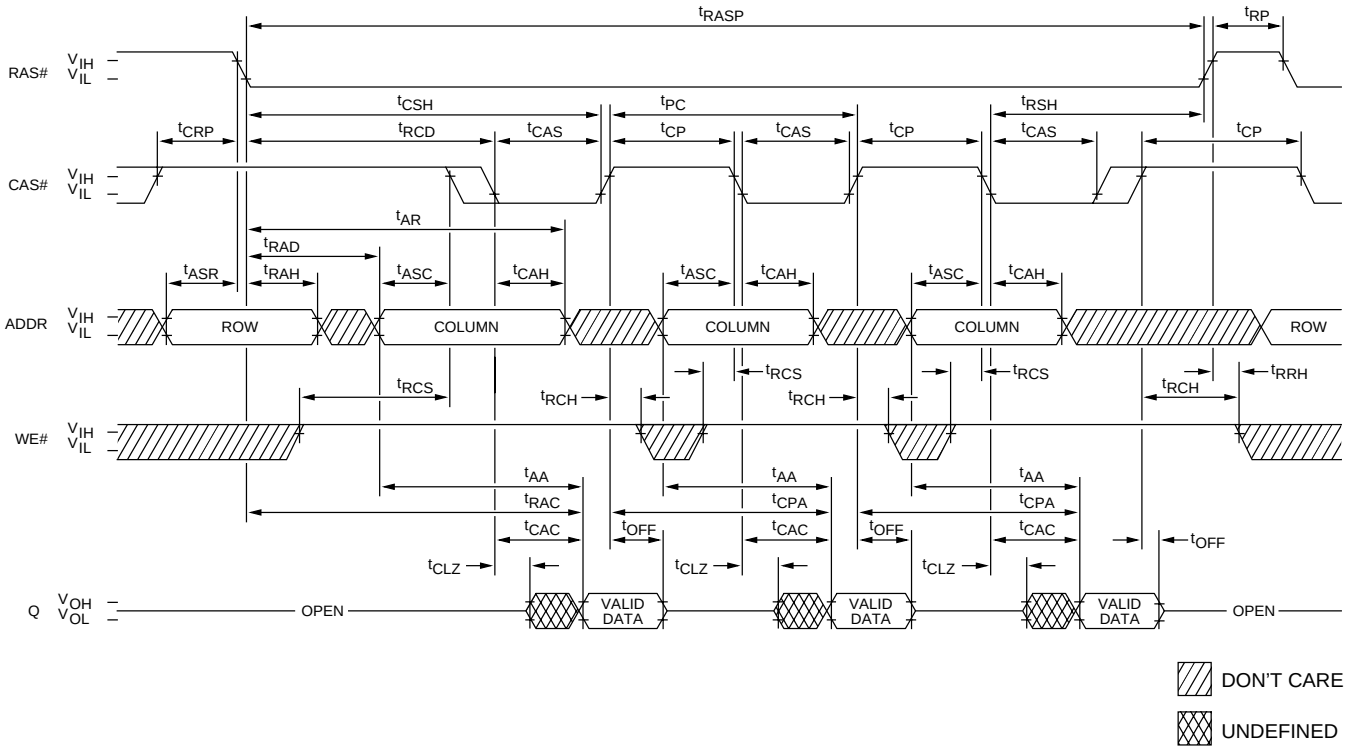


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tAWD	30		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	0		ns
tCRP	10		ns
tCSH	60		ns
tCWD	15		ns
tCWL	15		ns
tDH	10		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tDS	0		ns
tOFF	3	15	ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWC	130		ns
tRWD	60		ns
tRWL	15		ns
tWP	10		ns

FAST-PAGE-MODE READ CYCLE

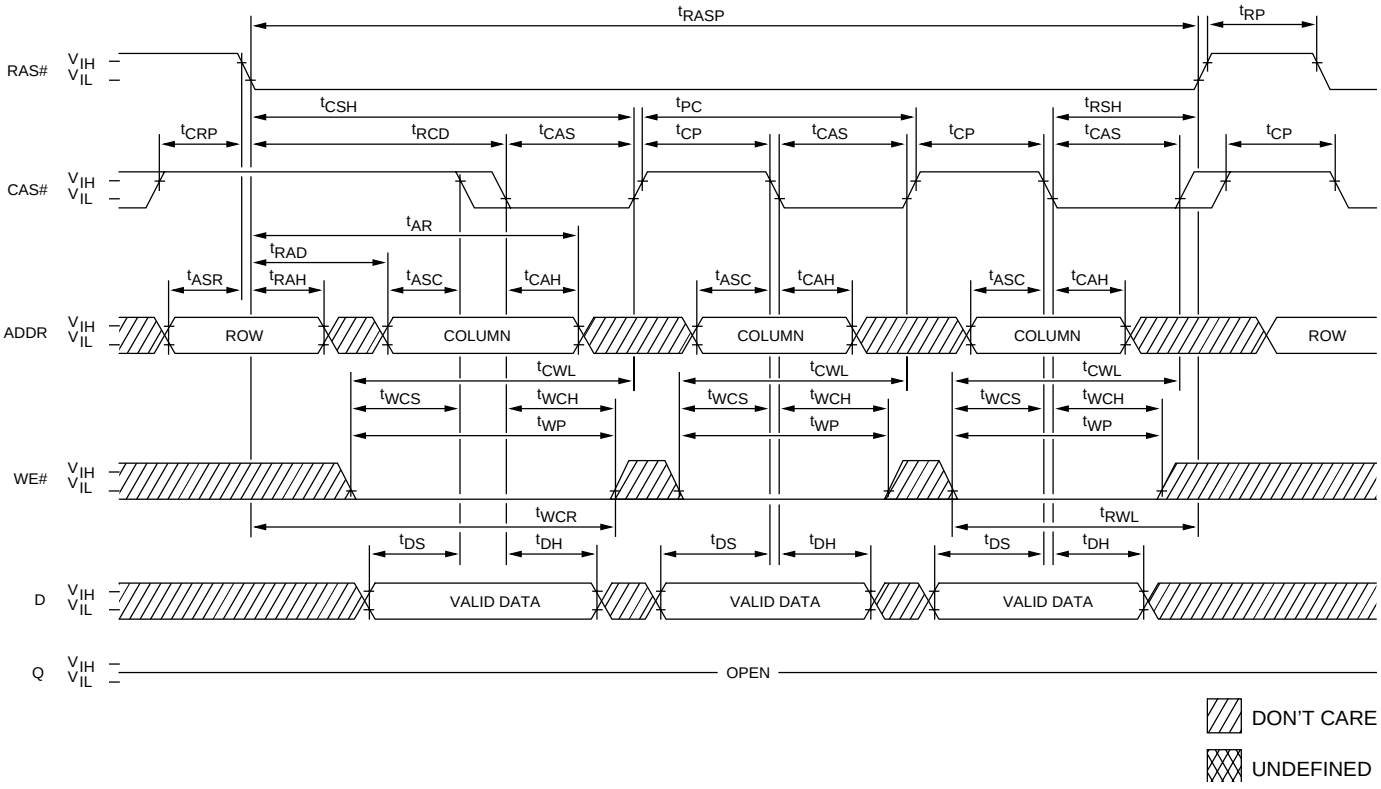


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	0		ns
tCP	10		ns
tCPA		35	ns
tCRP	10		ns
tCSH	60		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

FAST-PAGE-MODE EARLY-WRITE CYCLE

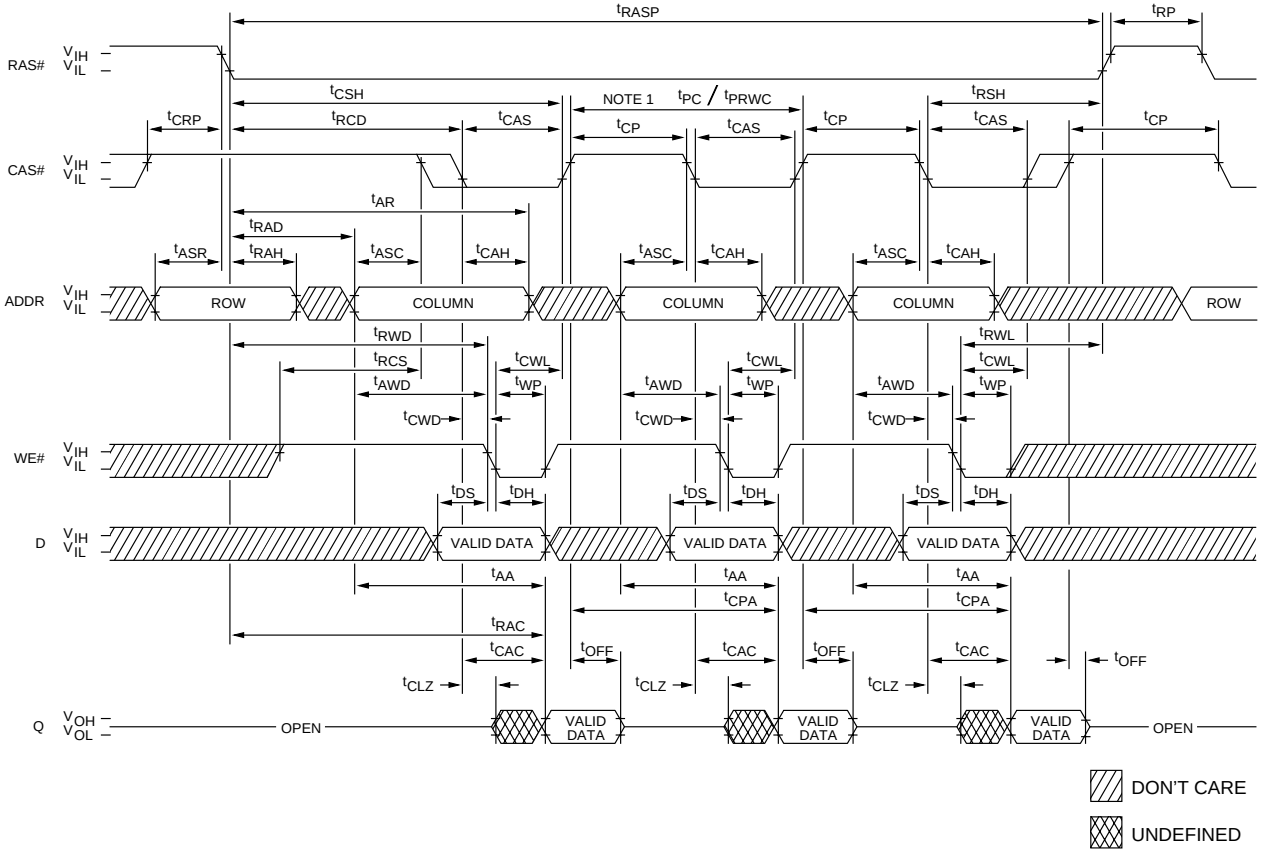


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAH	10		ns
tCAS	15	10,000	ns
tCP	10		ns
tCRP	10		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns
tPC	35		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCR	45		ns
tWCS	0		ns
tWP	10		ns

FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



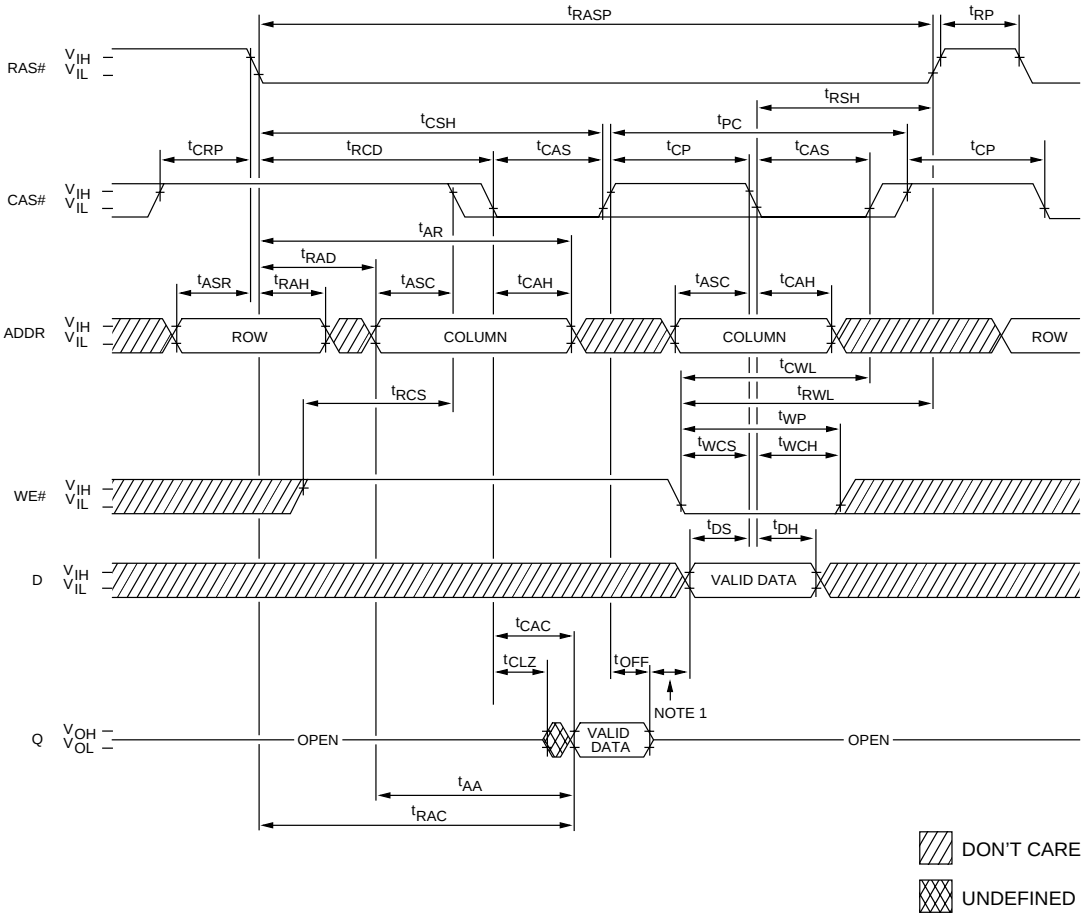
TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tAWD	30		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	0		ns
tCP	10		ns
tCPA		35	ns
tCRP	10		ns
tCSH	60		ns
tCWD	15		ns
tCWL	15		ns
tDH	10		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tDS	0		ns
tOFF	3	15	ns
tPC	35		ns
tPRWC	60		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWD	60		ns
tRWL	15		ns
tWP	10		ns

NOTE: 1. tPC is for LATE WRITE only.

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE



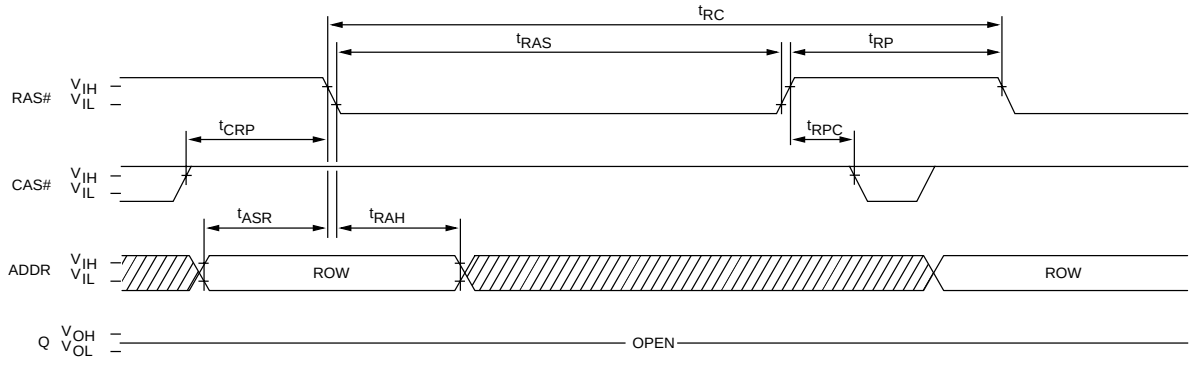
TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	0		ns
tCP	10		ns
tCRP	10		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns

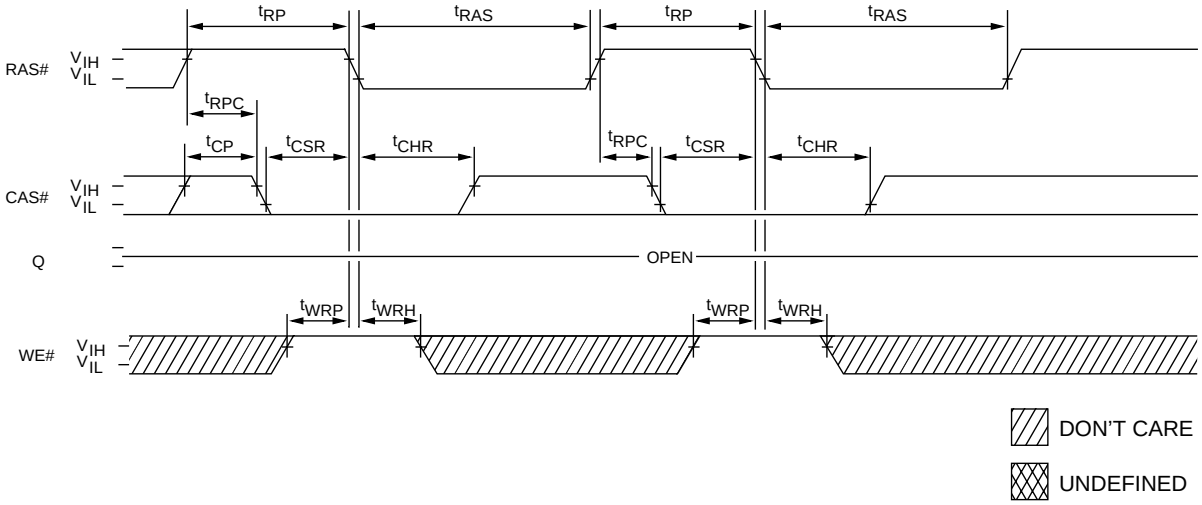
SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCS	0		ns
tWP	10		ns

NOTE: 1. Do not drive data prior to tristate.
2. Assumes D and Q are tied together.

RAS#-ONLY REFRESH CYCLE
(WE# and A10 = DON'T CARE)



CBR REFRESH CYCLE
(Addresses = DON'T CARE)

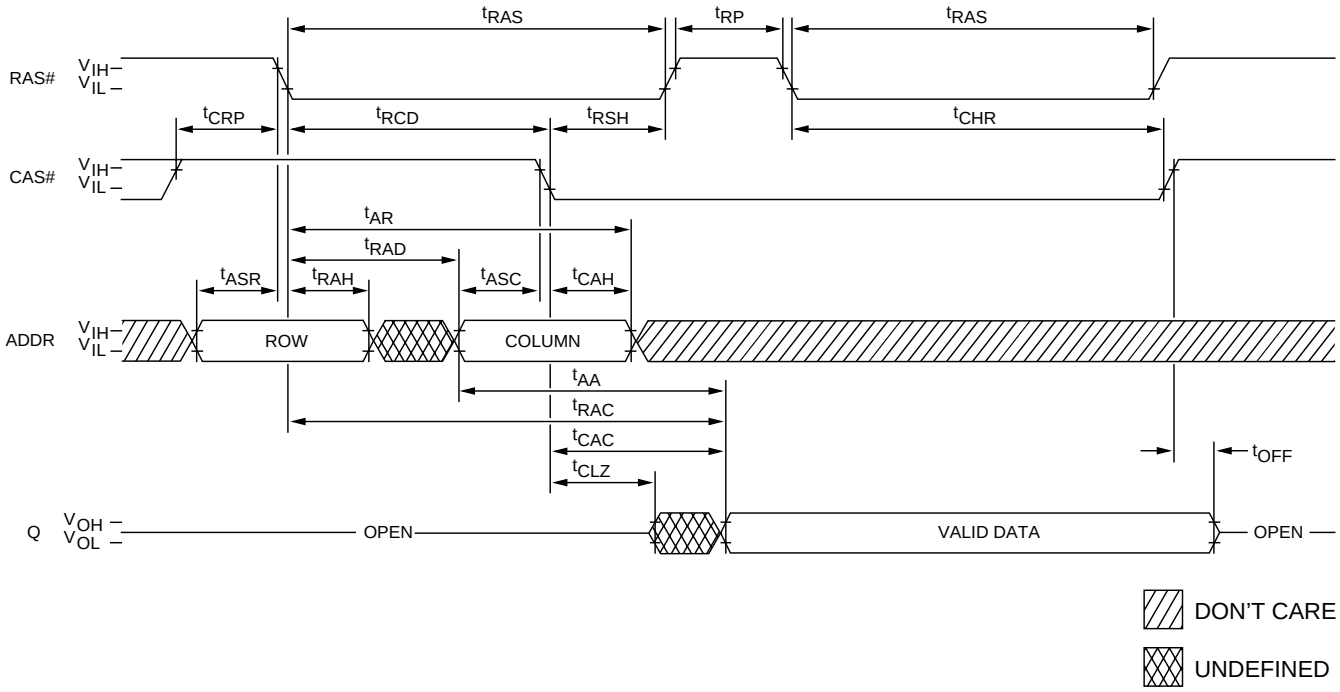


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tASR	0		ns
tCHR	10		ns
tCP	10		ns
tCRP	10		ns
tCSR	10		ns
tRAH	10		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAS	60	10,000	ns
tRC	110		ns
tRP	40		ns
tRPC	0		ns
tWRH	10		ns
tWRP	10		ns

HIDDEN REFRESH CYCLE [20]
(WE# = HIGH)

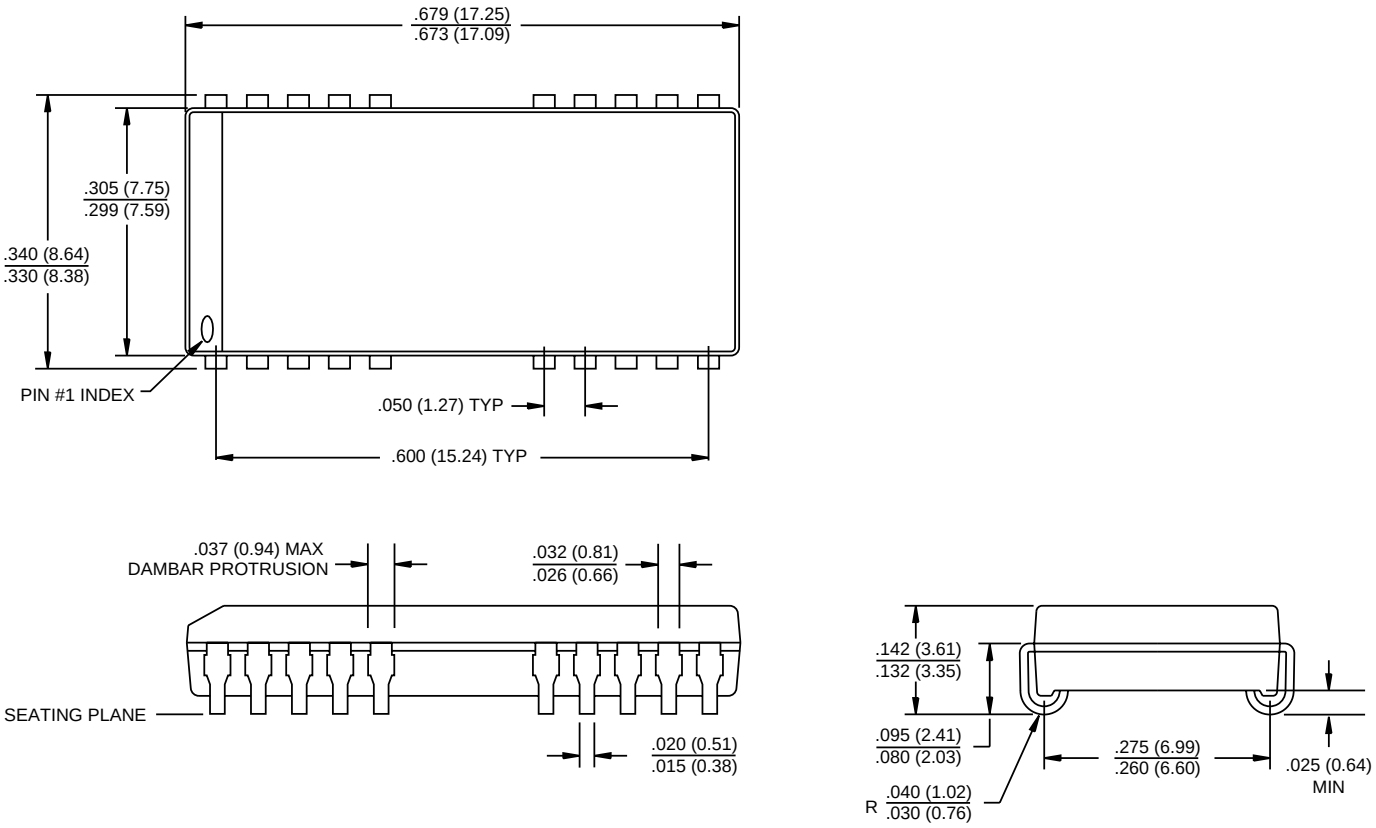


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCHR	10		ns
tCLZ	0		ns
tCRP	10		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns

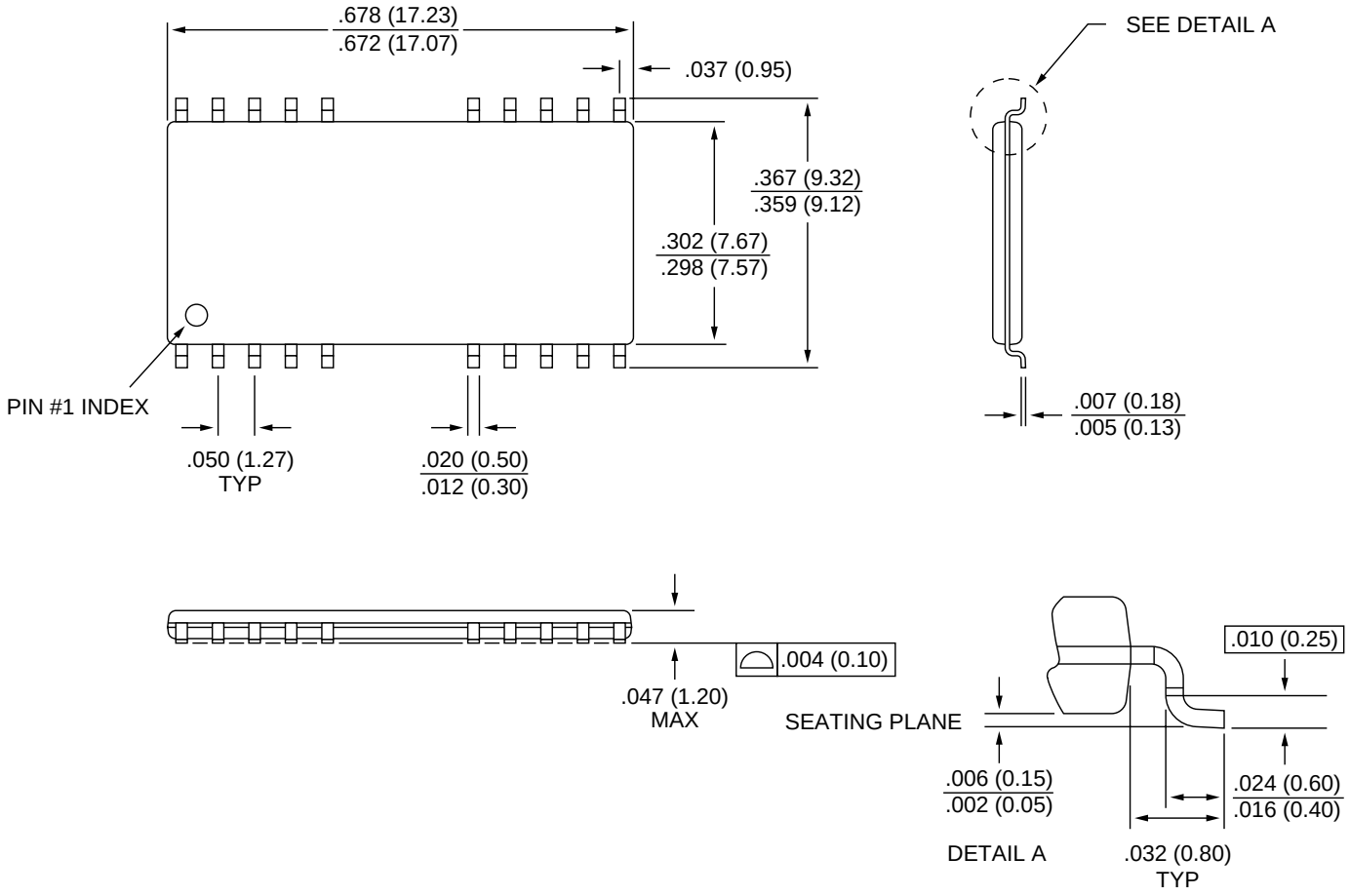
20/26-PIN PLASTIC SOJ (300 mil)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

20/26-PIN PLASTIC TSOP (300 mil)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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