Si4720/21-B20

BROADCAST FM RADIO TRANSCEIVER FOR PORTABLE APPLICATIONS

Features

- Full FM RX and TX in 3 x 3 QFN
- Worldwide FM RX band support
- Compliant with worldwide FM TX regulations
- Excellent real-world performance
- Supports integrated TX/RX antenna
- Programmable transmit output voltage
- Frequency synthesizer with integrated VCO
- Integrated LDO regulator
- Minimal BOM (15 mm^2)
- Digital audio output (Si4721 only)
- Digital audio input
- Adjustable seek parameters
- Adjustable mono/stereo blend
- Adjustable soft mute
- Advanced modulation control
- Audio dynamic range control
- Audio silence detector
- Programmable reference clock input
- 2-wire and 3-wire control interface
- 2.7 to 5.5 V supply voltage
- 3 x 3 x 0.55 mm 20-pin Pb-free QFN package
- RDS/RDBS encoder/decoder (Si4721 only)

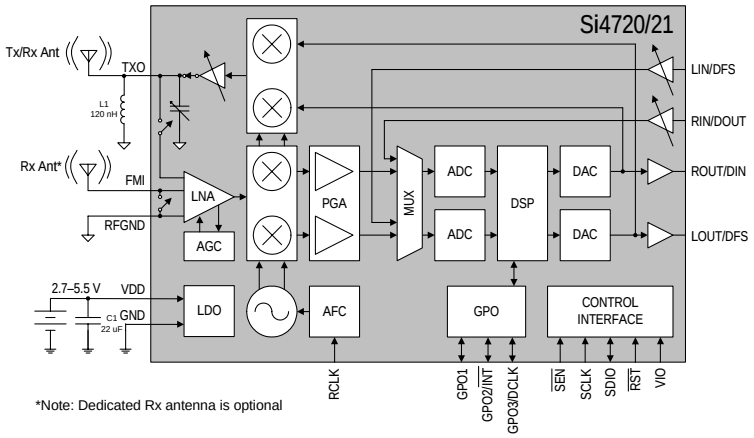
Applications

- Cellular handsets/hands-free
- MP3 players
- Portable media players
- Wireless speakers/microphone
- Satellite digital audio radios
- Personal computers/notebooks

Description

The Si4720/21 integrates the complete tuner and transmit functions for FM broadcast reception and standards-compliant, unlicensed FM broadcast stereo transmission. Users must comply with local radio frequency (RF) transmission regulations.

Functional Block Diagram



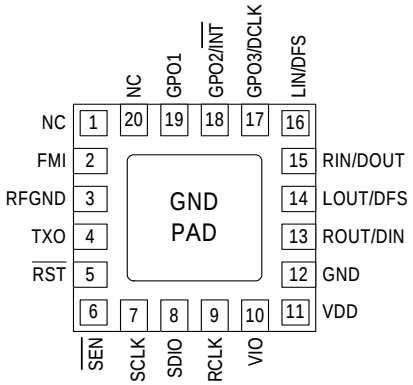
*Note: Dedicated Rx antenna is optional

Ordering Information:

See page 42.

Pin Assignments

Si4720/21
(Top View)



Patents pending

Notes:

1. To ensure proper operation and FM transceiver performance, follow the guidelines in "AN383: 3 mm x 3 mm QFN Universal Layout Guide." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. Place the Si4720/21 as close as possible to the antenna jack, and keep the FMI trace as short as possible.

TABLE OF CONTENTS

Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.7	—	5.5	V
Interface Supply Voltage	V_{IO}		1.5	—	3.6	V
Power Supply Power-Up Rise Time	V_{DDRISE}		10	—	—	µs
Interface Power Supply Power-Up Rise Time	V_{IORISE}		10	—	—	µs
Ambient Temperature	T_A		–20	25	85	°C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{IO} + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{PK}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4720/21 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, GPO1, GPO2/$\overline{\text{INT}}$, and GPO3.
4. At RF input pin FMI.

Table 3. DC Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Receiver						
RX Supply Current	I_{RX}		—	19.2	22	mA
RX Supply Current[1]	I_{RX}	Low SNR level	—	19.8	23	mA
RX Interface Supply Current	I_{IORX}		—	320	600	µA
RX RDS Supply Current[2]	I_{FM}	Analog Output Mode	—	19.9	23	mA
RX Supply Current[2]	I_{FMD}	Digital Output Mode	—	18.0	20.5	mA
FM Transmitter						
TX Supply Current	I_{TX}		—	18.8	22.8	mA
TX Interface Supply Current	I_{IOTX}		—	320	600	µA
FM Transmitter from Digital Audio Input						
TX Supply Current	I_{DTX}	DCLK = 3.072 MHz	—	18.3	—	mA
TX Interface Supply Current	I_{DIO}	DCLK = 3.072 MHz	—	320	—	µA
FM Transmitter in Receive Power Scan Mode						
RX Supply Current	I_{RX}		—	16.8	—	mA
RX Interface Supply Current	I_{IORPS}		—	400	—	µA
Supplies and Interface						
V_{DD} Powerdown Current	I_{DDPD}	Powerdown mode	—	10	20	µA
V_{IO} Powerdown Current	I_{IOPD}	SCLK, RCLK inactive Powerdown mode	—	3	10	µA
High Level Input Voltage[3]	V_{IH}		0.7 x V_{IO}	—	VIO + 0.3	V
Low Level Input Voltage[3]	V_{IL}		–0.3	—	0.3 x V_{IO}	V
High Level Input Current[3]	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
Low Level Input Current[3]	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
High Level Output Voltage[4]	V_{OH}	I_{OUT} = 500 µA	0.8 x VIO	—	—	V
Low Level Output Voltage[4]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{IO}	V

Notes:
1. LNA is automatically switched to higher current mode for optimum sensitivity in weak signal conditions.
2. Guaranteed by characterization.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, GPO1, GPO2/$\overline{\text{INT}}$, and GPO3.
4. For output pins SDIO, GPO1, GPO2/$\overline{\text{INT}}$, and GPO3.

Table 4. Reset Timing Characteristics[1,2,3]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width and GPO1, GPO2/$\overline{INT}$ Setup to $\overline{RST}\uparrow$[4]	t_{SRST}	100	—	—	µs
GPO1, GPO2/$\overline{INT}$ Hold from $\overline{RST}\uparrow$	t_{HRST}	30	—	—	ns

Important Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the 1st start condition.
3. When selecting 3-wire or SPI modes, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.
4. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is hi-Z, then minimum t_{SRST} is 100 µs, to provide time for on-chip 1 MΩ devices (active while $\overline{RST}$ is low) to pull GPO1 high and GPO2 low.

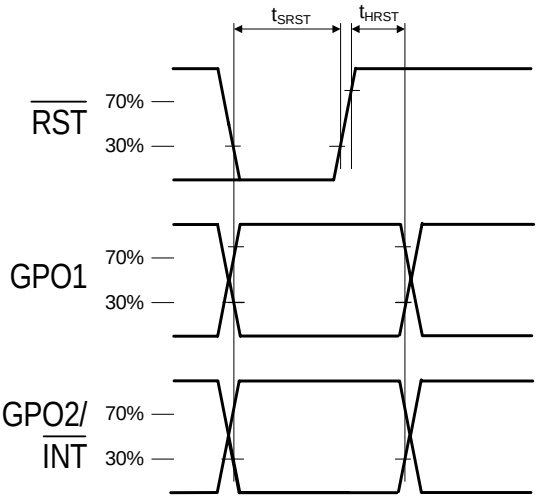


Figure 1. Reset Timing Parameters for Busmode Select

Table 5. 2-Wire Control Interface Characteristics[1,2,3]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK↓ Hold[4,5]	$t_{HD:DAT}$		0	—	900	ns
SCLK input to SDIO↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		$20 + 0.1\frac{C_b}{1\ pF}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		$20 + 0.1\frac{C_b}{1\ pF}$	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:

1. When V_{IO} = 0 V, SCLK and SDIO are low-impedance. 2-wire control interface is I^2C compatible.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
4. The Si4720/21 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum $t_{HD:DAT}$ specification.
5. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 KHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

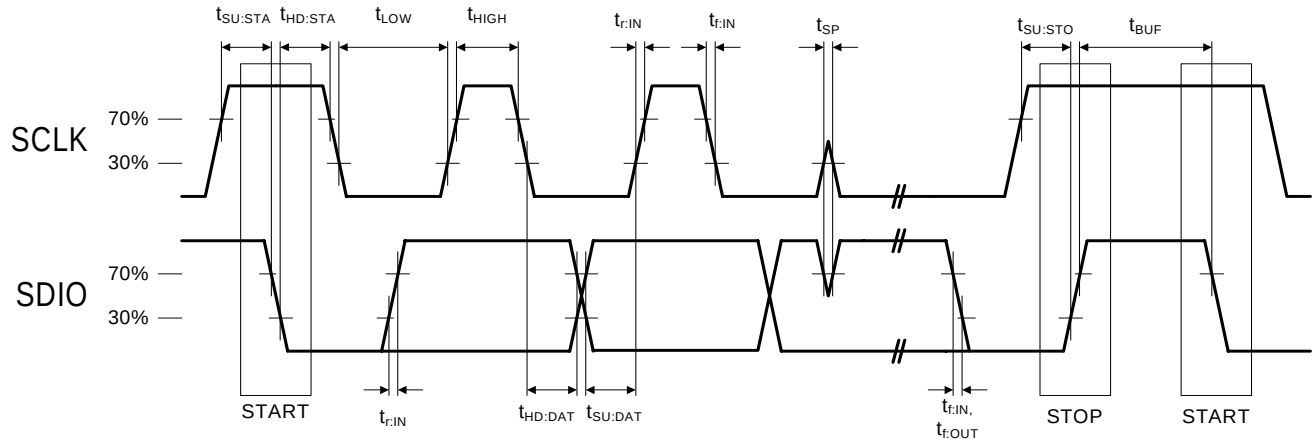


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

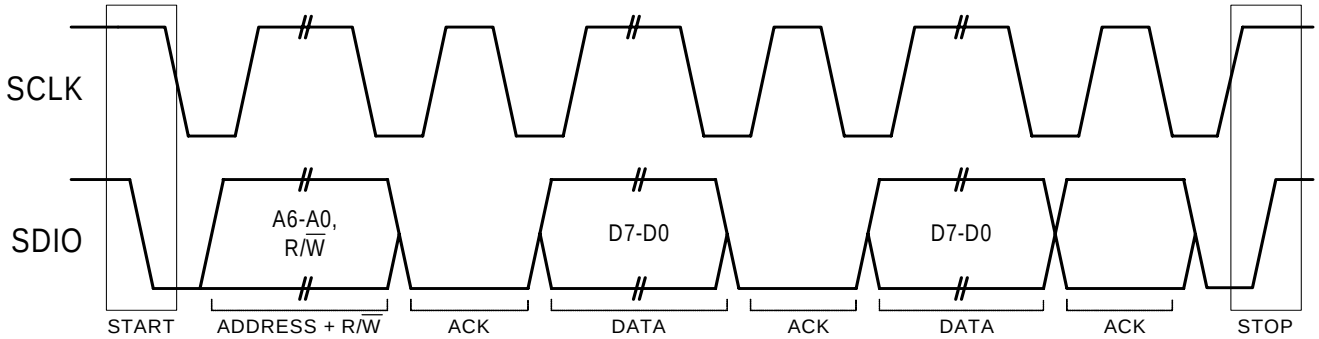


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 6. 3-Wire Control Interface Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		10	—	—	ns
SCLK↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R, t_F		—	—	10	ns

Note: When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

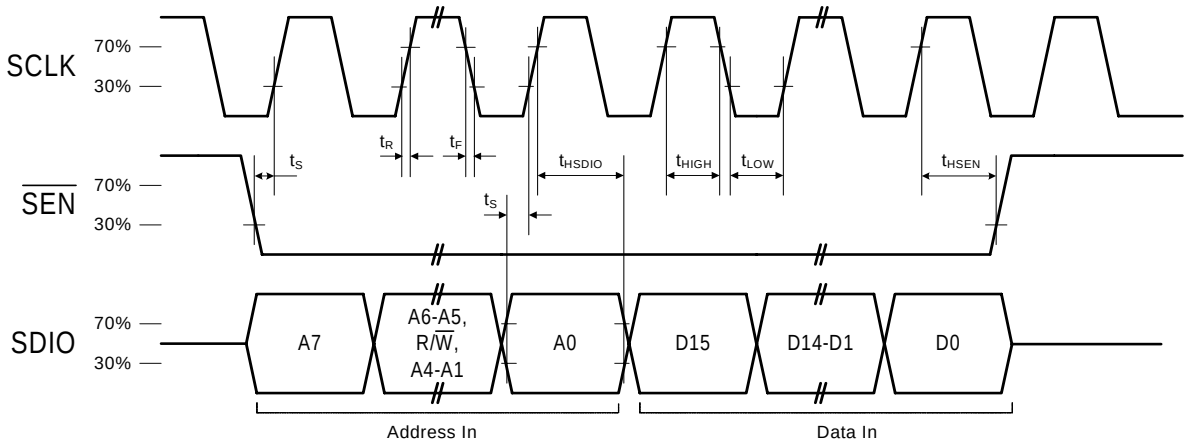


Figure 4. 3-Wire Control Interface Write Timing Parameters

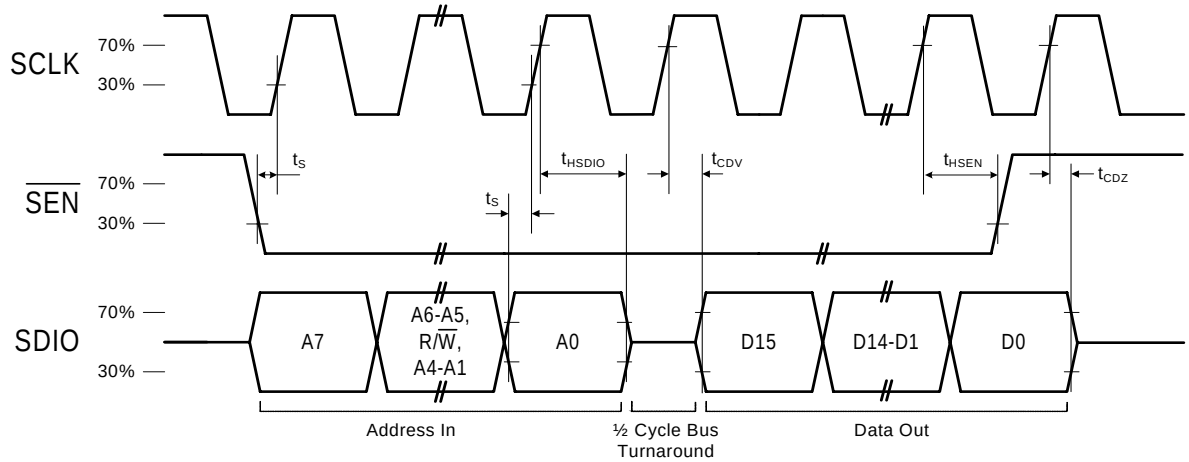


Figure 5. 3-Wire Control Interface Read Timing Parameters

Table 7. SPI Control Interface Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		15	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		5	—	—	ns
SCLK↓ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↓ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R, t_F		—	—	10	ns

Note: When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

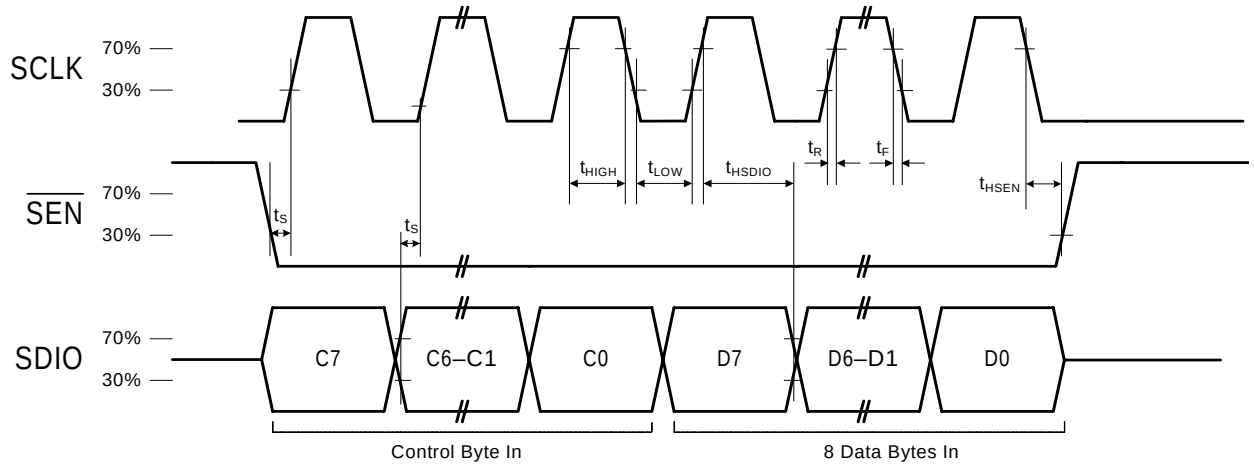


Figure 6. SPI Control Interface Write Timing Parameters

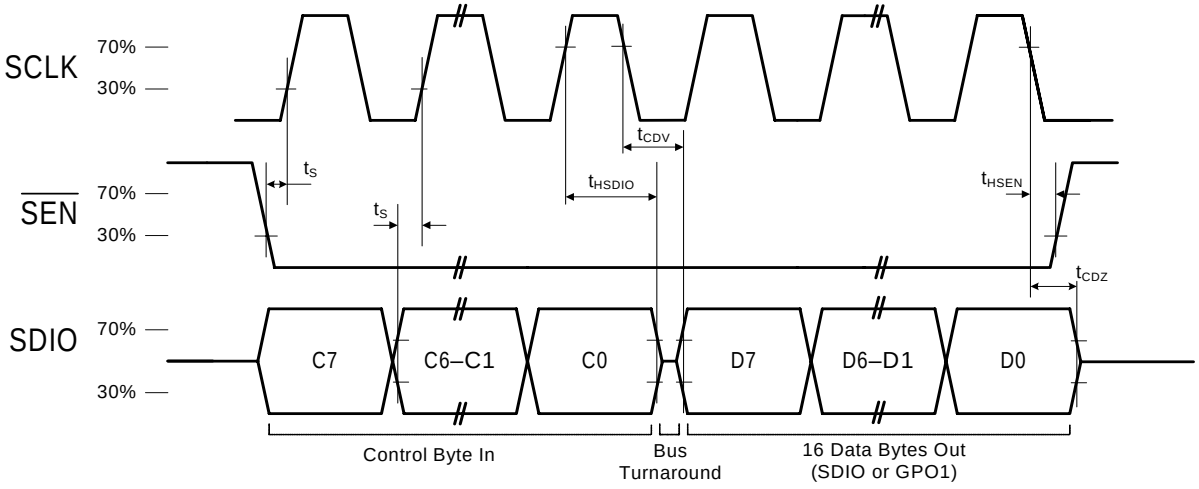


Figure 7. SPI Control Interface Read Timing Parameters

Table 8. Digital Audio Interface Characteristics (Receive)
(V_{DD} = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	1000	ns
DCLK pulse width high	t_{DCH}		10	—	—	ns
DCLK pulse width low	t_{DCL}		10	—	—	ns
DFS set-up time to DCLK rising edge	$t_{SU:DFS}$		5	—	—	ns
DFS hold time from DCLK rising edge	$t_{HD:DFS}$		5	—	—	ns
DOUT propagation delay from DCLK falling edge	$t_{PD:DOUT}$		0	—	12	ns

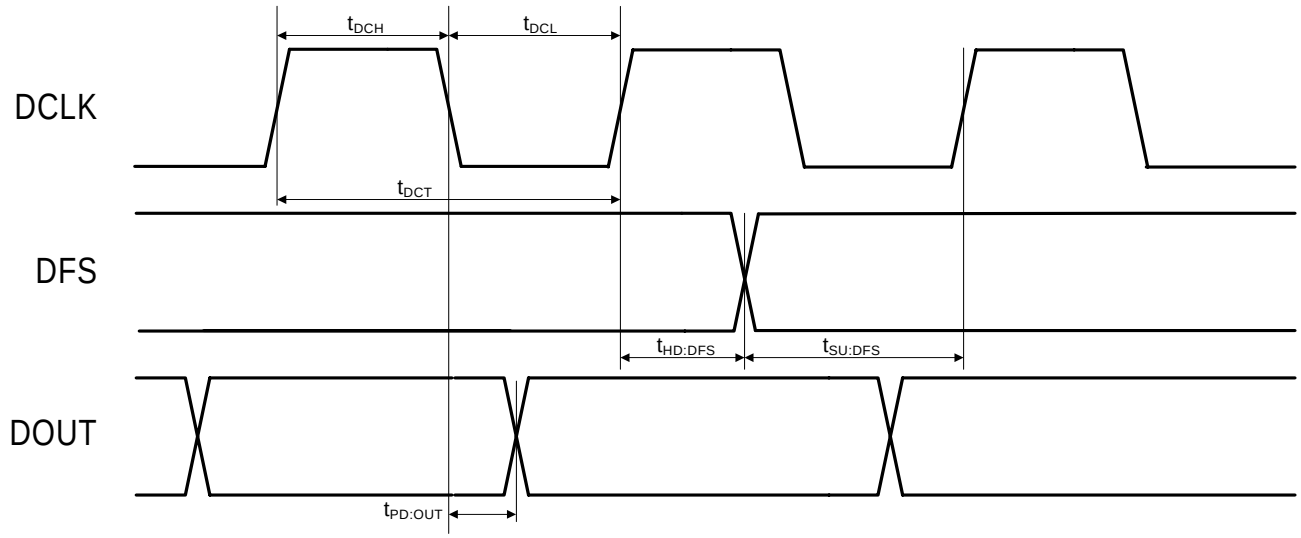


Figure 8. Digital Audio Interface Timing Parameters, I^2S Mode

Table 9. FM Receiver Characteristics[1,2]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		76	—	108	MHz
Sensitivity with Headphone Network[3,4,5]		(S+N)/N = 26 dB	—	2.2	3.5	µV EMF
Sensitivity with 50 Ω Network[3,4,5,6]		(S+N)/N = 26 dB	—	1.1	—	µV EMF
RDS Sensitivity[6]		Δf = 2 kHz, RDS BLER < 5%	—	15	—	µV EMF
TXO Receiver Mode Sensitivity[6]			—	3.5	—	µV EMF
LNA Input Resistance[6,7]			3	4	5	kΩ
LNA Input Capacitance[6,7]			4	5	6	pF
Input IP3[6,8]			100	105	—	dBµV EMF
AM Suppression[3,4,6,7]		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection[6]		In-band	35	—	—	dB
Audio Output Voltage[3,4,7]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[3,7,9]			—	—	1	dB
Audio Frequency Response Low[6]		–3 dB	—	—	30	Hz
Audio Frequency Response High[6]		–3 dB	15	—	—	kHz
Audio Stereo Separation[7,9]			25	—	—	dB
Audio Mono S/N[3,4,5,7,10]			55	63	—	dB
Audio Stereo S/N[4,5,7,10,11]			—	58	—	dB
Audio THD[3,7,9]			—	0.1	0.5	%
De-emphasis Time Constant[6]		FM_DEEMPHASIS = 2	70	75	80	µs
		FM_DEEMPHASIS = 1	45	50	54	µs
Audio Output Load Resistance[6,10]	R_L	Single-ended	10	—	—	kΩ

Notes:

1. Additional testing information is available in Application Note AN388. Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Antenna Selection and Universal Layout Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. V_{EMF} = 1 mV.
8. $|f_2 – f_1| > 2$ MHz, $f_0 = 2 \times f_1 – f_2$. AGC is disabled. Refer to "7. Pin Descriptions: Si4720/21-GM" on page 41.
9. Δf = 75 kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. At temperature 25 °C.

Table 9. FM Receiver Characteristics[1,2] (Continued)

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Audio Output Load Capacitance[6,10]	C_L	Single-ended	—	—	50	pF
Seek/Tune Time[6]		RCLK tolerance = 100 ppm	—	—	80	ms/channel
Powerup Time[6]		From powerdown	—	—	110	ms
RSSI Offset[12]		Input levels of 8 and 60 dBµV at RF Input	–3	—	3	dB

Notes:

1. Additional testing information is available in Application Note AN388. Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Antenna Selection and Universal Layout Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. V_{EMF} = 1 mV.
8. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled. Refer to "7. Pin Descriptions: Si4720/21-GM" on page 41.
9. Δf = 75 kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. At temperature 25 °C.

Table 10. FM Transmitter Characteristics[1]

Test conditions: V_{RF} = 118 dBµV, stereo, Δf = 68.25 kHz, Δfpilot = 6.75 kHz, REFCLK = 32.768 kHz, 75 µs pre-emphasis, unless otherwise specified.
Production test conditions: V_{DD} = 3.3 V, V_{IO} = 3.3 V, T_A = 25 °C, F_{RF} = 98 MHz.
Characterization test conditions: V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C, F_{RF} = 76–108 MHz.
All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions.
Typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
Parameters are tested in production unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Frequency Range[2]	f_{RF}		76	—	108	MHz
Transmit Frequency Accuracy and Stability[2,3]			–3.5	—	3.5	kHz
Transmit Voltage Accuracy[2]		V_{RF} = 103–117 dBµV	–2.5	—	2.5	dB
Transmit Voltage Accuracy		V_{RF} = 102, 118 dBµV	–2.5	—	2.5	dB
Transmit Voltage Temperature Coefficient[2]			–0.075	—	–0.025	dB/°C
Transmit Channel Edge Power		> ±100 kHz, pre-emphasis off	—	—	–20	dBc
Transmit Adjacent Channel Power		> ±200 kHz, pre-emphasis off	—	–30	–26	dBc
Transmit Alternate Channel Power		> ±400 kHz, pre-emphasis off	—	–30	–26	dBc
Transmit Emissions		In-band (76–108 MHz)	—	—	–30	dBc
Output Capacitance Max[2]	C_{TUNE}		—	53	—	pF
Output Capacitance Min[2]	C_{TUNE}		—	5	—	pF
Pre-emphasis Time Constant[2]		TX_PREMPHASIS = 75 µs	70	75	80	µs
		TX_PREMPHASIS = 50 µs	45	50	54	µs
Audio SNR Mono[2]		Δf = 22.5 kHz, Mono, limiter off	58	63	—	dB
Audio SNR Stereo		Δf = 22.5 kHz, Δfpilot = 6.75 kHz, Stereo, limiter off	53	58	—	dB
Audio THD Mono		Δf = 75 kHz, Mono, limiter off	—	0.1	0.5	%

Notes:
1. FM transmitter performance specifications are subject to adherence to Silicon Laboratories guidelines in "AN383: Universal Antenna Selection and Layout Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers. Tested with test schematic (L = 120 nH, Q ≥ 30) shown in Figure 10 on page 19.
2. Guaranteed by characterization.
3. No measurable $\Delta fRF/\Delta V_{DD}$ at ΔV_{DD} of 500 mVpk-pk at 100 Hz to 10 kHz.

Table 10. FM Transmitter Characteristics[1] (Continued)

Test conditions: V_{RF} = 118 dBµV, stereo, Δf = 68.25 kHz, Δfpilot = 6.75 kHz, REFCLK = 32.768 kHz, 75 µs pre-emphasis, unless otherwise specified.
Production test conditions: V_{DD} = 3.3 V, V_{IO} = 3.3 V, T_A = 25 °C, F_{RF} = 98 MHz.
Characterization test conditions: V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C, F_{RF} = 76–108 MHz.
All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions.
Typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
Parameters are tested in production unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Audio THD Stereo[2]		Δf = 22.5 kHz, Δfpilot = 6.75 kHz, Stereo, limiter off	—	0.1	0.5	%
Audio Stereo Separation[2]		left channel only	30	35	—	dB
Sub Carrier Rejection Ratio	SCR		40	50	—	dB
Powerup Settling Time[2]			—	—	110	ms
Input Signal Level[2]	V_{AI}		—	—	0.636	V_{PK}
Frequency Flatness[2]		Mono, ±1.5 dB, Δf = 75 kHz, 0, 50, 75 µs pre-emphasis, limiter off	30	—	15 k	Hz
High Pass Corner Frequency[2]		Mono, –3 dB, Δf = 75 kHz, 0, 50, 75 µs pre-emphasis, limiter off	5	—	30	Hz
Low Pass Corner Frequency[2]		Mono, –3 dB, Δf = 75 kHz, 0, 50, 75 µs pre-emphasis, limiter off	15 k	—	16 k	Hz
Audio Imbalance		Mono	–1	—	1	dB
Pilot Modulation Rate Accuracy[2]		Δf = 68.25 kHz, Δfpilot = 6.75 kHz, Stereo	–10	—	10	%
Audio Modulation Rate Accuracy[2]		Δf = 68.25 kHz, Δfpilot = 6.75 kHz, Stereo	–10	—	10	%
Input Resistance[2]		LIATTEN[1:0] = 11	50	60	—	kΩ
Input Capacitance[2]			—	10	—	pF
Received Noise Level Accuracy (Si4720/21 Only)[2]		60 dBµV input, T_A = 25 ºC	—	54	—	dBuV

Notes:
1. FM transmitter performance specifications are subject to adherence to Silicon Laboratories guidelines in "AN383: Universal Antenna Selection and Layout Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers. Tested with test schematic (L = 120 nH, Q ≥ 30) shown in Figure 10 on page 19.
2. Guaranteed by characterization.
3. No measurable $\Delta fRF/\Delta V_{DD}$ at ΔV_{DD} of 500 mVpk-pk at 100 Hz to 10 kHz.

Table 11. Digital Audio Interface Characteristics (Transmit)

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK pulse width high	t_{DCH}		10	—	—	ns
DCLK pulse width low	t_{DCL}		10	—	—	ns
DFS set-up time to DCLK rising edge	$t_{SU:DFS}$		5	—	—	ns
DFS hold time from DCLK rising edge	$t_{HD:DFS}$		5	—	—	ns
DIN set-up time from DCLK rising edge	$t_{SU:DIN}$		5	—	—	ns
DIN hold time from DCLK rising edge	$t_{HD:DIN}$		5	—	—	ns
DCLK, DFS, DIN, Rise/Fall time	t_R t_F		—	—	10	ns
DCLK Tx Frequency[1,2]			1.0	—	40.0	MHz

Notes:

1. Guaranteed by characterization.
2. The DCLK frequency may be set below the minimum specification if DIGITAL_INPUT_SAMPLE_RATE is first set to 0 (disable).

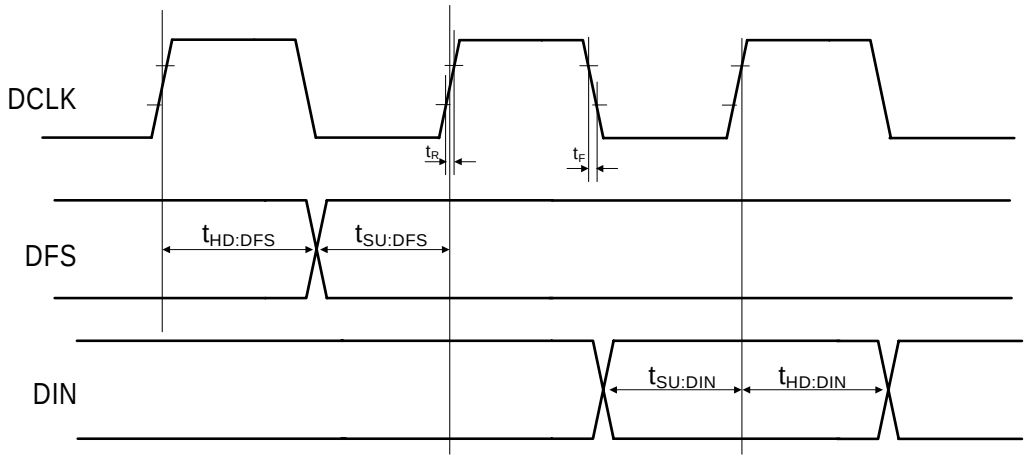


Figure 9. Digital Audio Interface Timing Parameters, I²S Mode

Table 12. FM Receive Power Scan Characteristics[1]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C, F_{RF} = 76–108 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tune and Signal Strength Measurement Time per Channel[2]			—	—	80	ms

Notes:
1. Settling time for ac coupling capacitors on the audio input pins after Receive to Transmit transition can take a few hundred milliseconds. The actual settling time depends on the values of the ac-coupling capacitors. Using digital audio input mode avoids this settling time.
2. Guaranteed by characterization.

Table 13. Reference Clock and Crystal Characteristics

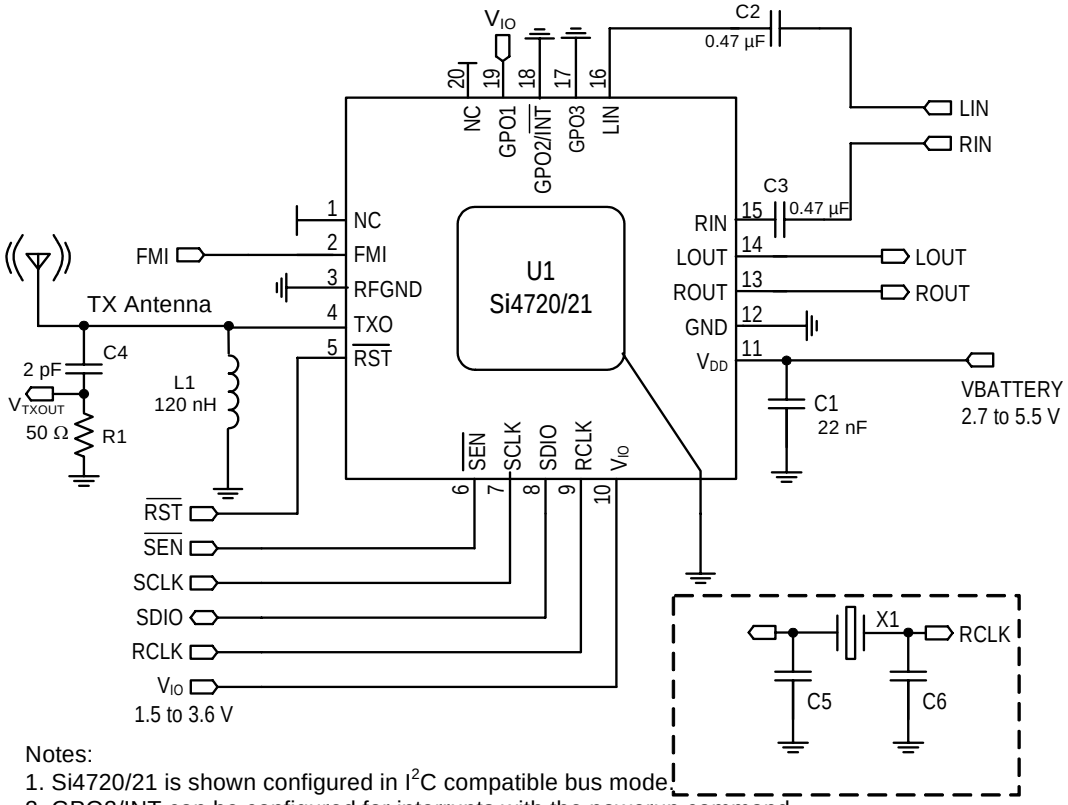
(V_{DD} = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
RCLK Supported Frequencies[1]			31.130	32.768	40,000	kHz
RCLK Frequency Tolerance[2]			–50	—	50	ppm
REFCLK_PRESCALE			1	—	4095	
REFCLK			31.130	32.768	34.406	kHz
Crystal Oscillator						
Crystal Oscillator Frequency			—	32.768	—	kHz
Crystal Frequency Tolerance[2]			–100	—	100	ppm
Board Capacitance			—	—	3.5	pF

Notes:
1. The Si4720/21 divides the RCLK input by REFCLK_PRESCALE to obtain REFCLK. There are some RCLK frequencies between 31.130 kHz and 40 MHz that are not supported. See “AN332: Si4704/05/06/1x/2x/3x/4x FM Transmitter/AM/FM/SW/LW/WB Receiver Programming Guide” for more details.
2. A frequency tolerance of ±50 ppm is required for FM seek/tune using 50 kHz channel spacing.

2. Test Circuit

2.1. Test Circuit Schematic



Notes:
1. Si4720/21 is shown configured in I^2C compatible bus mode.
2. GPO2/INT can be configured for interrupts with the powerup command.
3. To ensure proper operation and FM transmitter performance, follow the guidelines in "AN383: 3 mm x 3 mm QFN Universal Layout Guide."
   Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. LIN, RIN line inputs must be ac-coupled.

Figure 10. Test Circuit Schematic

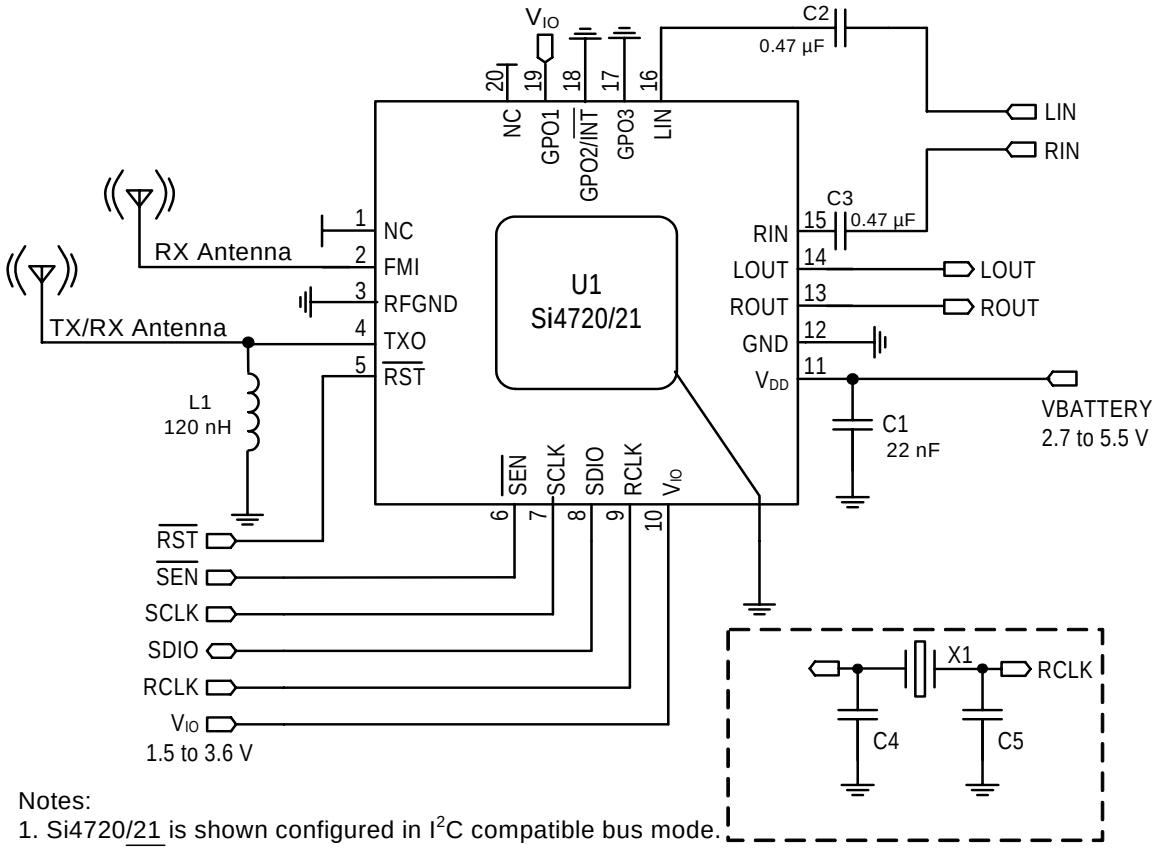
2.2. Test Circuit Bill of Materials

Table 14. Si4720/21 Test Circuit Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, 20%, Z5U/X7R	Murata
C2, C3	AC Coupling Capacitor, 0.47 µF	Murata
C4	2 pF, ±.05 pF, 06035JZR0AB	AVX
C5, C6	Crystal load capacitors, 22 pF, ±5%, COG (Optional: for crystal oscillator option)	Venkel
L1	120 nH inductor, Qmin = 30	Murata
R1	49.9 Ω, 5%	Murata
X1	32.768 kHz crystal (Optional: for crystal oscillator option)	Epson
U1	Si4720/21 FM Radio Transceiver	Silicon Laboratories

3. Typical Application Schematic

3.1. Analog Audio Inputs/Outputs



Notes:
1. Si4720/21 is shown configured in I²C compatible bus mode.
2. GPO2/INT can be configured for interrupts with the powerup command.
3. To ensure proper operation and FM transmitter performance, follow the guidelines in
   "AN383: 3 mm x 3 mm QFN Universal Layout Guide."
   Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. LIN, RIN line inputs must be ac-coupled.
5. Dedicated RX antenna at FMI input optional.

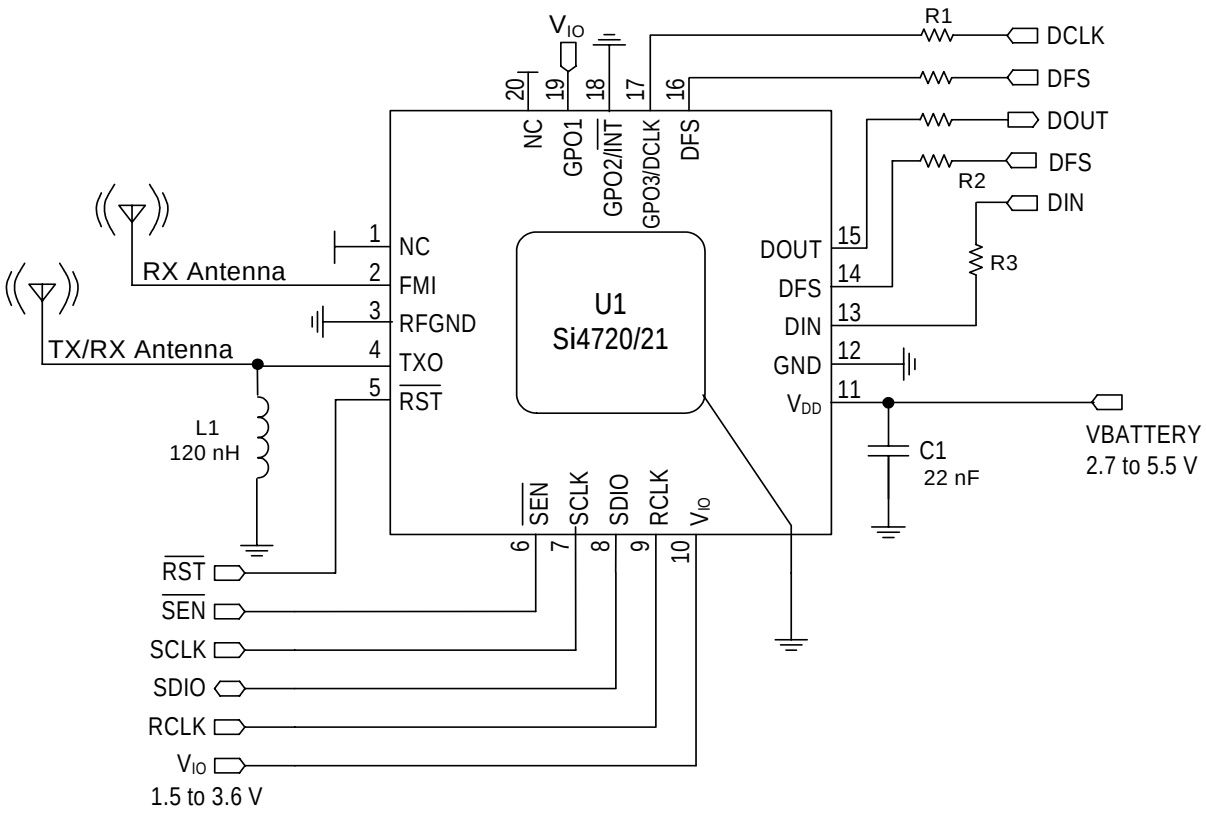
Figure 11. Analog Audio Inputs/Outputs (L_{IN}, R_{IN}, L_{OUT}, R_{OUT})

3.2. Typical Application Bill of Materials

Table 15. Si4720/21 Typical Application Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, 20%, Z5U/X7R	Murata
C2, C3	AC Coupling Capacitor, 0.47 µF	Murata
C4, C5	Crystal load capacitors, 22 pF, ±5%, COG (Optional: for crystal oscillator option)	Venkel
L1	120 nH inductor, Qmin = 30	Murata
X1	32.768 kHz crystal (Optional: for crystal oscillator option)	Epson
U1	Si4720/21 FM Radio Transceiver	Silicon Laboratories

3.3. Digital Audio Inputs/Outputs



Notes:
1. Si4720/21 is shown configured in I^2C compatible bus mode.
2. GPO2/INT can be configured for interrupts with the powerup command.
3. To ensure proper operation and FM transmitter performance, follow the guidelines in "AN383: Si47xx 3 mm x 3 mm QFN Universal Layout Guide." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. Dedicated RX antenna at FMI input optional.

Figure 12. Digital Audio Inputs (DIN, DFS, DCLK)

3.4. Typical Application Schematic Bill of Materials

Table 16. Si4720/21 Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, 20%, Z5U/X7R	Murata
C2, C3	AC Coupling Capacitor, 0.47 µF	Murata
L1	120 nH inductor, Qmin = 30	Murata
R1, R2	2 kΩ Resistor	Any
R3	600 Ω Resistor	Any
U1	Si4720/21 FM Radio Transceiver	Silicon Laboratories

4. Universal AM/FM RX/FM TX Application Schematic

Figure 13 shows an application schematic that supports the Si47xx family of 3 mm x 3 mm QFN products, including the Si4702/3/4/5 FM receivers, Si471x FM transmitters, Si472x FM transceivers, and Si473x AM/FM receivers.

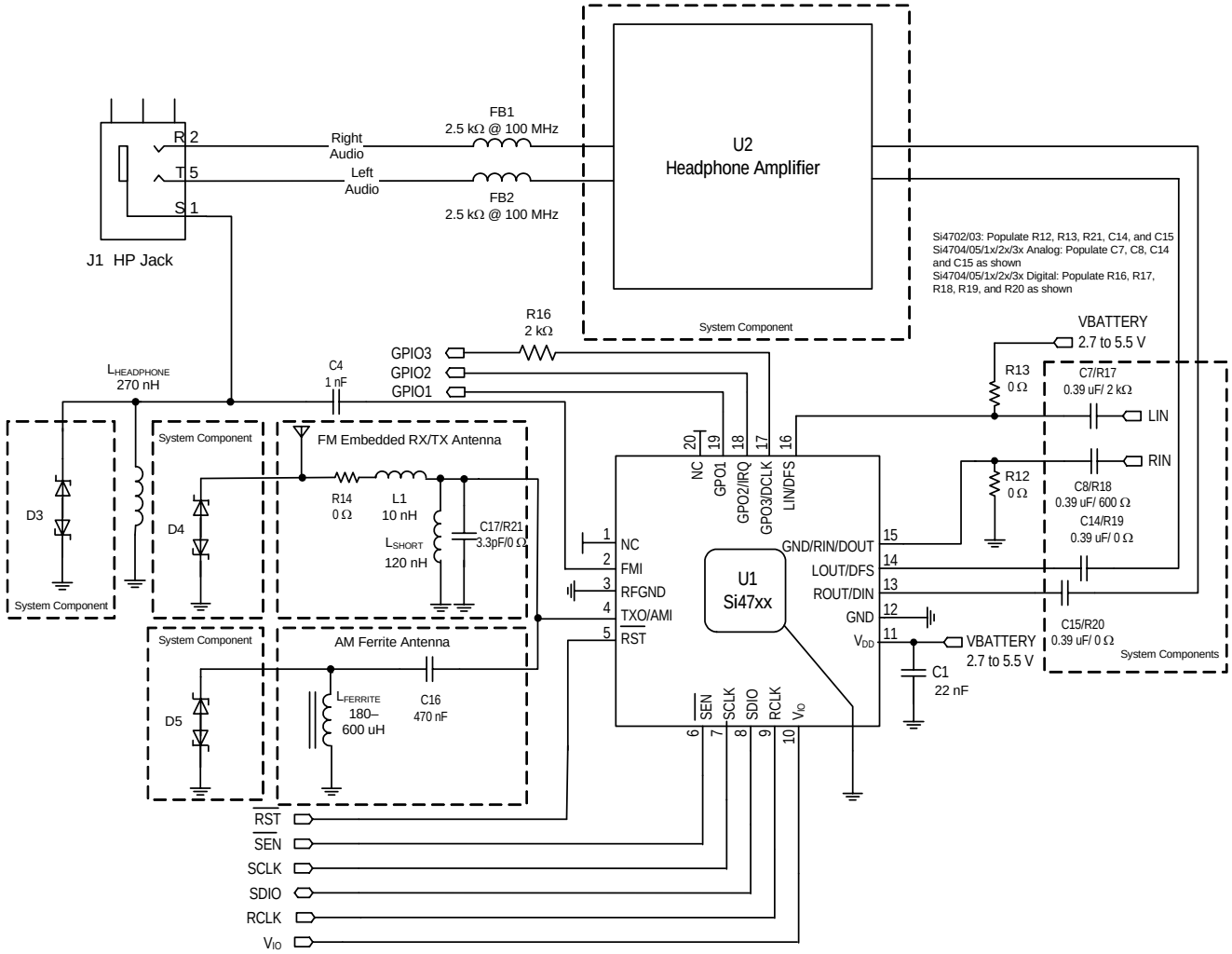


Figure 13. Universal AM/FM RX/FM TX Application Schematic

Following the schematic and layout recommendations detailed in “AN383: Universal Antenna Selection and Layout Guidelines” will result in optimal performance with the minimal application schematic shown in Figure 13. “Universal AM/FM RX/FM TX Application Schematic”. System components are those that are likely to be present for any tuner or transmitter design.

4.1. Universal AM/FM RX/FM TX Bill of Materials

The bill of materials for the expanded application schematic shown in Figure 13 is provided in Table 17. Refer to the individual device layout guides and antenna interface guides for a discussion of the purpose of each component.

Table 17. Universal AM/FM/RX/FM TX Bill of Materials

Designator	Description	Note
C1	Supply bypass capacitor, 22 nF, 10%, Z5U/X7R, 0402	
U1	Silicon Laboratories Si47xx, 3 mm x 3 mm, 20 pin, QFN	
R12, R13, R19, R20, R21	0 Ω jumper, 0402	R12, R13, and R21 for Si4702/03 Only
C16	AM antenna ac coupling capacitor, 470 nF, 20%, Z5U/X7R	AM Ferrite Antenna
LFERRITE	AM Ferrite loop stick, 180–600 µH	AM Ferrite Antenna
FB1,FB2	Ferrite bead, 2.5 kΩ @ 100 MHZ, 0603, Murata BLM18BD252SN1D	Headphone Antenna
LHEADPHONE	Headphone antenna matching inductor, 270 nH, 0603, Q>15, Murata LQW18ANR27J00D	Headphone Antenna
LSHORT	Embedded antenna matching inductor, 120 nH, 0603, Q>30, Murata LQW18ANR12J00D	Embedded Antenna
R14	Embedded antenna jumper, 2.2 Ω, 0402	Optional
C2	Supply bypass capacitor, 22 nF, 10%, Z5U/X7R, 0402	Optional
C3	Supply bypass capacitor, 100 nF, 10%, Z5U/X7R, 0402	Optional
C5, C6	Headphone amp output shunt capacitor, 100 pF, 10%, Z5U/X7R, 0402	Optional
R7-R11	Current limiting resistor, 20 Ω–2 kΩ, 0402	Optional
C12, C13	Crystal load capacitor, 22 pF, 5%, COG	Optional
X1	Crystal, Epson FC-135	Optional
C7, C8	Si47xx input ac coupling capacitor, 0.39 µF, X7R/X5R, 0402	System Component
D1-D5	ESD Diode, SOT23-3, California Micro Devices CM1214-01ST	System Component
C11	Supply bypass capacitor, 100 nF, 10%, Z5U/X7R, 0402	Headphone Amplifier
C4	Headphone antenna ac coupling capacitor, 1 nF, 10%, Z5U/X7R, 0402	Headphone Antenna
C9, C10	Headphone amp output ac coupling capacitor, 125 uF, X7R, 0805	Headphone Amplifier
C14, C15	Headphone amp input ac coupling capacitor, 0.39 µF, X7R/X5R, 0402	Headphone Amplifier
R1,R2,R3,R4	Headphone amp feedback/gain resistor, 20 kΩ, 0402	Headphone Amplifier
R5, R6	Headphone amp bleed resistor, 100 kΩ, 0402	Headphone Amplifier
U2	Headphone amplifier, National Semiconductor, LM4910MA	Headphone Amplifier
R16, R17	Current limiting resistor, 2 kΩ, 0402	System Component
R18	Current limiting resistor, 600 Ω, 0402	System Component
L1	VCO filter inductor, 10 nH, 0603, Q>30, Murata, LQW18ANR01J00D	Optional
C17	VCO filter capacitor, 3.3 pF, 0402, COG, Venkel, C0402COG2503R3JN	Optional

5. Functional Description

5.1. Overview

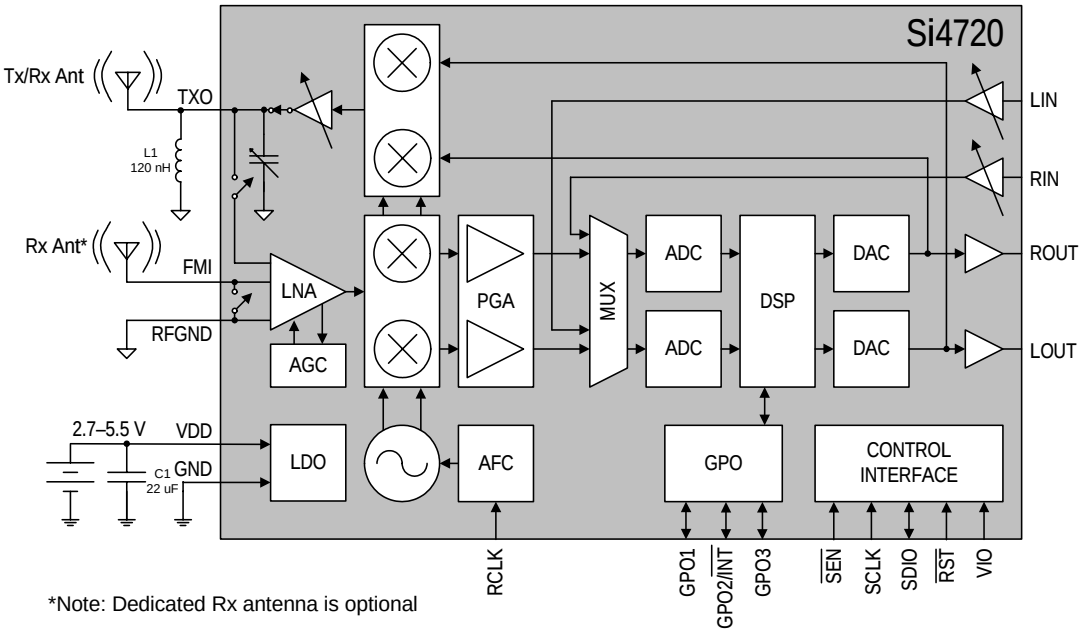


Figure 14. Functional Block Diagram

The Si4720/21 is the first single-chip FM radio transceiver. The proven and patented digital architecture of the Si4720/21 combines the functionality of the Si470x FM radio receiver with the Si471x FM transmitter, offering full FM receive and transmit capabilities in a single, ultra-small 3x3x0.55 mm QFN package. The device leverages Silicon Laboratories' highly successful and proven FM technology and offers unmatched integration and performance. FM receiver and transmit functionality may be added to any portable device by using this single chip. As with the Si470x and Si471x products, the Si4720/21 offers industry leading size, performance, low power consumption, and ease of use.

The Si4720/21 is the first FM radio transceiver integrated circuit to support a small loop antenna, which can be integrated into the enclosure or PCB of a portable device. This feature enables applications that also include Bluetooth functionality to perform FM radio reception without cables. For portable navigation devices, the Si4720's antenna architecture permits integration of the traffic messaging antenna into the enclosure of the portable device, and eliminates the need for external antenna cables.

The Si4720's digital integration reduces the required external components of traditional offerings, resulting in a solution requiring only an external inductor and bypass capacitor, and a PCB space of approximately 15 mm^2. The Si4720/21 is layout compatible with Silicon Laboratories' Si470x FM radio receivers, Si473x AM/FM radio receivers, and the Si471x FM radio transmitter solutions, allowing a single PCB layout to accommodate a variety of music features. High yield manufacturability, unmatched performance, easy design-in, and software programmability are key advantages of the Si4720.

The Si4720/21's integrated receive power scan function shares the same antenna as the transmitter allowing for a compact printed circuit board design. The device operates in half duplex mode, meaning the transmitter and receiver do not operate at the same time.

The Si4720/21 performs FM modulation in the digital domain to achieve high fidelity, optimal performance versus power consumption, and flexibility of design. The onboard DSP provides modulation adjustment and audio dynamic range control for optimum sound quality.

The Si4721 supports the European Radio Data System (RDS) and the US Radio Broadcast Data System (RBDS) including all the symbol encoding, block synchronization, and error correction functions. Using this feature, the Si4721 enables data such as artist name and song title to be transmitted to an RDS/RBDS receiver.

The transmit output (TXO) connects directly to the transmit antenna with only one external inductor to provide harmonic filtering. The output is programmable over a 10 dB voltage range in 1 dB steps. The TXO output pin can also be configured for loop antenna support. Users are responsible for complying with local regulations on RF transmission (FCC, ETSI, ARIB, etc.).

The digital audio interface operates in slave mode and supports a variety of MSB-first audio data formats including I^2S and left-justified modes. The interface has three pins: digital data input (DIN), digital frame synchronization input (DFS), and a digital bit synchronization input clock (DCLK). The Si4720/21 supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor.

The Si4720/21 includes a low-noise stereo line input (LIN/RIN) with programmable attenuation. To ensure optimal audio performance, the Si4720/21 has a transmit line input property that allows the user to specify the peak amplitude of the analog input required to reach maximum deviation level. The deviation levels of the audio, pilot, and RDS/RBDS signals can be independently programmed to customize FM transmitter designs. The Si4720/21 has a programmable low audio level and high audio level indicators that allows the user to selectively enable and disable the carrier based on the presence of audio content. In addition, the device provides an overmodulation indicator to allow the user to dynamically set the maximum deviation level. The Si4720/21 has a programmable audio dynamic range control that can be used to reduce the dynamic range of the audio input signal and increase the volume at the receiver. These features can dramatically improve the end user’s listening experience.

The Si4720/21 is reset by applying a logic low on the RST pin. This causes all register values to be reset to their default values. The digital input/output interface supply (V_{IO}) provides voltage to the RST, SEN, SDIO, RCLK, DIN, DFS, and DCLK pins and can be connected to the audio baseband processor's supply voltage to save power and remove the need for voltage level translators. RCLK is not required for register operation.

The Si4720/21 reference clock is programmable, supporting many RCLK inputs as shown in Table 10.

The S4720/21 are part of a family of broadcast audio solutions offered in standard, 3 x 3 mm 20-pin QFN packages. All solutions are layout compatible, allowing a single PCB to accommodate various feature offerings.

The Si4720/21 includes line inputs to the on-chip analog-to-digital converters (ADC), a programmable reference clock input, and a configurable digital audio interface. The chip supports I^2C-compliant 2-wire, 8-bit SPI, and a 3-wire control interface.

5.2. Application Schematics and Operating Modes

The application schematic for the Si4720/21 is shown in Section "3. Typical Application Schematic" on page 20. The Si4720/21 supports selectable analog, digital, or concurrent analog and digital audio output modes. In the analog output mode, pin 13 is ROUT, pin 14 is LOUT, and pin 17 is GPO3. In the digital output mode, pin 15 is DOUT, pin 16 is DFS, and pin 17 is DCLK. Concurrent analog and digital audio output mode requires pins 13, 14, 15, 16, and 17. In addition to output mode, there is a clocking mode to clock the Si4720/21 from a reference clock or crystal oscillator. The user sets the operating modes with commands as described in Section "6. Commands and Properties" on page 36.

5.3. FM Receiver

The Si4720/21 FM receiver is based on the proven Si4700/01/02/03 FM radio receiver. The part leverages Silicon Laboratories' proven and patented Si4700/01 FM broadcast radio receiver digital architecture, delivering superior RF performance and interference rejection. The proven digital techniques provide excellent sensitivity in weak signal environments while providing superb selectivity and inter-modulation immunity in strong signal environments.

The FM receiver supports the worldwide FM broadcast band (76 to 108 MHz) with channel spacings of 50–200 kHz. The Low-IF architecture utilizes a single converter stage and digitizes the signal using a high-resolution analog-to-digital converter. The resulting digital signals are further processed through an on-chip DSP for digital channel selection, FM demodulation, and ultimately stereo audio output. The audio output can be directed either to an external headphone amplifier via analog in/out or to other system ICs through digital audio interface (I^2S).

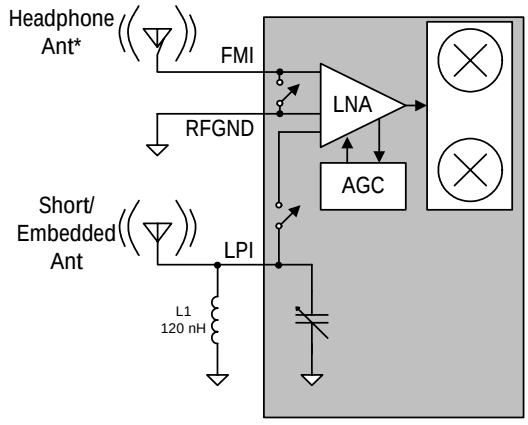
5.4. Integrated Antenna Support

The Si4720/21 is the first FM receiver to support the fast growing trend to integrate the FM receiver antenna into the device enclosure. The chip is designed with this function in mind from the outset, with multiple international patents pending, thus it is superior to many other options in price, board space, and performance.

The Si4720/21 supports an internal RX antenna allowing for "wire free" listening to FM over Bluetooth. The user can receive FM over the integrated RX antenna and stream it via Bluetooth to a Bluetooth-enabled headset.

Testing indicates that using Silicon Laboratories' patented techniques provides FM performance over an integrated antenna that can be very similar in many key metrics to performance using standard FM receive antennas (e.g., wired headset). Refer to “AN383: Antenna Selection and Universal Layout Guidelines” for additional details on the implementation of support for an integrated antenna.

Figure 15 shows a conceptual block diagram of the Si4720/21 architecture used to support the short antenna. The headphone/dedicated FM receive antenna is therefore optional. Host software can detect the presence of a headphone antenna and switch between the integrated antenna if desired.



*Note: Dedicated RX antenna is optional.

Figure 15. Conceptual Block Diagram of the Si4720/21 Short Antenna Support

5.5. Receiver Digital Audio Interface (Si4721 Only)

The digital audio interface operates in slave mode and supports three different audio data formats:

- I^2S
- Left-Justified
- DSP Mode

5.5.1. Audio Data Formats

In I^2S mode, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

In Left-Justified mode, by default the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of 1DCLK period. The left channel is transferred first, followed right away by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency, and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In addition, if preferred, the user can configure the MSB to be captured on the falling edge of DCLK via properties.

The number of audio bits can be configured for 8, 16, 20, or 24 bits.

5.5.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs on the audio baseband processor.

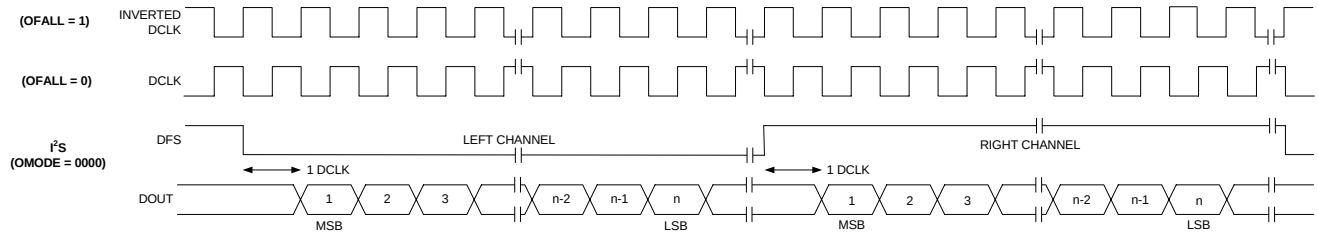


Figure 16. I²S Digital Audio Format

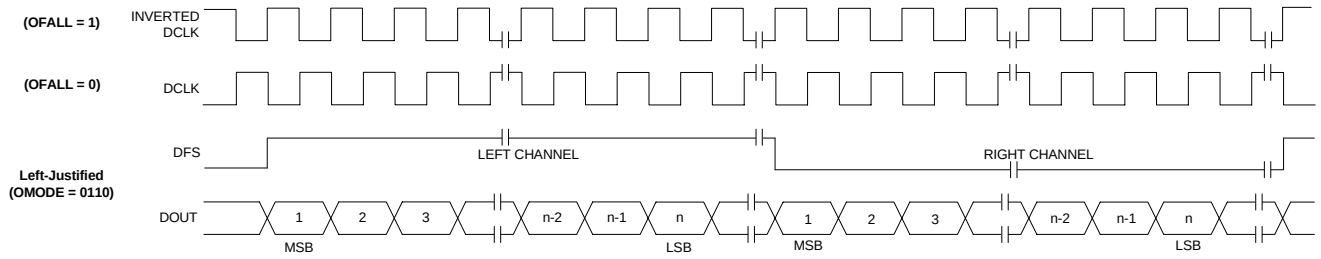


Figure 17. Left-Justified Digital Audio Format

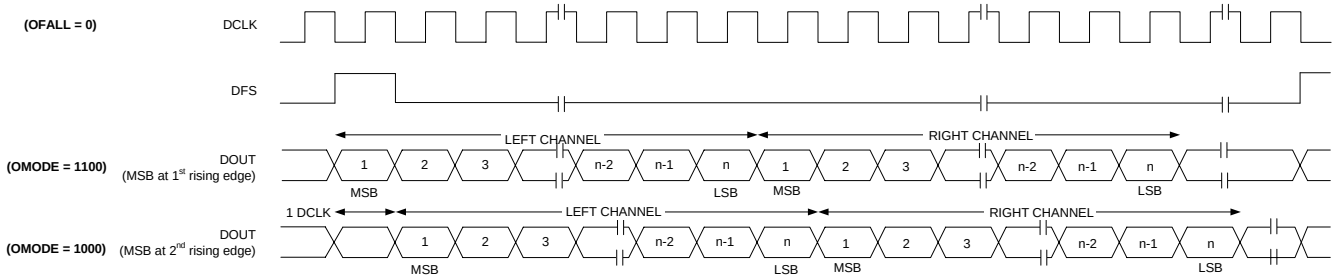


Figure 18. DSP Digital Audio Format

5.6. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 19 below.

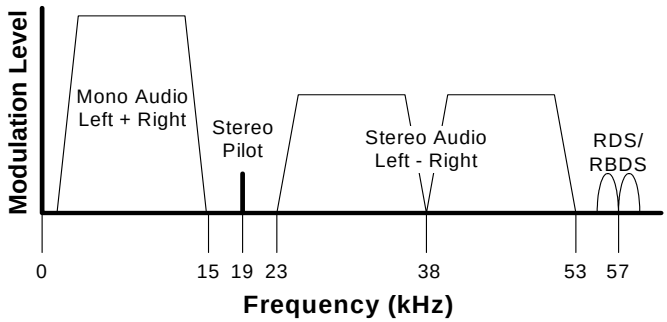


Figure 19. MPX Signal Spectrum

5.6.1. Stereo Decoder

The Si4720/21's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively. The Si4721 uses frequency information from the 19 kHz stereo pilot to recover the 57 kHz RDS/RBDS signal.

5.6.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Stereo/mono status can be monitored with the FM_RSQ_STATUS command. Mono operation can be forced with the FM_BLEND_MONO_THRESHOLD property.

5.7. De-Emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. The Si4720/21 incorporates a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis time constant is programmable to 50 or 75 µs and is set by the FM_DEEMPHASIS property.

5.8. Stereo DAC

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted. Volume is adjusted digitally with the RX_VOLUME property.

5.9. Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. The softmute attenuation level is adjustable using the FM_SOFT_MUTE_MAX_ATTENUATION property.

5.10. RDS/RBDS Processor (Si4721 Only)

The Si4721 implements an RDS/RBDS* processor for symbol decoding, block synchronization, error detection, and error correction.

The Si4721 device is user configurable and provides an optional interrupt when RDS is synchronized, loses synchronization, and/or the user configurable RDS FIFO threshold has been met.

The Si4721 reports RDS decoder synchronization status and detailed bit errors in the information word for each RDS block with the FM_RDS_STATUS command. The range of reportable block errors is 0, 1–2, 3–5, or 6+. More than six errors indicates that the corresponding block information word contains six or more non-correctable errors or that the block checkword contains errors.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

5.11. Tuning

The frequency synthesizer uses Silicon Laboratories' proven technology, including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the reference clock and adjusted with an automatic frequency control (AFC) servo loop during reception. The tuning frequency can be directly programmed using the FM_TUNE_FREQ and command. The Si4720/21 supports channel spacing of 50, 100, or 200 kHz in FM receiver mode.

5.12. Seek

Seek tuning will search up or down for a valid channel. Valid channels are found when the receive signal strength indicator (RSSI) and the signal-to-noise ratio (SNR) values exceed the set threshold. Using the SNR qualifier rather than solely relying on the more traditional RSSI qualifier can reduce false stops and increase the number of valid stations detected. Seek is initiated using the FM_SEEK_START command. The RSSI and SNR threshold settings are adjustable using properties (see Table 15).

Two seek options are available. The device will either wrap or stop at the band limits. If the seek operation is unable to find a channel, the device will indicate failure and return to the channel selected before the seek operation began.

5.13. Reference Clock

The Si4720/21 reference clock is programmable, supporting RCLK frequencies in Table 13. Refer to Table 3, “DC Characteristics,” on page 6 for switching voltage levels and Table 9, “FM Receiver Characteristics,” on page 13 for frequency tolerance information.

An onboard crystal oscillator is available to generate the 32.768 kHz reference when an external crystal and load capacitors are provided. Refer to "3. Typical Application Schematic" on page 20. This mode is enabled using the POWER_UP command. Refer to Table 21 "Si472x Property Summary".

The Si4720/21 performance may be affected by data activity on the SDIO bus when using the integrated internal oscillator. SDIO activity results from polling the tuner for status or communicating with other devices that share the SDIO bus. If there is SDIO bus activity while the Si4720/21 is performing the seek/tune function, the crystal oscillator may experience jitter, which may result in mistunes, false stops, and/or lower SNR.

For best seek/tune results, Silicon Laboratories recommends that all SDIO data traffic be suspended during Si4720/21 seek and tune operations. This is achieved by keeping the bus quiet for all other devices on the bus, and delaying tuner polling until the tune or seek operation is complete. The seek/tune complete (STC) interrupt should be used instead of polling to determine when a seek/tune operation is complete.

5.14. FM Transmitter

The transmitter (TX) integrates a stereo audio ADC to convert analog audio signals to high fidelity digital signals. Alternatively, digital audio signals can be applied to the Si4720/21 directly to reduce power consumption by eliminating the need to convert audio baseband signals to analog and back again to digital. Digital signal processing is used to perform the stereo MPX encoding and FM modulation to a low digital IF. Transmit baseband filters suppress out-of-channel noise and images from the digital low-IF signal. A quadrature single-sideband mixer up-converts the digital IF signal to RF, and internal RF filters suppress noise and harmonics to support the harmonic emission requirements of cellular phones, GPS, WLAN, and other wireless standards.

The TXO output has over 10 dB of output level control, programmable in approximately 1 dB steps. This large output range enables a variety of antennas to be used for transmit, such as a monopole stub antenna or a loop antenna. The 1 dB step size provides fine adjustment of the output voltage.

The TXO output requires only one external 120 nH inductor. The inductor is used to resonate the antenna and is automatically calibrated within the integrated circuit to provide the optimum output level and frequency response for supported transmit frequencies. Users are responsible for adjusting their system's radiated power levels to comply with local regulations on RF transmission (FCC, ETSI, ARIB, etc.).

5.15. Receive Power Scan

The Si4720/21 is the industry's first FM transmitter with integrated receive functionality to measure received signal strength. This has been designed to specifically handle various antenna lengths including integrated PCB antennas, wire antennas, and loop antennas, allowing it to share the same antenna as the transmitter. The receive function reuses the on-chip varactor from the transmitter to optimize the receive signal power applied to the front-end amplifier. Auto-calibration of the varactor occurs with each tune command for consistent performance across the FM band.

5.15.1. Stereo Encoder

Figure 19 shows an example modulation level breakdown for the various components of a typical MPX signal.

The total modulation level for the MPX signal shown in Figure 19, assuming no correlation, is equal to the arithmetic sum of each of the subchannel levels resulting in 102.67 percent modulation or a peak frequency deviation of 77.0025 kHz (an instantaneous frequency deviation of 75 kHz corresponds to 100 percent modulation). Frequency deviation is related to the amplitude of the MPX signal by a gain constant, K_{VCO}, as given by the following equation:

$$\Delta f = K_{VCO} A_m$$

where Δf is the frequency deviation; K_{VCO} is the voltage-to-frequency gain constant, and A_m is the amplitude of the MPX message signal. For a fixed K_{VCO}, the amplitude of all the subchannel signals within the MPX message signal must be scaled to give the appropriate total frequency deviation.

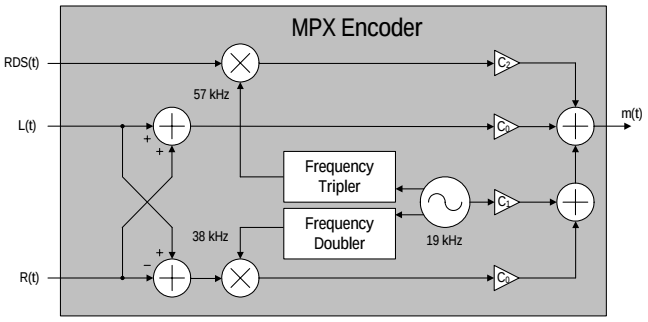


Figure 20. MPX Encoder

Figure 20 shows a conceptual block diagram of an MPX encoder used to generate the MPX signal. L(t) and R(t) denote the time domain waveforms from the left and right audio channels, and RDS(t) denotes the time domain waveform of the RDS/RBDS signal.

The MPX message signal can be expressed as follows:

$$m(t) = C_0[L(t) + R(t)] + C_1 \cos(2\pi 19\ kHz) + C_0[L(t) - R(t)] \cos(2\pi 38\ kHz) + C_2 RDS(t) \cos(2\pi 57\ kHz)$$

where C_0, C_1, and C_2 are gains used to scale the amplitudes of the audio signals (L(t) ± R(t)), the 19 kHz pilot tone, and the RDS subcarrier respectively, to generate the appropriate modulation level. To achieve the modulation levels of Figure 20 with K_{VCO} = 75 kHz/V, C_0 would be set to 0.45; C_1 would be set to 0.1, and C_2 would be set to 0.0267 giving a peak audio frequency deviation of 0.9 x 75 kHz = 67.5 kHz, a peak pilot frequency deviation of 0.1 x 75 kHz = 7.5 kHz, and a peak RDS frequency deviation of 0.0267 x 75 kHz = 2.0025 kHz for a total peak frequency deviation of 77.0025 kHz.

In the Si4720/21, the peak audio, pilot, and RDS frequency deviations can be programmed directly with the Transmit Audio, Pilot, and RDS Deviation commands with an accuracy of 10 Hz. For the example in Figure 20, the Transmit Audio Deviation is

programmed with the value 6750, the Transmit Pilot Deviation with 750, and the Transmit RDS Deviation with 200, generating peak audio frequency deviations of 67.5 kHz, peak pilot deviations of 7.5 kHz, and peak RDS deviations of 2.0 kHz for a total peak frequency deviation of 77 kHz. The total peak transmit frequency deviation of the Si4720/21 can range from 0 to 100 kHz and is equal to the arithmetic sum of the Transmit Audio, Pilot, and RDS deviations. Users must comply with local regulations on radio frequency transmissions.

Each of the individual deviations (transmit audio, pilot, and RDS) can be independently programmed; however, the total peak frequency deviation cannot exceed 100 kHz.

The Si4720/21 provides an overmodulation indicator to allow the user to dynamically set the maximum deviation level. If the instantaneous frequency exceeds the deviation level specified by the TX_AUDIO_DEVIATION property, the SQINT interrupt bit (and optional interrupt) will be set.

5.16. Transmitter Digital Audio Interface

The digital audio interface operates in slave mode and supports 3 different audio data formats:

1. I^2S
2. Left-Justified
3. DSP Mode

5.16.1. Audio Data Formats

In I^2S mode, the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The Left Channel is transferred first when the DFS is low, and the Right Channel is transferred when the DFS is high.

In Left-Justified mode, the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The Left Channel is transferred first when the DFS is high, and the Right Channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of 1 DCLK period. The Left Channel is transferred first, followed right away by the Right Channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word.

The number of audio bits can be configured for 8, 16, 20, or 24 bits.

5.16.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor. The sampling rate is selected using the DIGITAL_INPUT_SAMPLE_RATE property.

The device supports DCLK frequencies above 1 MHz. After powerup the DIGITAL_INPUT_SAMPLE_RATE property defaults to 0 (disabled). After DCLK is supplied, the DIGITAL_INPUT_SAMPLE_RATE property should be set to the desired audio sample rate such as 32, 40, 44.1, or 48 kHz. The DIGITAL_INPUT_SAMPLE_RATE property must be set to 0 before DCLK is removed or the DCLK frequency drops below 1 MHz. A device reset is required if this requirement is not followed.

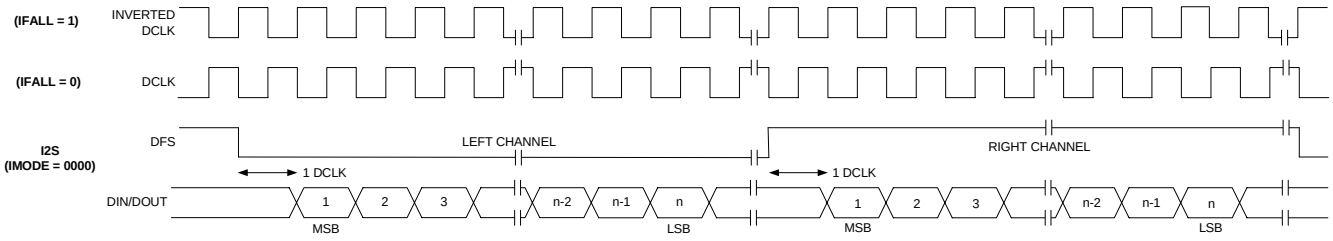


Figure 21. I^2S Digital Audio Format

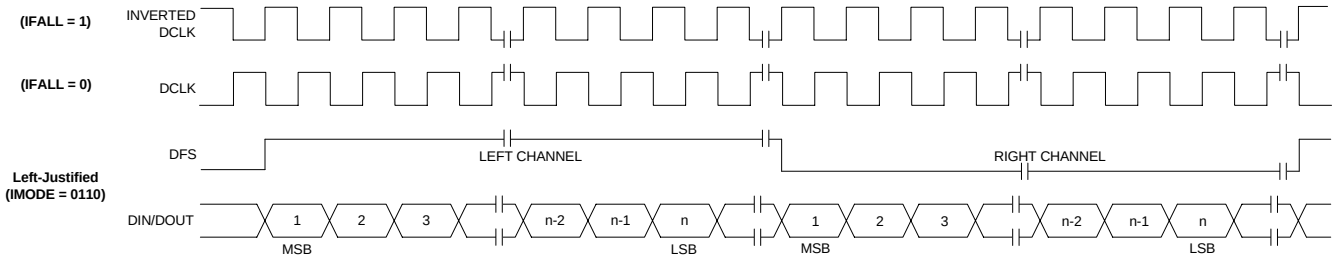


Figure 22. Left-Justified Digital Audio Format

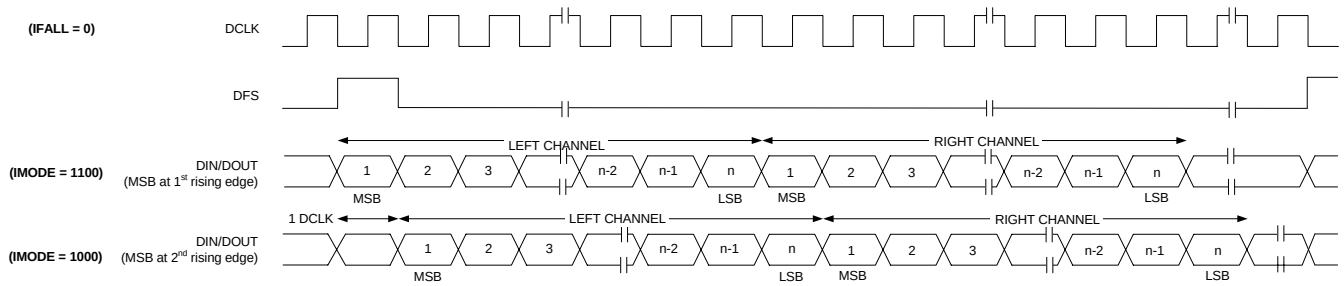


Figure 23. DSP Digital Audio Format

5.17. Line Input

The Si4720/21 provides left and right channel line inputs (LIN and RIN). The inputs are high-impedance and low-capacitance, suited to receiving line level signals from external audio baseband processors. Both line inputs are low-noise inputs with programmable attenuation. Passive and active anti-aliasing filters are incorporated to prevent high frequencies from aliasing into the audio band and degrading performance.

To ensure optimal audio performance, the Si4720/21 has a TX_LINE_INPUT_LEVEL property that allows the user to specify the peak amplitude of the analog input (LILEVEL[9:0]) required to reach the maximum deviation level programmed in the audio deviation property, TX_AUDIO_DEVIATION. A corresponding line input attenuation code, LIATTEN[1:0], is also selected by the expected peak amplitude level. Table 18 shows the line attenuation codes.

Table 18. Line Attenuation Codes

LIATTEN[1:0]	Peak Input Voltage [mV]	RIN/LIN Input Resistance [kΩ]
00	190	396
01	301	100
10	416	74
11	636	60

The line attenuation code is chosen by picking the lowest Peak Input Voltage in Table 18 that is just above the expected peak input voltage coming from the audio baseband processor. For example, if the expected peak input voltage from the audio baseband processor is 400 mV, the user chooses LIATTEN[1:0] = 10 since the Peak Input Voltage of 416 mV associated with LIATTEN[1:0] = 10 is just greater than the expected peak input voltage of 400 mV. The user also enters 400 mV into the LILEVEL[9:0] to associate this input level to the maximum frequency deviation level programmed into the audio deviation property. Note that selecting a particular value of LIATTEN[1:0] changes the input resistance of the LIN and RIN pins. This feature is used for cases where the expected peak input level exceeds the maximum input level of the LIN and RIN pins.

The maximum analog input level is 636 mVpK. If the analog input level from the audio baseband processor exceeds this voltage, series resistors must be inserted in front of the LIN and RIN pins to attenuate the voltage such that it is within the allowable operating range. For example, if the audio baseband's expected peak amplitude is 900 mV and the V_{IO} supply voltage is 1.8 V, the designer can use 30 kΩ series resistors in front of the LIN and RIN pins and select LIATTEN[1:0] = 11. The resulting expected peak input voltage at the LIN/RIN pins is 600 mV, since this is just a voltage divider between the LIN/RIN input resistance (see Table 18, 60 kΩ for this example) and the external resistor. Note that the Peak Input Voltage corresponding to the chosen

LIATTEN[1:0] code still needs to satisfy the condition of being just greater than the attenuated voltage. In this example, a line attenuation code of LIATTEN[1:0] = 11 has a Peak Input Voltage of 636 mV, which is just greater than the expected peak attenuated voltage of 600 mV. Also, the expected peak attenuated voltage is entered into the LILEVEL[9:0] parameter. Again, in this example, 600 mV is entered into LILVEVEL[9:0]. This example shows one possible solution, but many other solutions exist. The optimal solution is to apply the largest possible voltage to the LIN and RIN pins for signal-to-noise considerations; however, practical resistor values may limit the choices.

Note that the TX_LINE_INPUT_LEVEL parameter will affect the high-pass filter characteristics of the ac-coupling capacitors and the resistance of the audio inputs.

The Si4720/21 has a programmable low audio level and high audio level indicators that allows the user to selectively enable and disable the carrier based on the presence of audio content. The TX_ASQ_LEVEL_LOW and TX_ASQ_LEVEL_HIGH parameters set the low level and high level thresholds in dBFS, respectively. The time required for the audio level to be below the low threshold is set with the TX_ASQ_DURATION_LOW parameter, and similarly, the time required for the audio level to be above the high threshold is set with the TX_ASQ_DURATION_HIGH parameter.

5.18. Audio Dynamic Range Control

The Si4720/21 includes digital audio dynamic range control with programmable gain, threshold, attack rate, and release rate. The total dynamic range reduction is set by the gain value and the audio output compression above the threshold is equal to Threshold/(Gain + Threshold) in dB. The gain specified cannot be larger than the absolute value of the threshold. This feature can also be disabled if audio compression is not desired.

The audio dynamic range control can be used to reduce the dynamic range of the audio signal, which improves the listening experience on the FM receiver. Audio dynamic range reduction increases the transmit volume by decreasing the peak amplitudes of audio signals and increasing the root mean square content of the audio signal. In other words, it amplifies signals below a threshold by a fixed gain and compresses audio signals above a threshold by the ratio of Threshold/(Gain + Threshold). Figure 24 shows an example transfer function of an audio dynamic range controller with the threshold set at –40 dBFS and a Gain = 20 dB relative to an uncompressed transfer function.

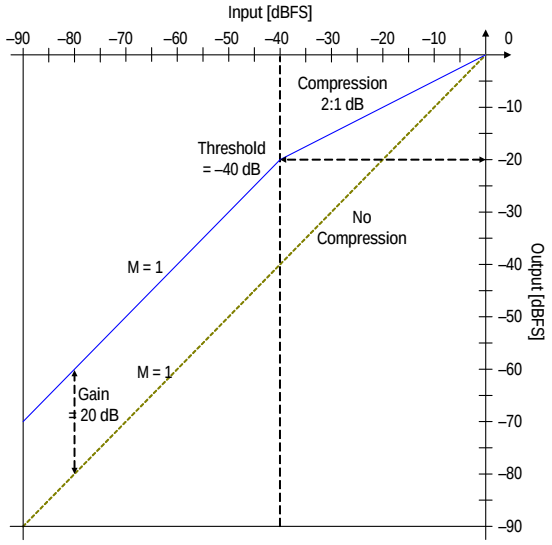


Figure 24. Audio Dynamic Range Transfer Function

For input signals below the threshold of –40 dBFS, the output signal is amplified or gained up by 20 dB relative to an uncompressed signal. Audio inputs above the threshold are compressed by a 2 to 1 dB ratio, meaning that every 2 dB increase in audio input level above the threshold results in an audio output increase of 1 dB. In this example, the input dynamic range of 90 dB is reduced to an output dynamic range of 70 dB.

Figure 25 shows the time domain characteristics of the audio dynamic range controller. The attack rate sets the speed with which the audio dynamic range controller responds to changes in the input level, and the release rate sets the speed with which the audio dynamic range controller returns to no compression once the audio input level drops below the threshold.

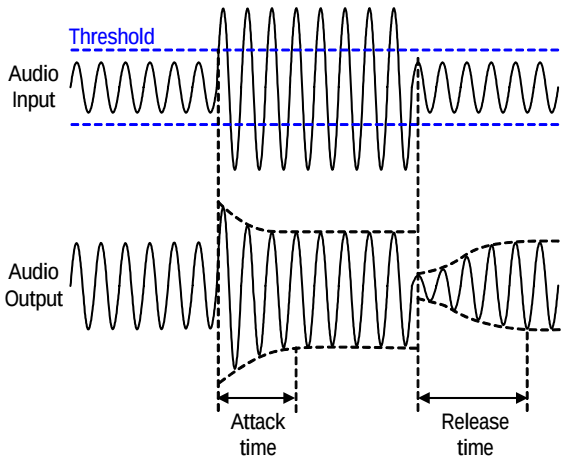


Figure 25. Time Domain Characteristics of the Audio Dynamic Range Controller

5.19. Audio Limiter

The 4720/21 also includes a digital audio limiter. The audio limiter prevents over-modulation of the FM transmit output by dynamically attenuating peaks in the audio input signal that exceed a programmable threshold. The limiter threshold is set to the programmed audio deviation + ten percent. The threshold ensures that the output signal audio deviation does not exceed the programmed levels, avoiding audible artifacts or distortion in the target FM receiver, and complying with FCC or ETSI regulatory standards.

The limiter performs as a peak detector with an attack rate set to one audio sample, resulting in an almost immediate attenuation of the input peak. The recover rate is programmable to the customer's preference, and is set by default to 5 ms. This is the recommended setting to avoid audible pumping or popping. Refer to "AN332: Universal Programming Guide."

5.20. Pre-emphasis and De-emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. All FM receivers incorporate a de-emphasis filter that attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The pre-emphasis time constant is programmable to 50 or 75 µs and is set by using the TX_PREEMPHASIS property.

5.21. RDS/RBDS Processor (Si4721 Only)

The Si4721 implements an RDS/RBDS* processor for symbol encoding, block synchronization, and error correction. Digital data can be transmitted with the Si4721 RDS/RBDS encoding feature.

RDS transmission is supported with three different modes. The first mode is the simplest mode and requires no additional user support except for pre-loading the desired RDS PI and PTY codes and up to 12 8-byte PS character strings. The Si4721 will transmit the PI code and rotate through the transmission of the PS character strings with no further control required from outside the device. The second mode allows for more complicated transmissions. The PI and PTY codes are written to the device as in mode 1. The remaining blocks (B, C, and D) are written to a 252 byte buffer. This buffer can hold 42 sets of BCD blocks. The Si4721 creates RDS groups by creating block A from the PI code, concatenating blocks BCD from the buffer, and rotating through the buffer. The BCD buffer is circular; so, the pattern is repeated until the buffer is changed. Finally, the third mode allows the outside controller to burst data into the BCD buffer, which emulates a FIFO. The data does not repeat, but, when the buffer is nearly empty, the Si4721 signals the outside device to initiate another data burst. This mode permits the outside device to use any RDS functionality (including open data applications) that it wants.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

5.22. Tuning

The frequency synthesizer uses Silicon Laboratories' proven technology including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to upconvert the low intermediate frequency to RF. The VCO frequency is locked to the reference clock and adjusted with an automatic frequency control (AFC) servo loop during transmission. The tuning frequency can be directly programmed with commands. For example, to tune to 98.1 MHz, the user writes the TX_TUNE_FREQ command with an argument = 9810. The Si4720/21 supports channel spacing of 50, 100, or 200 kHz.

5.23. Reference Clock

The Si4720/21 reference clock is programmable, supporting RCLK frequencies from 31.130 kHz to 40 MHz. The RCLK frequency divided by an integer number (the prescaler value) must fall in the range of 31,130 to 34,406 Hz. Therefore, the range of RCLK frequencies is not continuous below frequencies of 311.3 kHz. The default RCLK frequency is 32.768 kHz. Please refer to "AN332: Universal Programming Guide" for using other RCLK frequencies.

5.24. Control Interface

A serial port slave interface is provided; this allows an external controller to send commands to the Si4720/21 and receive responses from the device. The serial port can operate in three bus modes: 2-wire mode, SPI mode, or 3-wire mode. The Si4720/21 selects the bus mode by sampling the state of the GPO1 and GPO2/INT pins on the rising edge of RST. The GPO1 pin includes an internal pull-up resistor that is connected while RST is low, and the GPO2/INT pin includes an internal pull-down resistor that is connected while RST is low. Therefore, it is only necessary for the user to actively drive pins that differ from these states.

Table 19. Bus Mode Select on Rising Edge of RST

Bus Mode	GPO1	GPO2/INT
2-Wire	1	0
SPI	1	1 (must drive)
3-Wire	0 (must drive)	0

After the rising edge of RST, the pins, GPO1 and GPO2/INT, are used as general-purpose output (O) pins as described in Section “5.15. GPO Outputs”. In any bus mode, commands may only be sent after V_{IO} and V_{DD} supplies are applied.

5.24.1. 2-Wire Control Interface Mode

When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of RST, and stays high until after the first start condition. Also, a start condition must not occur within 300 ns before the rising edge of RST.

2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a seven bit device address followed by a read/write bit (read = 1, write = 0). The Si4720/21 acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the Si4720/21 responds to only a single device address, this address can be changed with the SEN pin (note that the SEN pin is not used for signaling in 2-wire mode). When SEN = 0, the seven-bit device address is 0010001. When SEN = 1, the address is 1100011.

For write operations, the user then sends an eight bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The Si4720/21 acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to eight data bytes in a single two-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si4720/21 has acknowledged the control byte, it drives an eight-bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction ends. The user may read up to 16 data bytes in a single two-wire transaction. These bytes contain the response data from the Si4720/21.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high.

For details on timing specifications and diagrams, refer to Table 5, “2-Wire Control Interface Characteristics[1,2,3],” on page 8, Figure 2, “2-Wire Control Interface Read and Write Timing Parameters,” on page 9, and Figure 3, “2-Wire Control Interface Read and Write Timing Diagram,” on page 9.

5.24.2. SPI Control Interface Mode

When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

SPI bus mode uses the SCLK, SDIO, and SEN pins for read/write operations. For reads, the user can choose to receive data from the device on either SDIO or GPO1. A transaction begins when the user drives SEN low. The user then pulses SCLK eight times while driving an 8-bit control byte (MSB first) serially on SDIO. The device captures the data on rising edges of SCLK. The control byte must have one of these values:

0x48 = write eight command/argument bytes (user drives write data on SDIO)

0x80 = read status byte (device drives read data on SDIO)

0xA0 = read status byte (device drives read data on GPO1)

0xC0 = read 16 response bytes (device drives read data on SDIO)

0xE0 = read 16 response bytes (device drives read data on GPO1)

When writing a command, after the control byte has been written, the user must drive exactly eight data bytes (a command byte and seven argument bytes) on SDIO. The data will be captured by the device on the rising edges of SCLK. After all eight data bytes have been written, the user raises SEN after the last falling edge of SCLK to end the transaction.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high). In SPI mode, this is done by sending control byte 0x80 or 0xA0, followed by reading a single byte on SDIO or GPO1. The Si4720/21 changes the state of SDIO or GPO1 after the falling edges of SCLK. Data should be captured by the user on the rising edges of SCLK. After the status byte has been read, the user raises SEN after the last falling edge of SCLK to end the transaction.

When reading a response, the user must read exactly 16 data bytes after sending the control byte. It is recommended that the user keep SEN low until all bytes have transferred. However, it will not disrupt the protocol if SEN temporarily goes high at any time, as long as the user does not change the state of SCLK while SEN is high. After 16 bytes have been read, the user raises SEN after the last falling edge of SCLK to end the transaction.

At the end of any SPI transaction, the user must drive SEN high after the final falling edge of SCLK. At any

time during a transaction, if $\overline{SEN}$ is sampled high by the device on a rising edge of SCLK, the transaction will be aborted. When $\overline{SEN}$ is high, SCLK may toggle without affecting the device.

For details on timing specifications and diagrams, refer to Figure 6 and Figure 7 on page 11.

5.24.3. 3-Wire Control Interface Mode

When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

3-wire bus mode uses the SCLK, SDIO and $\overline{SEN}$ pins. A transaction begins when the system controller drives $\overline{SEN}$ low. Next, the system controller drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word is comprised of a three bit chip address (A7:A5 = 101b), a read/write bit (write = 0, read = 1), the chip address (A4 = 0), and a four bit register address (A3:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turnaround. Next, the Si4720/21 drives the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets $\overline{SEN}$ high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while $\overline{SEN}$ is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

For details on timing specifications and diagrams, refer to Table 6, “3-Wire Control Interface Characteristics,” on page 10, Figure 4, “3-Wire Control Interface Write Timing Parameters,” on page 10, and Figure 5, “3-Wire Control Interface Read Timing Parameters,” on page 10.

5.25. GPO Outputs

The Si4720/21 provides three general-purpose output pins. The GPO pins can be configured to output a constant low, constant high, or high-Z. The GPO pins are multiplexed with the bus mode pins or DCLK depending on the application schematic of the device. GPO2/$\overline{INT}$ can be configured to provide interrupts for seek and tune complete, receive signal quality, and RDS.

5.26. Reset, Powerup, and Powerdown

Setting the RST pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RST pin high will bring the device out of reset and place it in powerdown mode.

A powerdown mode is available to reduce power consumption when the part is idle. Putting the device in powerdown mode will disable analog and digital circuitry and keep the bus active. For more information concerning Reset, Powerup, Powerdown, and Initialization, refer to “AN332: Universal Programming Guide.”

5.27. Programming with Commands

To ease development time and offer maximum customization, the Si4720/21 provides a simple yet powerful software interface to program the transmitter. The device is programmed using commands, arguments, properties, and responses.

To perform an action, the user writes a command byte and associated arguments causing the chip to execute the given command. Commands control actions, such as powering up the device, shutting down the device, or tuning to a station. Arguments are specific to a given command and are used to modify the command. For example, after the TX_TUNE_FREQ command, arguments are required to set the tune frequency. A complete list of commands is available in Table 17, “Si471x Command Summary,” on page 30.

Properties are a special command argument used to modify the default chip operation and are generally configured immediately after powerup. Examples of properties are TX_PREEMPHASIS and GPO_CONFIGURE. A complete list of properties is available in Table 21, “Si472x Property Summary,” on page 37.

Responses provide the user information and are echoed after a command and associated arguments are issued. At a minimum, all commands provide a one-byte status update indicating interrupt and clear-to-send status information. For a detailed description of using the commands and properties of the Si4720/21, see “AN332: Universal Programming Guide.”

6. Commands and Properties

Table 20. Si472x Command Summary

Cmd	Name	Description
Transmit Commands		
0x01	POWER_UP	Power up device and mode selection. Modes include FM transmit and analog/digital audio interface configuration.
0x10	GET_REV	Returns revision information on the device.
0x11	POWER_DOWN	Power down device.
0x12	SET_PROPERTY	Sets the value of a property.
0x13	GET_PROPERTY	Retrieves a property's value.
0x14	GET_INT_STATUS	Read interrupt status bits.
0x15	PATCH_ARGS	Reserved command used for patch file downloads.
0x16	PATCH_DATA	Reserved command used for patch file downloads.
0x30	TX_TUNE_FREQ	Tunes to given transmit frequency.
0x31	TX_TUNE_POWER	Sets the output power level and tunes the antenna capacitor.
0x32	TX_TUNE_MEASURE	Measure the received noise level at the specified frequency.
0x33	TX_TUNE_STATUS	Queries the status of a previously sent TX Tune Freq, TX Tune Power, or TX Tune Measure command.
0x34	TX_ASQ_STATUS	Queries the TX status and input audio signal metrics.
0x35	TX_RDS_BUFF	Queries the status of the RDS Group Buffer and loads new data into buffer.
0x36	TX_RDS_PS	Set up default PS strings.
0x80	GPIO_CTL	Configures GPO1, 2, and 3 as output or Hi-Z.
0x81	GPIO_SET	Sets GPO1, 2, and 3 output level (low or high).
Receive Commands		
0x01	POWER_UP	Power up device and mode selection.
0x10	GET_REV	Returns revision information on the device.
0x11	POWER_DOWN	Power down device.
0x12	SET_PROPERTY	Sets the value of a property.
0x13	GET_PROPERTY	Retrieves a property's value.
0x14	GET_INT_STATUS	Reads interrupt status bits.
0x15	PATCH_ARGS	Reserved command used for patch file downloads.
0x16	PATCH_DATA	Reserved command used for patch file downloads.
0x20	FM_TUNE_FREQ	Selects the FM tuning frequency.
0x21	FM_SEEK_START	Begins searching for a valid frequency.
0x22	FM_TUNE_STATUS	Queries the status of previous FM_TUNE_FREQ or FM_SEEK_START command.
0x23	FM_RSQ_STATUS	Queries the status of the Received Signal Quality (RSQ) of the current channel.

Table 20. Si472x Command Summary (Continued)

0x24	FM_RDS_STATUS	Returns RDS information for current channel and reads an entry from RDS FIFO (Si4721 only).
0x27	FM_AGC_STATUS	Queries the current AGC settings
0x28	FM_AGC_OVERRIDE	Override AGC setting by disabling and forcing it to a fixed value
0x80	GPIO_CTL	Configures GPO1, 2, and 3 as output or Hi-Z.
0x81	GPIO_SET	Sets GPO1, 2, and 3 output level (low or high).

Table 21. Si472x Property Summary

Prop	Name	Description	Default
Transmit Properties			
0x0001	GPO_IEN	Enables interrupt sources.	0x0000
0x0101	DIGITAL_INPUT _FORMAT	Configures the digital input format.	0x0000
0x0103	DIGITAL_INPUT _SAMPLE_RATE	Configures the digital input sample rate in 1 Hz steps. Default is 0.	0x0000
0x0201	REFCLK_FREQ	Sets frequency of the reference clock in Hz. The range is 31130 to 34406 Hz, or 0 to disable the AFC. Default is 32768 Hz.	0x8000
0x0202	REFCLK_PRESCALE	Sets the prescaler value for the reference clock.	0x0001
0x2100	TX_COMPONENT_ENABLE	Enable transmit multiplex signal components. Default has pilot and L-R enabled.	0x0003
0x2101	TX_AUDIO_DEVIATION	Configures audio frequency deviation level. Units are in 10 Hz increments. Default is 6825 (68.25 kHz).	0x1AA9
0x2102	TX_PILOT_DEVIATION	Configures pilot tone frequency deviation level. Units are in 10 Hz increments. Default is 675 (6.75 kHz)	0x02A3
0x2103	TX_RDS_DEVIATION	**Si4721 Only.** Configures the RDS/RBDS frequency deviation level. Units are in 10 Hz increments. Default is 2 kHz.	0x00C8
0x2104	TX_LINE_INPUT_LEVEL	Configures maximum analog line input level to the LIN/RIN pins to reach the maximum deviation level programmed into the audio deviation property TX Audio Deviation. Default is 636 mV_{PK}.	0x327C
0x2105	TX_LINE_INPUT_MUTE	Sets line input mute. L and R inputs may be independently muted. Default is not muted.	0x0000
0x2106	TX_PREEMPHASIS	Configures pre-emphasis time constant. Default is 0 (75 µS).	0x0000
0x2107	TX_PILOT_FREQUENCY	Configures the frequency of the stereo pilot. Default is 19000 Hz.	0x4A38
0x2200	TX_ACOMP_ENABLE	Enables audio dynamic range control and limiter. Default is 2 (limiter is enabled, audio dynamic range control is disabled).	0x0002
0x2201	TX_ACOMP_THRESHOLD	Sets the threshold level for audio dynamic range control. Default is –40 dB.	0xFFD8
0x2202	TX_ACOMP_ATTACK_TIME	Sets the attack time for audio dynamic range control. Default is 0 (0.5 ms).	0x0000

Table 21. Si472x Property Summary (Continued)

Prop	Name	Description	Default
0x2203	TX_ACOMP_RELEASE_TIME	Sets the release time for audio dynamic range control. Default is 4 (1000 ms).	0x0004
0x2204	TX_ACOMP_GAIN	Sets the gain for audio dynamic range control. Default is 15 dB.	0x000F
0x2205	TX_LIMITER_RELEASE_TIME	Sets the limiter release time. Default is 102 (5.01 ms)	0x0066
0x2300	TX_ASQ_INTERRUPT_SOURCE	Configures measurements related to signal quality metrics. Default is none selected.	0x0000
0x2301	TX_ASQ_LEVEL_LOW	Configures low audio input level detection threshold. This threshold can be used to detect silence on the incoming audio.	0x0000
0x2302	TX_ASQ_DURATION_LOW	Configures the duration which the input audio level must be below the low threshold in order to detect a low audio condition.	0x0000
0x2303	TX_ASQ_LEVEL_HIGH	Configures high audio input level detection threshold. This threshold can be used to detect activity on the incoming audio.	0x0000
0x2304	TX_ASQ_DURATION_HIGH	Configures the duration which the input audio level must be above the high threshold in order to detect a high audio condition.	0x0000
0x2C00	TX_RDS_INTERRUPT_SOURCE	**Si4721 Only.** Configure RDS interrupt sources. Default is none selected.	0x0000
0x2C01	TX_RDS_PI	**Si4721 Only.** Sets transmit RDS program identifier.	0x40A7
0x2C02	TX_RDS_PS_MIX	**Si4721 Only.** Configures mix of RDS PS Group with RDS Group Buffer.	0x0003
0x2C03	TX_RDS_PS_MISC	**Si4721 Only.** Miscellaneous bits to transmit along with RDS_PS Groups.	0x1008
0x2C04	TX_RDS_PS_REPEAT_COUNT	**Si4721 Only.** Number of times to repeat transmission of a PS message before transmitting the next PS message.	0x0003
0x2C05	TX_RDS_PS_MESSAGE_COUNT	**Si4721 Only.** Number of PS messages in use.	0x0001
0x2C06	TX_RDS_PS_AF	**Si4721 Only.** RDS Program Service Alternate Frequency. This provides the ability to inform the receiver of a single alternate frequency using AF Method A coding and is transmitted along with the RDS_PS Groups.	0xE0E0
0x2C07	TX_RDS_FIFO_SIZE	**Si4721 Only.** Number of blocks reserved for the FIFO. Note that the value written must be one larger than the desired FIFO size.	0x0000
Receive Properties			
0x0001	GPO_IEN	Enables interrupt sources.	0x0000
0x0102	DIGITAL_OUTPUT_FORMAT	Configure digital audio outputs (Si4721 only)	0x0000
0x0104	DIGITAL_OUTPUT_SAMPLE_RATE	Configure digital audio output sample rate (Si4721 only)	0x0000

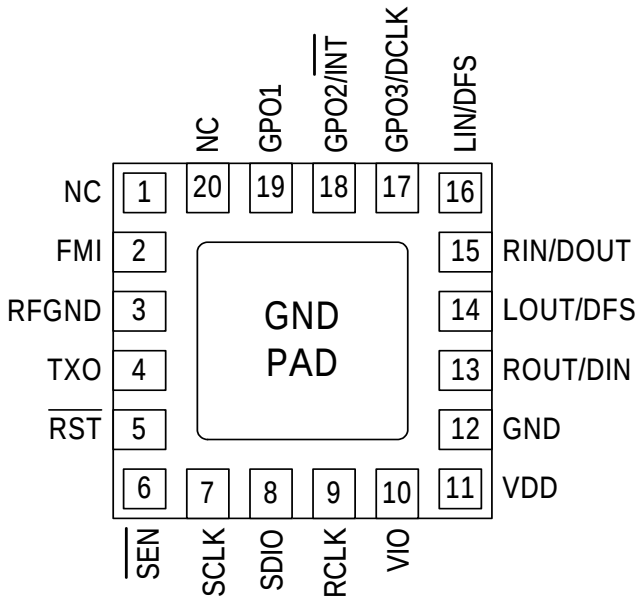
Table 21. Si472x Property Summary (Continued)

Prop	Name	Description	Default
0x0201	REFCLK_FREQ	Sets frequency of reference clock in Hz. The range is 31130 to 34406 Hz, or 0 to disable the AFC. Default is 32768 Hz.	0x8000
0x0202	REFCLK_PRESCALE	Sets the prescaler value for RCLK input.	0x0001
0x1100	FM_DEEMPHASIS	Sets deemphasis time constant. Default is 75 µs.	0x0002
0x1105	FM_BLEND_STEREO_THRESHOLD	Sets RSSI threshold for stereo blend (Full stereo above threshold, blend below threshold). To force stereo set this to 0. To force mono set this to 127. Default value is 49 dBµV.	0x0031
0x1106	FM_BLEND_MONO_THRESHOLD	Sets RSSI threshold for mono blend (Full mono below threshold, blend above threshold). To force stereo set this to 0. To force mono set this to 127. Default value is 30 dBµV.	0x001E
0x1107	FM_ANTENNA_INPUT	Selects the antenna type and the pin to which it is connected. (Si4721 only).	0x0000
0x1108	FM_MAX_TUNE_ERROR	Sets the maximum freq error allowed before setting the AFC rail (AFCRL) indicator. Default value is 30 kHz.	0x001E
0x1200	FM_RSQ_INT_SOURCE	Configures interrupt related to Received Signal Quality metrics.	0x0000
0x1201	FM_RSQ_SNR_HI_THRESHOLD	Sets high threshold for SNR interrupt.	0x007F
0x1202	FM_RSQ_SNR_LO_THRESHOLD	Sets low threshold for SNR interrupt.	0x0000
0x1203	FM_RSQ_RSSI_HI_THRESHOLD	Sets high threshold for RSSI interrupt.	0x007F
0x1204	FM_RSQ_RSSI_LO_THRESHOLD	Sets low threshold for RSSI interrupt.	0x0000
0x1207	FM_RSQ_BLEND_THRESHOLD	Sets the blend threshold for blend interrupt when boundary is crossed.	0x0081
0x1300	FM_SOFT_MUTE_RATE	Sets the attack and decay rates when entering and leaving soft mute.	0x0040
0x1302	FM_SOFT_MUTE_MAX_ATTENUATION	Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute. Default is 16 dB.	0x0010
0x1303	FM_SOFT_MUTE_SNR_THRESHOLD	Sets SNR threshold to engage soft mute. Default is 4 dB.	0x0004
0x1400	FM_SEEK_BAND_BOTTOM	Sets the bottom of the FM band for seek. Default is 8750 (87.5 MHz).	0x222E
0x1401	FM_SEEK_BAND_TOP	Sets the top of the FM band for seek. Default is 10790 (107.9 MHz).	0x2A26
0x1402	FM_SEEK_FREQ_SPACING	Selects frequency spacing for FM seek. Default value is 10 (100 kHz).	0x000A
0x1403	FM_SEEK_TUNE_SNR_THRESHOLD	Sets the SNR threshold for a valid FM Seek/Tune. Default value is 3 dB.	0x0003
0x1404	FM_SEEK_TUNE_RSSI_TRESHOLD	Sets the RSSI threshold for a valid FM Seek/Tune. Default value is 20 dBµV.	0x0014

Table 21. Si472x Property Summary (Continued)

Prop	Name	Description	Default
0x1500	RDS_INT_SOURCE	Configures RDS interrupt behavior (Si4721 only).	0x0000
0x1501	RDS_INT_FIFO_ COUNT	Sets the minimum number of RDS groups stored in the receive FIFO required before RDSRECV is set (Si4721 only).	0x0000
0x1502	RDS_CONFIG	Configures RDS setting (Si4721 only).	0x0000
0x4000	RX_VOLUME	Sets the output volume.	0x003F
0x4001	RX_HARD_MUTE	Mutes the audio output. L and R audio outputs may be muted independently.	0x0000

7. Pin Descriptions: Si4720/21-GM



Pin Number(s)	Name	Description
1, 20	NC	No connect. Leave floating.
2	FMI	FM RF input.
3	RFGND	RF ground. Connect to ground plane on PCB.
4	TXO	FM transmit output connection to transmit antenna.
5	RST	Device reset (active low) input.
6	SEN	Serial enable input (active low).
7	SCLK	Serial clock input.
8	SDIO	Serial data input/output.
9	RCLK	External reference oscillator input.
10	VIO	I/O supply voltage.
11	VDD	Supply voltage. May be connected directly to battery.
13	ROUT/DIN	Right audio line output—digital input data.
14	LOUT/DFS	Left audio line output—digital frame synchronization.
15	RIN/DOUT	Right audio line input—digital output data.
16	LIN/DFS	Left audio line input—digital frame synchronization.
17	GPO3/DCLK	General purpose output—digital bit synchronous clock.
18	GPO2/INT	General purpose output—interrupt request.
19	GPO1	General purpose output.
12, GND PAD	GND	Ground. Connect to ground plane on PCB.

8. Ordering Guide

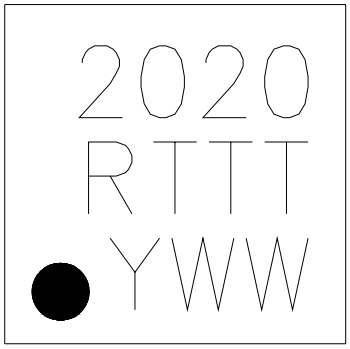
Part Number*	Description	Package Type	Operating Temperature
Si4720-B20-GM	Broadcast FM Radio Transceiver for Portable Applications	QFN Pb-free	–20 to 85 °C
Si4721-B20-GM	Broadcast FM Radio Transceiver for Portable Applications with RDS/RBDS Encoder/Decoder	QFN Pb-free	–20 to 85 °C
***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel.			

9. Package Markings (Top Marks)

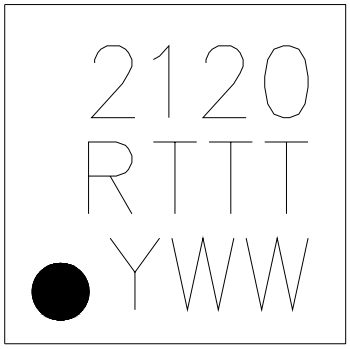
9.1. Top Mark Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	20 = Si4720; 21 = Si4721
	Firmware Revision	20 = Firmware Revision 2.0
Line 2 Marking:	Die Revision	B = Revision B Die
	TTT = Internal Code	Internal tracking code.
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier
	Y = Year WW = 'Workweek	Assigned by the Assembly House. Corresponds to the last significant digit of the year and workweek of the mold date.

9.2. Si4720/21 Top Mark



9.3. Si4721 Top Mark



10. Package Outline: Si4720/21-GM

Figure 26 illustrates the package details for the Si4720. Table 22 lists the values for the dimensions shown in the illustration.

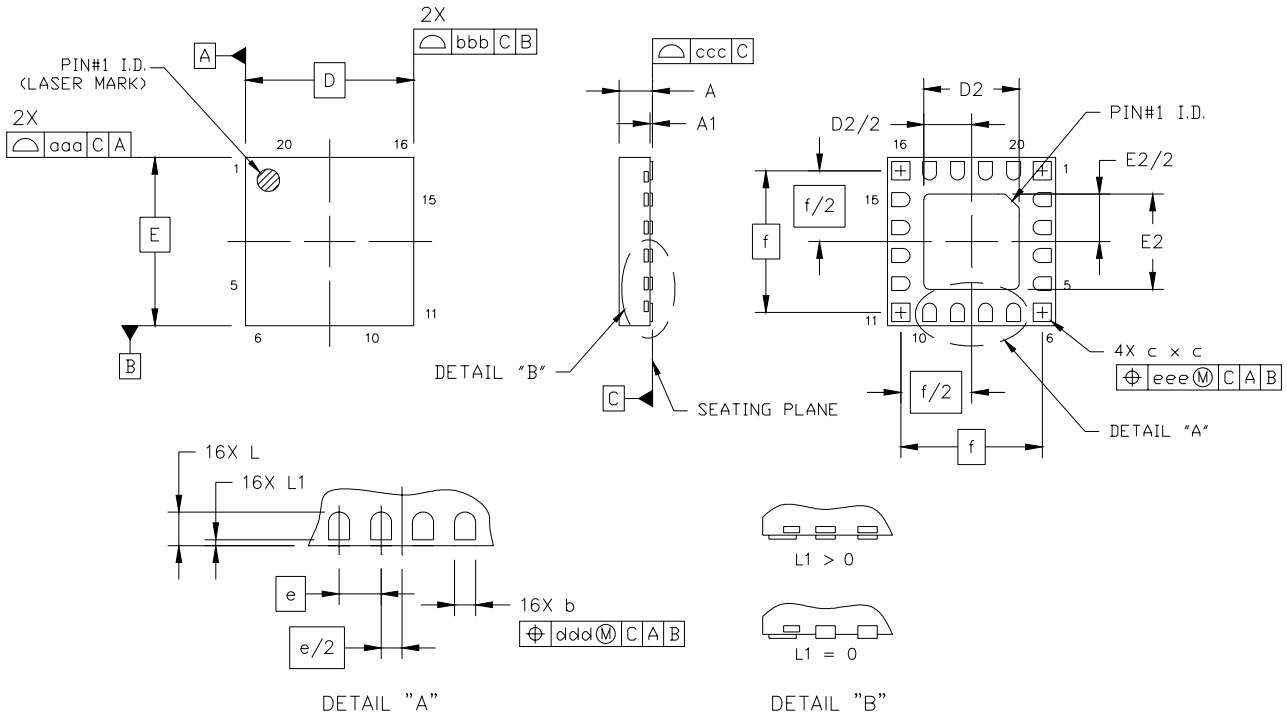


Figure 26. 20-Pin Quad Flat No-Lead (QFN)

Table 22. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.27	0.32	0.37
D		3.00 BSC	
D2	1.65	1.70	1.75
e		0.50 BSC	
E		3.00 BSC	
E2	1.65	1.70	1.75

Symbol	Millimeters		
	Min	Nom	Max
f		2.53 BSC	
L	0.35	0.40	0.45
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

11. PCB Land Pattern: Si4720/21-GM

Figure 27 illustrates the PCB land pattern details for the Si4720-GM. Table 23 lists the values for the dimensions shown in the illustration.

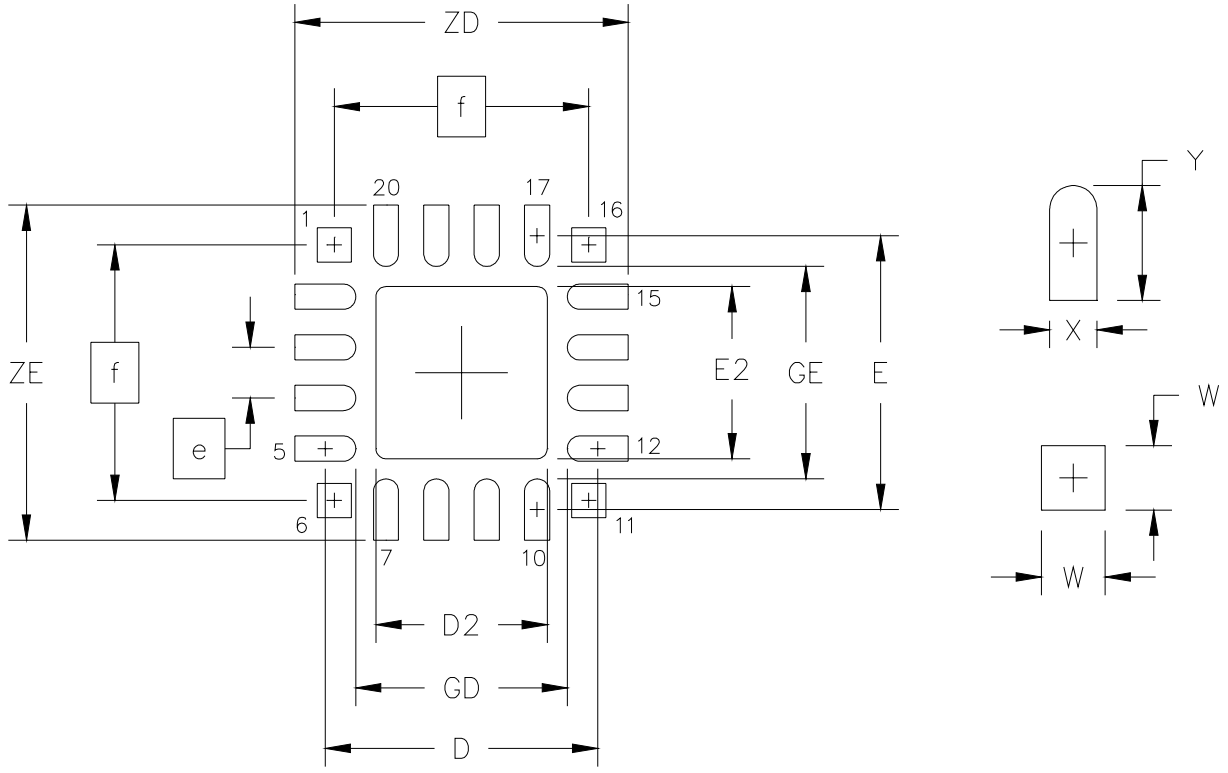


Figure 27. PCB Land Pattern

Table 23. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 BSC	
GD	2.10	—

Symbol	Millimeters	
	Min	Max
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing is per the ANSI Y14.5M-1994 specification.
3. This land pattern design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm.

Note: Solder Mask Design

1. All metal pads are to be non-solder-mask-defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component standoff.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for small body components.

12. Additional Reference Resources

- Si47xx Evaluation Board User's Guide
- AN307: Si4712/13/20/21 Receive Power Scan
- AN332: Universal Programming Guide
- AN341: Si4720/21 Evalution Board Quick Start Guide
- AN383: Universal Antenna Selection and Layout Guidelines
- AN388: Universal Evaluation Board Test Procedure
- Si4720/21 Customer Support Site: www.mysilabs.com
  This site contains all application notes, evaluation board schematics and layouts, and evaluation software. NDA is required for access. To request access, send mysilabs user name and request for access to fminfo@silabs.com.

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