

Digital servo controller for VCRs

BU2880 series

The BU2880 series are linear digital-servo controllers that allow construction of a VCR servo system using one IC. The DRUM and CAPSTAN systems have digital filters, and the IC is compatible with VISS / VASS overwriting and wide-aspect operation.

●Applications

Video cassette recorders

●Features

- 1) All VCR servo functions on a single chip.
- 2) Digital filters in the DRUM and CAPSTAN speed and phase systems.
- 3) Built-in CTL amplifier with serial gain setting.
- 4) VISS / VASS overwriting and INDEX detection functions for wide-aspect operation.
- 5) DRUM f_H compensation calculation function from speed detect function.
- 6) 6.5H discrimination.
- 7) Compatible with 19 μ m heads.

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{DD}	7.0	V
Power dissipation	P _d	500*	mW
Operating temperature	T _{opr}	– 15 ~ + 70	°C
Storage temperature	T _{stg}	– 55 ~ + 125	°C

* Reduced by 5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V _{DD}	4.5	5.0	5.5	V

The diagram illustrates the internal architecture of the TMS320C24 DSP, organized around a central 24-pin package. The pins and their functions are as follows:

- Pin 1 (SDATA):** Connected to the SIDATA DET block.
- Pin 2 (VSYNCIN):** Connected to the SYNC SEP block, which outputs VD.
- Pin 3 (FSCIN):** Connected to the PWMGEN block, which outputs FSC BIT PAT.
- Pin 4 (CFGOUT):** Connected to the ROMDATA block.
- Pin 5 (CTLOUT1):** Connected to the SAMPLE block.
- Pin 6 (CTLOUT2):** Connected to the REF COUNTER and DRUM TRAPE block.
- Pin 7 (DRUMPFV):** Connected to the DIGITAL FILTER + MIX block.
- Pin 8 (CAPPFV):** Connected to the DIGITAL FILTER + MIX block.
- Pin 9 (VDD):** Connected to the ROM and CAPFV block.
- Pin 10 (CTLAMP-OUT):** Connected to the CTLAMP- pin.
- Pin 11 (CTLAMP-):** Connected to the CTLAMP- pin.
- Pin 12 (CTLAMP+):** Connected to the CTLAMP+ pin.
- Pin 13 (RECCTL-):** Connected to the RECCTL- pin.
- Pin 14 (RECCTL+):** Connected to the RECCTL+ pin.
- Pin 15 (CTLCOMPIN):** Connected to the CTLCOMPIN pin.
- Pin 16 (VSS):** Connected to the VSS pin.
- Pin 17 (CFGIN):** Connected to the CFG COUNT block.
- Pin 18 (VPDL):** Connected to the VP DELAY block.
- Pin 19 (VHPULSE):** Connected to the VP WIDTH block.
- Pin 20 (AHSW):** Connected to the AHSWON block.
- Pin 21 (DPGIN):** Connected to the DPGIN pin.
- Pin 22 (DFGIN):** Connected to the DFGIN pin.
- Pin 23 (CTLDUTY):** Connected to the CTLDUTY pin.
- Pin 24 (VHSW):** Connected to the VHSW pin.

The internal blocks include:

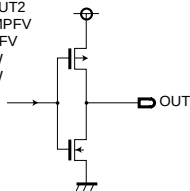
- ROMDATA:** Receives data from the ROM and provides it to the REF COUNTER and DRUM TRAPE block.
- REF COUNTER and DRUM TRAPE:** Processes the REF COUNTER and DRUM TRAPE signals.
- DIGITAL FILTER + MIX:** Processes the DRUMPFV and CAPPFV signals.
- ROM and CAPFV:** Provides data to the DIGITAL FILTER + MIX block.
- CTLAMP- and CTLAMP+:** Control lamp signals.
- RECCTL- and RECCTL+:** Record control signals.
- CTLCOMPIN:** Control lamp comparison input.
- CFG COUNT:** Configuration count block.
- VP DELAY:** Variable pulse delay block.
- VP WIDTH:** Variable pulse width block.
- AHSWON:** Audio high-speed window block.
- DPGIN:** Digital pulse generator input.
- DFGIN:** Digital filter generator input.
- CTLDUTY:** Control lamp duty block.
- VHSW:** Variable high-speed window block.

● Pin descriptions

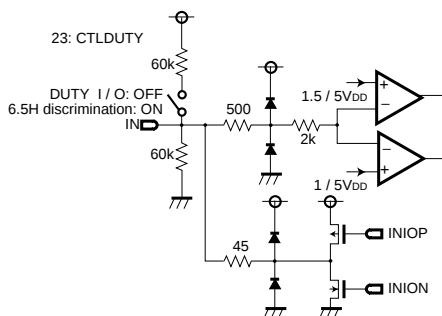
Pin No.	Pin name	Function
1	SDATA	Serial data input (tri-state)
2	VSIN	Composite sync input
3	FSCIN	System clock input
4	CFGOUT	CFG divider output
5	CTLOUT1	CTL comparator output
6	CTLOUT2	CTL divider output
7	DRUMPFV	DRUM control output (digital filter output)
8	CAPPFV	CAPSTAN control output (digital filter output)
9	V _{DD}	Power supply
10	CTLAMP _{OUT}	CTLAMP output
11	CTLAMP ⁻	CTLAMP – input
12	CTLAMP ⁺	CTLAMP + input
13	RECCTL ⁻	Recording CTL – output
14	RECCTL ⁺	Recording CTL + output
15	CTLCOMPIN	CTL comparator input
16	VSS	GND
17	CFGIN	CFG input
18	VPDLY	Quasi-VH pulse delay amount control input
19	VHPULSE	Quasi-VH pulse output
20	AHSW	Head switch audio output
21	DPGIN	DRUM PG input
22	DFGIN	DRUM FG input
23	CTLDUTY	Duty discrimination, VISS discrimination, 6.5H discrimination output / VASS duty control input
24	VHSW	HEAD SW video output

● Input / output circuits

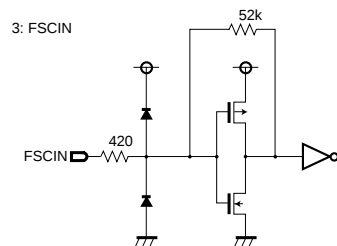
4: CFGOUT
5: CTLOUT1
6: CTLOUT2
7: DRUMPFV
8: CAPPFV
20: AHSW
24: VHSW



Logic output

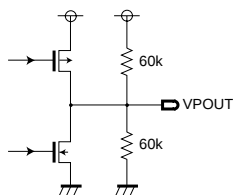


Shared input / output terminal

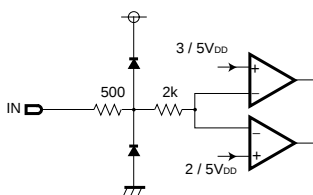


FSC input

19: VHPULSE

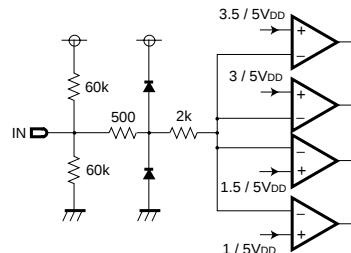


Tri-state output

2: VSYNCIN
18: VPDLY

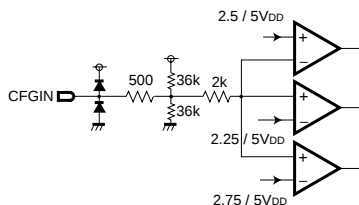
Two-value input

1: SDATA



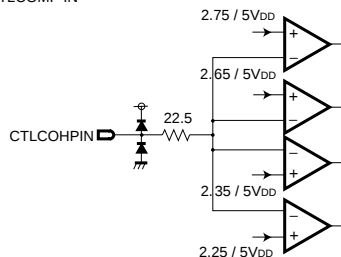
Three-value input

17: CFGIN

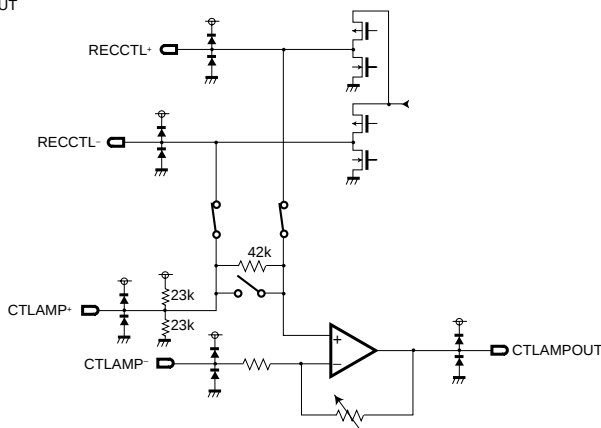


CFG input (zero cross comparator)

15: CTLCOMP IN

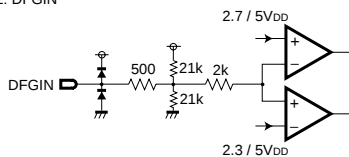


CTL comparator input

10: CTLAMP-OUT
11: CTLAMP-
12: CTLAMP+
13: RECCTL-
14: RECCTL+

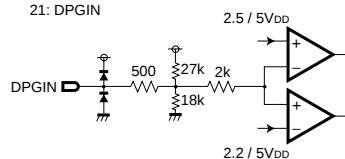
CTLAMP

22: DFGIN



DFG input

21: DPGIN



DPG input

●Electrical characteristics (unless otherwise noted, Ta = 25°C and V_{DD} = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply current	I _{DD}	—	27	38	mA	
Power on reset threshold	V _{PON}	1.0	1.5	2.0	V	
Two-value output high level voltage	V _H	4.0	4.5	—	V	I _{LOAD} = 1.5mA
Two-value output low level voltage	V _L	—	0.4	1.0	V	I _{LOAD} = 1.5mA
Two-value input threshold	V _{TH}	2.5	3.0	3.5	V	Schmitt level + 0V, – 1.0V
Two-value input current	I _{LIN}	—	0	1	μA	V _{IN} = V _{DD} , GND
Pullup input current	I _{PU}	59	83	116	μA	V _N = GND
CFG input current	I _{CFG}	100	140	196	μA	V _N = V _{DD} , GND
Three-value output high voltage	V _{H3}	4.0	4.5	—	V	I _{LOAD} = 1.5mA
Three-value output low voltage	V _{L3}	—	0.4	1.0	V	I _{LOAD} = 1.5mA
Three-value output mid voltage	V _{M3}	2.0	2.5	3.0	V	
Three-value input "H" threshold	V _{TINH}	3.10	3.50	4.00	V	Schmitt level + 0V, – 0.5V
Three-value input "L" threshold	V _{TINL}	1.00	1.50	1.90	V	Schmitt level + 0V, – 0.5V
Three-value input current (±)	I _{TIN}	59	83	116	μA	V _{IN} = V _{DD} , GND
FSC operating input level	V _{RCK}	0.2	—	4.0	V _{P-P}	AC coupled, duty: 40 to 60%, C = 1000pF
FSC input current (±)	I _{FSCIN}	61	85	119	μA	V _{IN} = V _{DD} , GND
RECCTL output high level voltage	V _{RCTH}	4.00	4.56	—	V	I _{LOAD} = 2.0mA
RECCTL output low level voltage	V _{RCTL}	—	0.16	0.60	V	I _{LOAD} = 2.0mA
〈CTLAMP〉						
Output high level voltage	V _{OH}	3.8	4.3	—	V	I _{LOAD} = 1.0mA
Output low level voltage	V _{OL}	—	0.2	0.5	V	I _{LOAD} = 1.0mA
CTLAMP comparator level	V _{CTLI}	200	250	300	mV	With respect to bias
CTLAMP comparator width	V _{CO}	75	100	125	mV	—
CTLAMP bias level	V _{BI}	2.4	2.5	2.6	V	—

○Not designed for radiation resistance.

● Measurement circuit

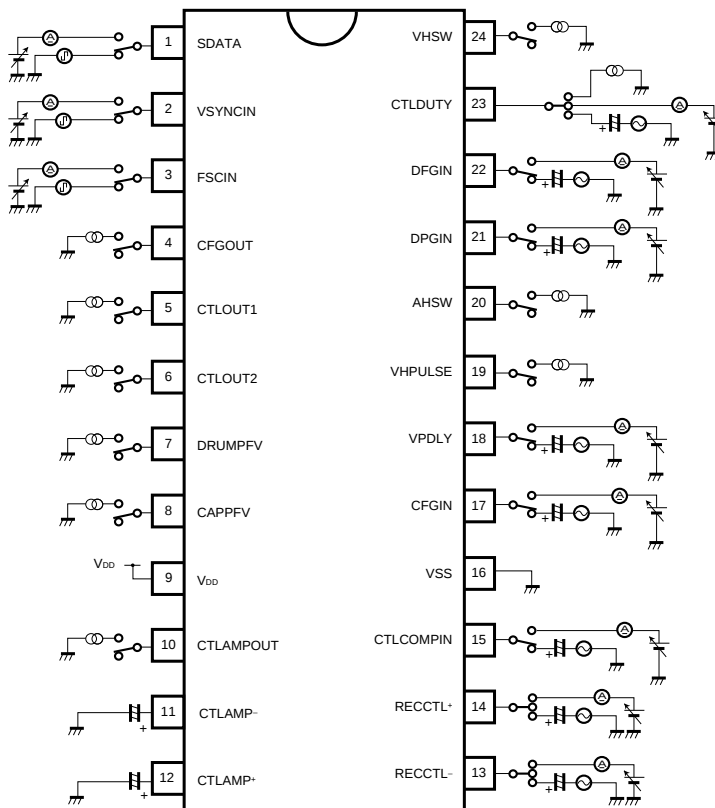


Fig.1

● Electrical characteristic curves

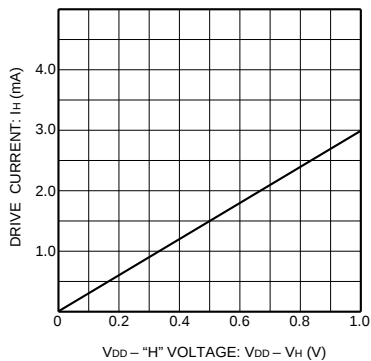


Fig. 2 Two-value output high level voltage vs. drive current characteristics

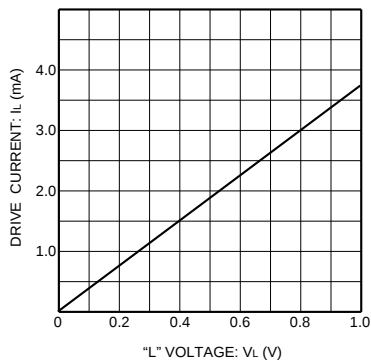


Fig. 3 Two-value output low level voltage vs. drive current characteristics

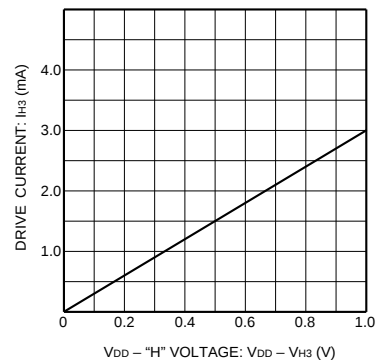


Fig. 4 Three-value output high level voltage vs. drive current characteristics

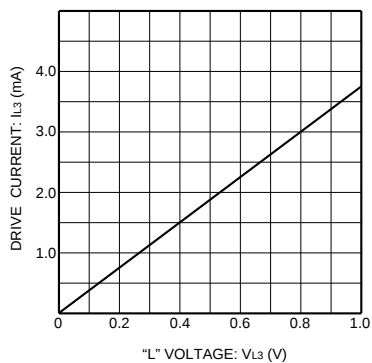


Fig. 5 Three-value output low level voltage vs. drive current characteristics

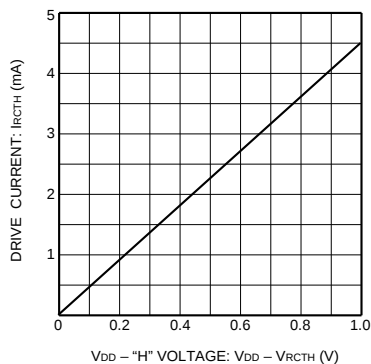


Fig. 6 RECCTL output high level voltage vs. drive current characteristics

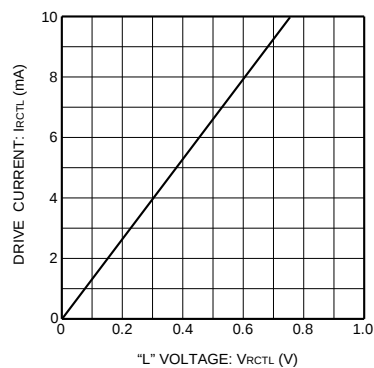


Fig. 7 RECCTL output low level voltage vs. drive current characteristics

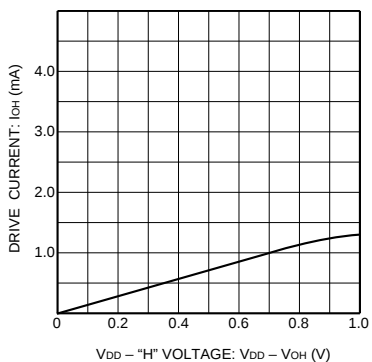


Fig. 8 CTLAMP output high level voltage vs. drive characteristics

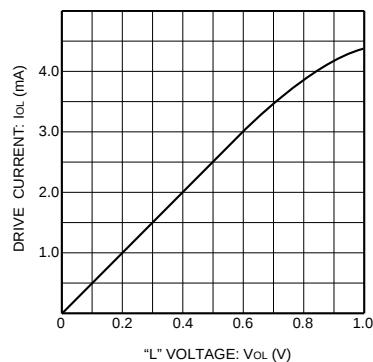


Fig. 9 CTLAMP output low level voltage vs. drive current characteristics

● External dimensions (Units: mm)

