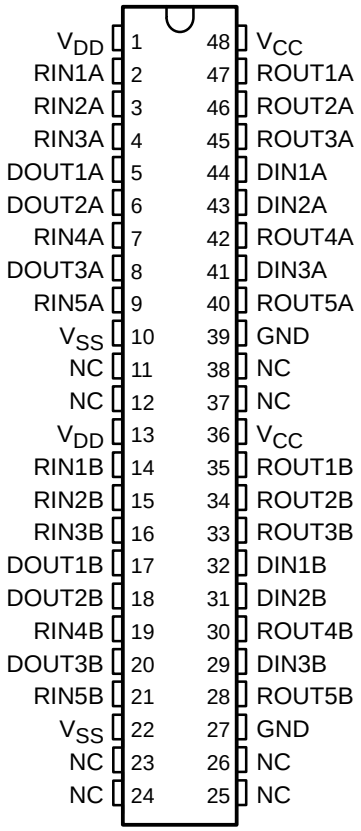
- **Single Chip With Easy Interface Between UART and Two Serial-Port Connectors of IBM™ PC/AT™ and Compatibles**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU Recommendation V.28**
- **Supports Data Rates up to 120 kbit/s**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Shrink Small-Outline (DL) Packages**

**DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The SN752232 consists of dual ports, each containing three drivers and five receivers, which reduce board space and allow easy interconnection of the UART and two serial-port connectors of an IBM™ PC/AT™ and compatibles. The bipolar circuits and processing of this ‘‘dual GD75232” provide, a rugged, low-cost solution for this function.

The SN752232 complies with the requirements of the TIA/EIA-232-F and ITU V.28 standards. These standards are for data interchange between a host computer and a peripheral at signaling rates up to 20 kbit/s. The device supports data rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be expected unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates up to 120 kbit/s, use of TIA/EIA-423-B (ITU V.10) and TIA/EIA-422-B (ITU V.11) standards is recommended.

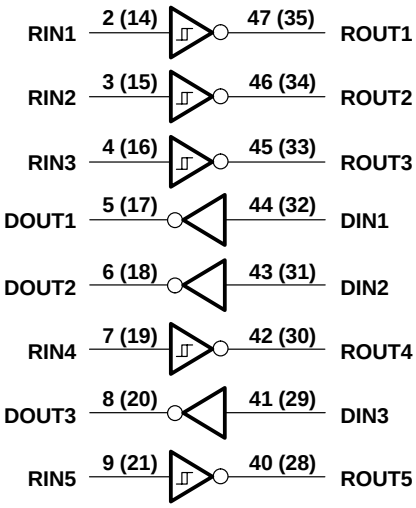
The SN752232 is characterized for operation over the temperature range of 0°C to 70°C.

**AVAILABLE OPTIONS**

| $T_A$ | PACKAGED DEVICES | |
|---|---|---|
| | PLASTIC SHRINK SMALL OUTLINE (DL) | PLASTIC THIN SHRINK SMALL OUTLINE (DGG) |
| 0°C to 70°C | SN752232DL | SN752232DGG |

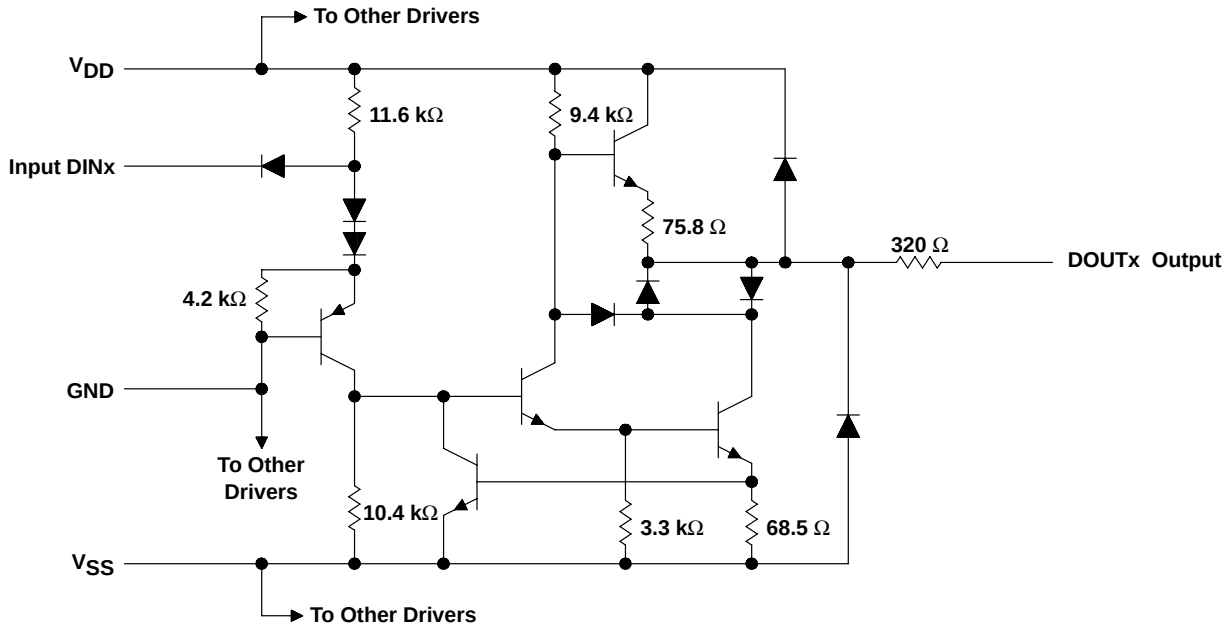
The DL package also is available taped and reeled. Add the suffix R to the device type (e.g., SN752232DLR). The DGG package is only available taped and reeled.

## logic diagram (positive logic)



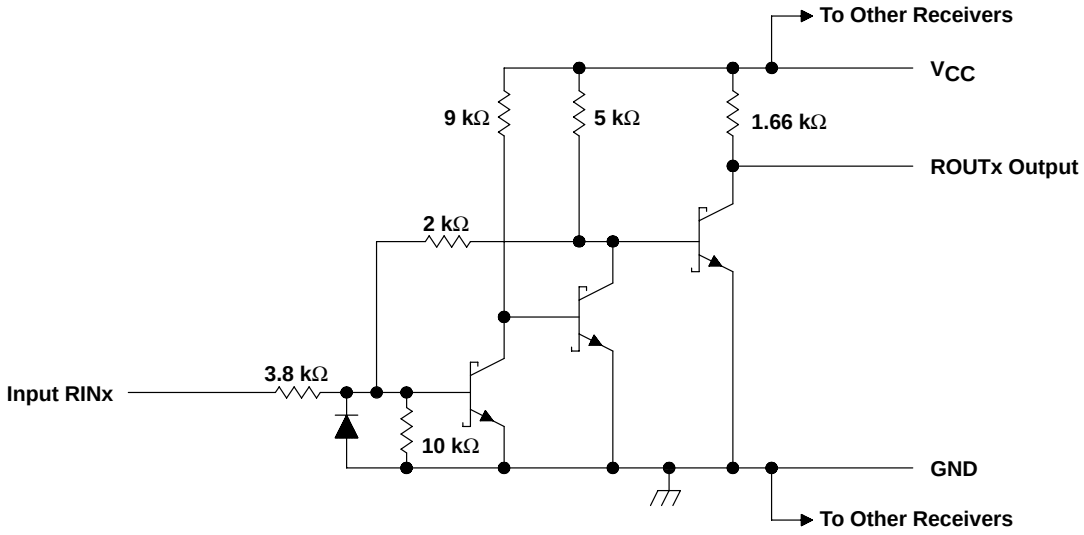

NOTE A: Numbers in parentheses are for B section.

## schematic (each driver)




NOTE A: Resistor values shown are nominal.

## schematic (each receiver)




NOTE A: Resistor values shown are nominal.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage (see Note 1): $V_{CC}$ | 10 V |
| $V_{DD}$ | 15 V |
| $V_{SS}$ | –15 V |
| Input voltage range, $V_I$: Driver | –15 V to 7 V |
| Receiver | –30 V to 30 V |
| Driver output voltage range, $V_O$ | –15 V to 15 V |
| Receiver low-level output current, $I_{OL}$ | 20 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package | 70°C/W |
| DL package | 63°C/W |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 7.5 | 9 | 15 | V |
| $V_{SS}$ | Supply voltage | | –7.5 | –9 | –15 | V |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage (driver only) | | 1.9 | | | V |
| $V_{IL}$ | Low-level input voltage (driver only) | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | Driver | | | –6 | mA |
| | | Receiver | | | –0.5 | |
| $I_{OL}$ | Low-level output current | Driver | | | 6 | mA |
| | | Receiver | | | 16 | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

## supply currents over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current from $V_{DD}$ | All inputs at 1.9 V, | No load | $V_{DD}$ = 9 V, $V_{SS}$ = –9 V | | 30 | mA |
| | | | | $V_{DD}$ = 12 V, $V_{SS}$ = –12 V | | 38 | |
| | | | | $V_{DD}$ = 15 V, $V_{SS}$ = –15 V | | 50 | |
| | | All inputs at 0.8 V, | No load | $V_{DD}$ = 9 V, $V_{SS}$ = –9 V | | 9 | |
| | | | | $V_{DD}$ = 12 V, $V_{SS}$ = –12 V | | 11 | |
| | | | | $V_{DD}$ = 15 V, $V_{SS}$ = –15 V | | 18 | |
| $I_{SS}$ | Supply current from $V_{SS}$ | All inputs at 1.9 V, | No load | $V_{DD}$ = 9 V, $V_{SS}$ = –9 V | | –30 | mA |
| | | | | $V_{DD}$ = 12 V, $V_{SS}$ = –12 V | | –38 | |
| | | | | $V_{DD}$ = 15 V, $V_{SS}$ = –15 V | | –50 | |
| | | All inputs at 0.8 V, | No load | $V_{DD}$ = 9 V, $V_{SS}$ = –9 V | | –6.4 | |
| | | | | $V_{DD}$ = 12 V, $V_{SS}$ = –12 V | | –6.4 | |
| | | | | $V_{DD}$ = 15 V, $V_{SS}$ = –15 V | | –6.4 | |
| $I_{CC}$ | Supply current from $V_{CC}$ | $V_{CC}$ = 5 V, | All inputs at 5 V, | No load | | 60 | mA |

## DRIVER SECTION

## electrical characteristics over recommended operating free-air temperature range, $V_{DD}$ = 9 V, $V_{SS}$ = –9 V, $V_{CC}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_{IL}$ = 0.8 V, | $R_L$ = 3 kΩ, | See Figure 1 | 6 | 7.5 | | V |
| $V_{OL}$ | Low-level output voltage (see Note 3) | $V_{IH}$ = 1.9 V, | $R_L$ = 3 kΩ, | See Figure 1 | | –7.5 | –6 | V |
| $I_{IH}$ | High-level input current | $V_I$ = 5 V, | See Figure 2 | | | | 10 | μA |
| $I_{IL}$ | Low-level input current | $V_I$ = 0, | See Figure 2 | | | | –1.6 | mA |
| $I_{OS(H)}$ | High-level short-circuit output current (see Note 4) | $V_{IL}$ = 0.8 V, | $V_O$ = 0, | See Figure 1 | –4.5 | –12 | –19.5 | mA |
| $I_{OS(L)}$ | Low-level short-circuit output current | $V_{IH}$ = 2 V, | $V_O$ = 0, | See Figure 1 | 4.5 | 12 | 19.5 | mA |
| $r_O$ | Output resistance (see Note 5) | $V_{CC}$ = $V_{DD}$ = $V_{SS}$ = 0, | | $V_O$ = –2 V to 2 V | 300 | | | Ω |

NOTES: 3. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if –10 V is maximum, the typical value is a more negative voltage).
4. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
5. Test conditions are those specified by TIA/EIA-232-F and as listed above.

### switching characteristics, $V_{CC}$ = 5 V, $V_{DD}$ = 12 V, $V_{SS}$ = –12 V, $T_A$ = 25°C (see Figure 3)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $R_L$ = 3 kΩ to 7 kΩ, | $C_L$ = 15 pF | | 315 | 500 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | $R_L$ = 3 kΩ to 7 kΩ, | $C_L$ = 15 pF | | 75 | 175 | ns |
| $t_{TLH}$ | Transition time, low- to high-level output | $R_L$ = 3 kΩ to 7 kΩ | $C_L$ = 15 pF | | 60 | 100 | ns |
| | | | $C_L$ = 2500 pF, See Note 6 | | 1.7 | 2.5 | µs |
| $t_{THL}$ | Transition time, high- to low-level output | $R_L$ = 3 kΩ to 7 kΩ | $C_L$ = 15 pF | | 40 | 75 | ns |
| | | | $C_L$ = 2500 pF, See Note 6 | | 1.5 | 2.5 | µs |

NOTE 6: Measured between ±3-V and ±3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied either high or low.

## RECEIVER SECTION

### electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | $T_A$ = 25°C | See Figure 5 | 1.75 | 1.9 | 2.3 | V |
| | | $T_A$ = 0°C to 70 °C | | 1.55 | | 2.3 | |
| $V_{IT–}$ | Negative-going input threshold voltage | | | 0.75 | 0.97 | 1.25 | V |
| $V_{hys}$ | Input hysteresis voltage ($V_{IT+} – V_{IT–}$) | | | 0.5 | | | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –0.5 mA | $V_{IH}$ = 0.75 V | 2.6 | 4 | 5 | V |
| | | | Inputs open | 2.6 | | | |
| $V_{OL}$ | Low-level input voltage | $I_{OL}$ = 10 mA, | $V_I$ = 3 V | | 0.2 | 0.45 | V |
| $I_{IH}$ | High-level input current | $V_I$ = 25 V, | See Figure 5 | 3.6 | | 8.8 | mA |
| | | $V_I$ = 3 V, | See Figure 5 | 0.43 | | | |
| $I_{IL}$ | Low-level output current | $V_I$ = –25 V, | See Figure 5 | –3.6 | | –8.8 | mA |
| | | $V_I$ = –3 V, | See Figure 5 | –0.43 | | | |
| $I_{OS}$ | Short-circuit output current | See Figure 4 | | | –3.4 | –12 | mA |

† All typical values are at $T_A$ = 25°C, $V_{CC}$ = 5 V, $V_{DD}$ = 9 V, and $V_{SS}$ = –9 V.

### switching characteristics, $V_{CC}$ = 5 V, $V_{DD}$ = 12 V, $V_{SS}$ = –12 V, $T_A$ = 25°C (see Figure 6)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $C_L$ = 50 pF, | $R_L$ = 5 kΩ | | 107 | 250 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | | | | 42 | 150 | ns |
| $t_{TLH}$ | Transition time, low- to high-level output | | | | 175 | 350 | ns |
| $t_{THL}$ | Transition time, high- to low-level output | | | | 16 | 60 | ns |
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $C_L$ = 15 pF, | $R_L$ = 1.5 kΩ | | 100 | 160 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | | | | 60 | 100 | ns |
| $t_{TLH}$ | Transition time, low- to high-level output | | | | 90 | 175 | ns |
| $t_{THL}$ | Transition time, high- to low-level output | | | | 15 | 50 | ns |

## PARAMETER MEASUREMENT INFORMATION

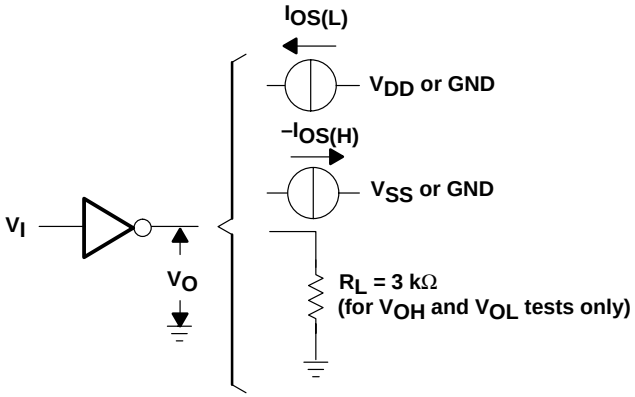



**Figure 1. Driver Test Circuit for $V_{OH}$, $V_{OL}$, $I_{OS(H)}$, and $I_{OS(L)}$**

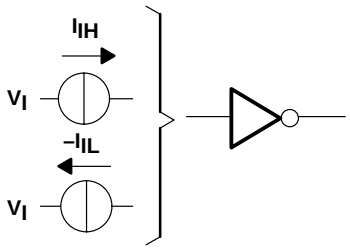
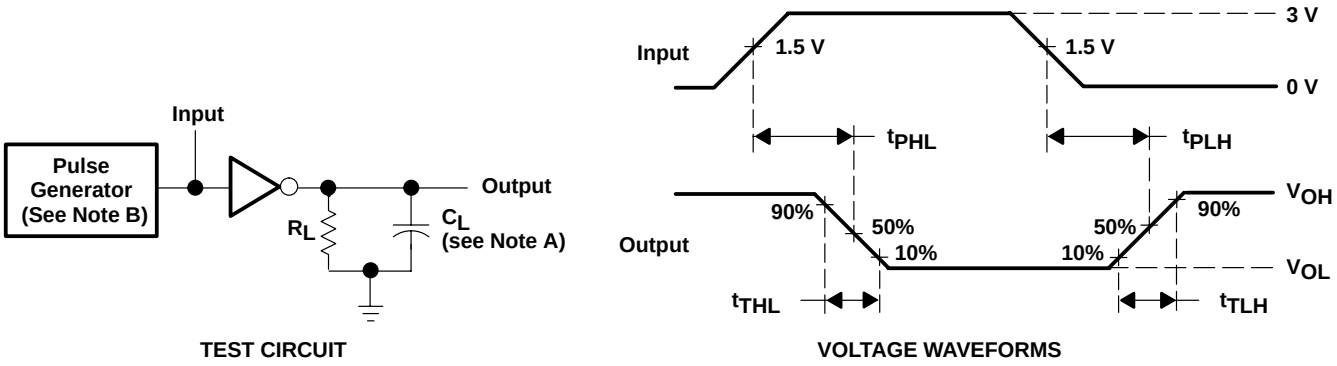



**Figure 2. Driver Test Circuit for $I_{IH}$ and $I_{IL}$**




NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $t_W$ = 25 µs, PRR = 20 kHz, $Z_O$ = 50 Ω, $t_r = t_f$ < 50 ns.

**Figure 3. Driver Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION

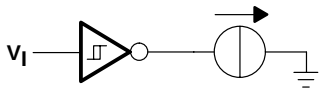



**Figure 4. Receiver Test Circuit for $I_{OS}$**

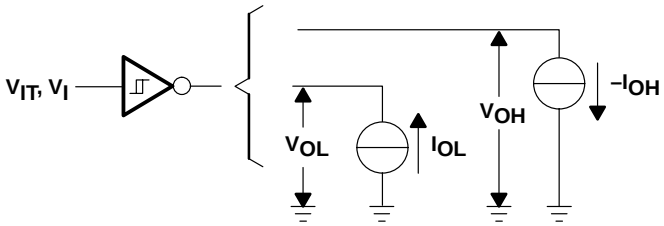
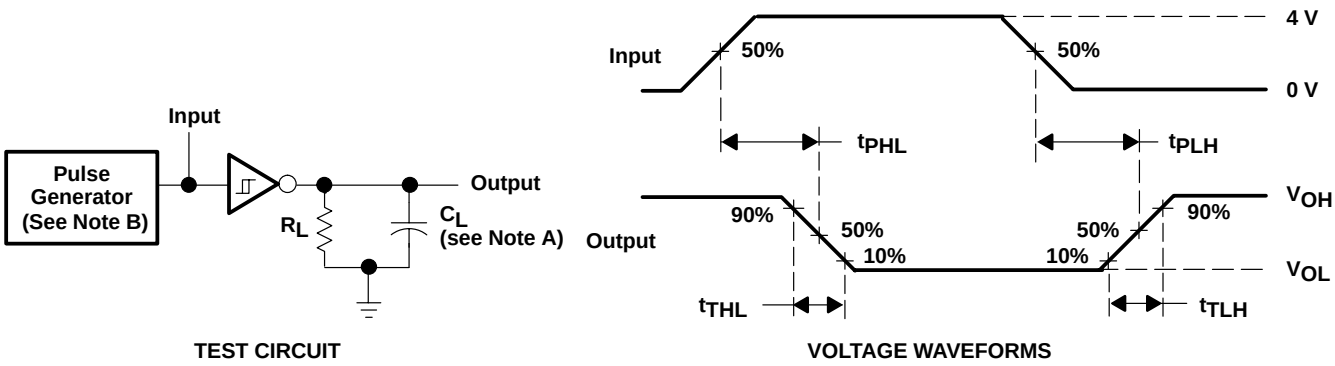



**Figure 5. Receiver Test Circuit for $V_{IT}$, $V_{OH}$, and $V_{OL}$**




NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $t_W$ = 25 µs, PRR = 20 kHz, $Z_O$ = 50 Ω, $t_r = t_f$ < 50 ns.

**Figure 6. Receiver Propagation and Transition Times**

## TYPICAL CHARACTERISTICS

## DRIVER SECTION

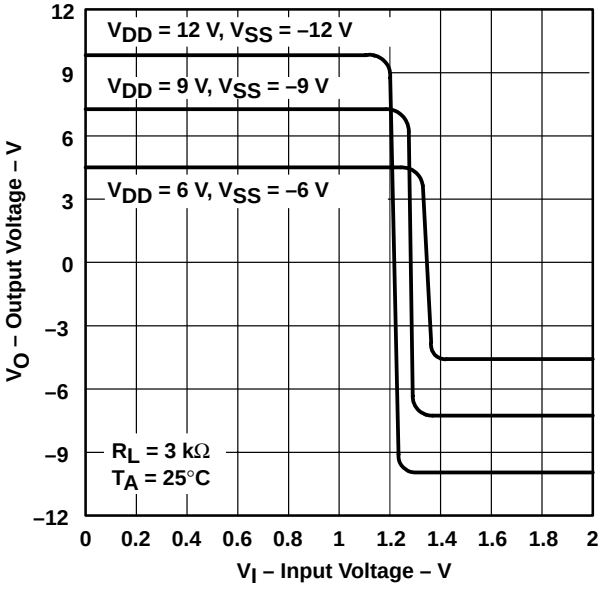



Figure 7

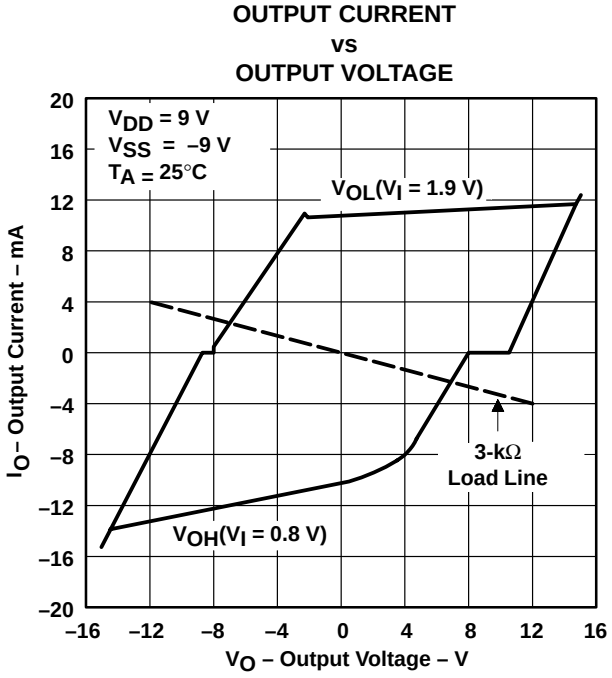



Figure 8

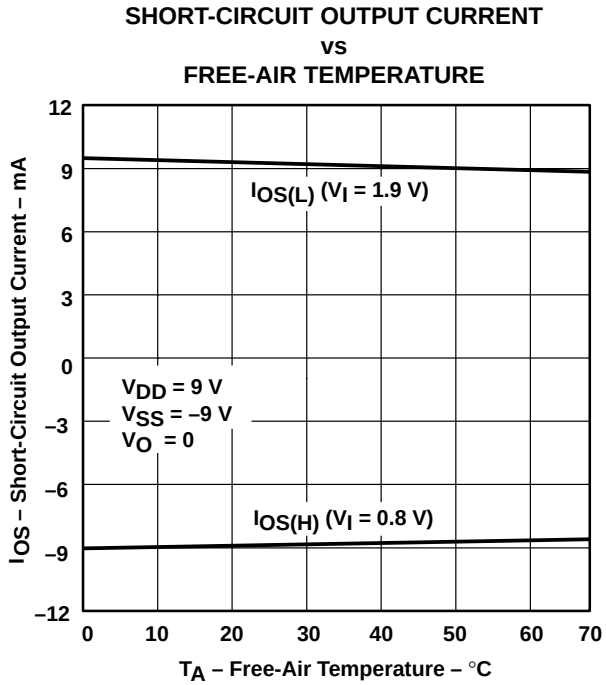



Figure 9

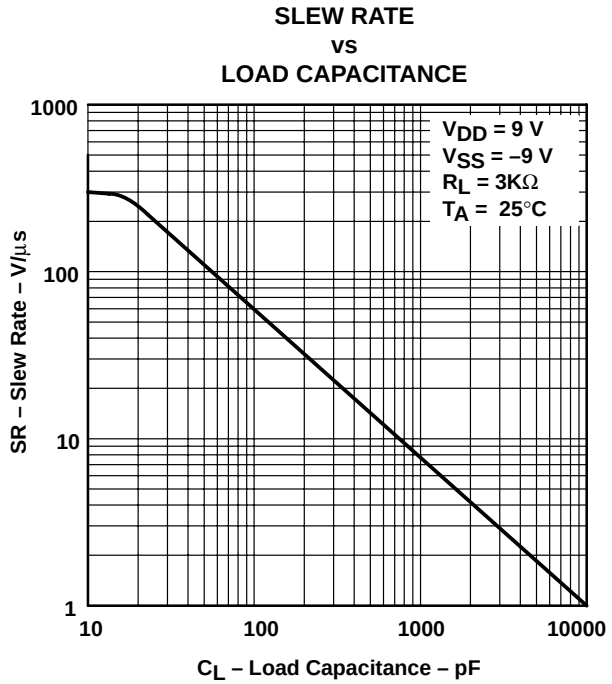



Figure 10

## TYPICAL CHARACTERISTICS

**INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE**

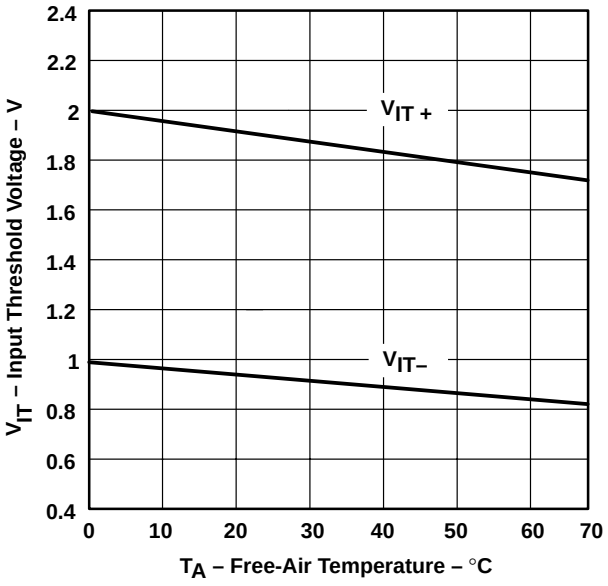



**Figure 11**

**INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE**

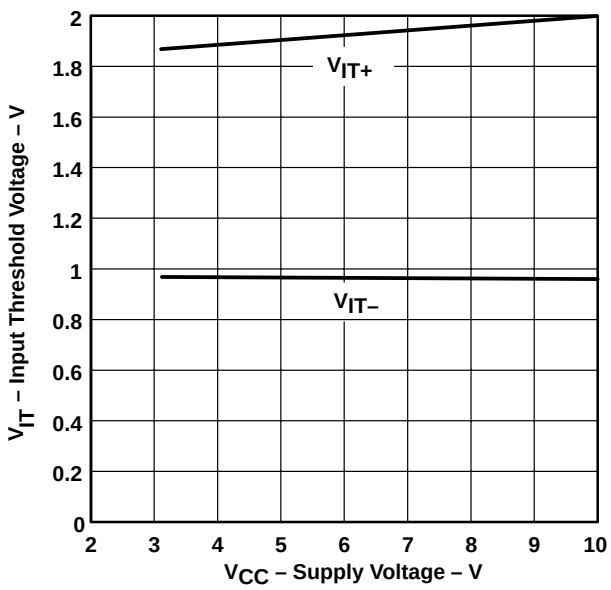
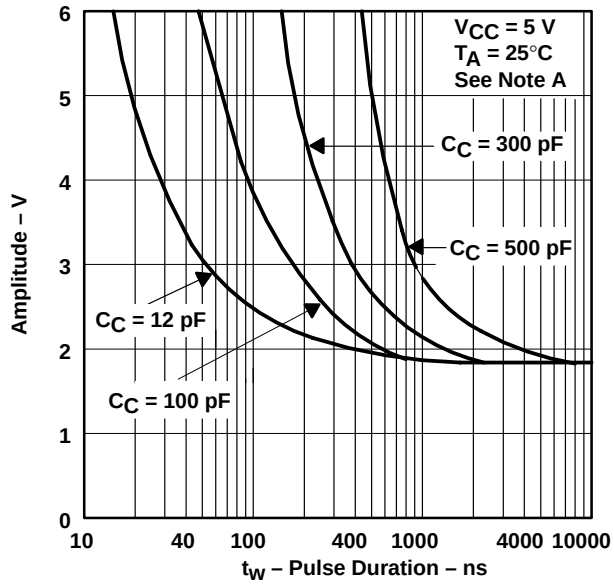



**Figure 12**

**NOISE REJECTION**




NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, does not cause a change of the output level.

**Figure 13**

**MAXIMUM SUPPLY VOLTAGE vs FREE-AIR TEMPERATURE**

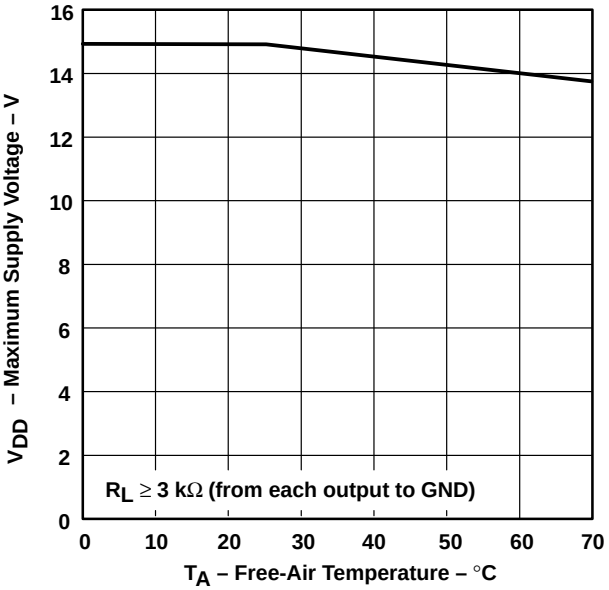



**Figure 14**

## APPLICATION INFORMATION

Diodes placed in series with the $V_{DD}$ and $V_{SS}$ leads protect the SN752232 in the fault condition in which the device outputs are shorted to ±15 V, and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

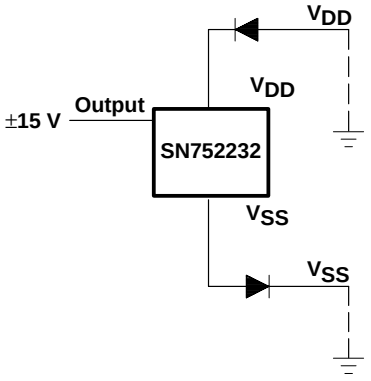
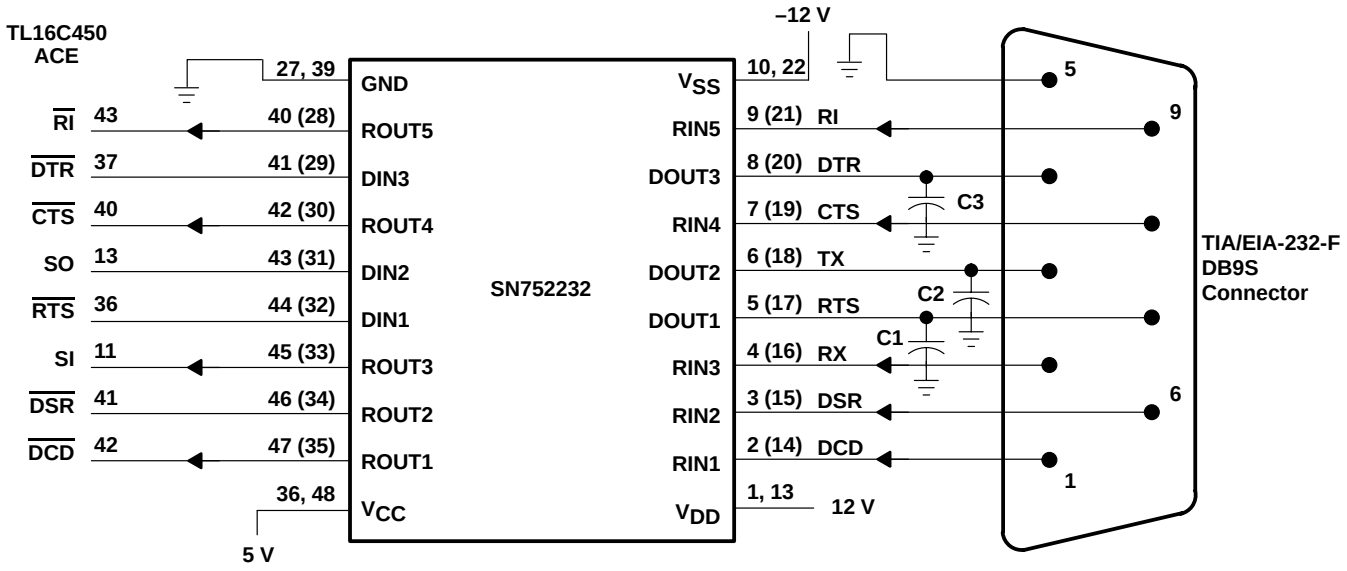



**Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F**




NOTE A: Numbers in parentheses are for B section.

**Figure 16. Typical Connection Per Port**

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