National Semiconductor Corporation

PRELIMINARY

DM54ALS190/DM74ALS190/DM54ALS191/DM74ALS191 Synchronous 4-Bit Up/Down Decade and Binary Counter

General Description

The 'ALS190 and 'ALS191 are synchronous, reversible up/down counters. The 'ALS190 is a 4-bit decade counter and the 'ALS191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high level transition of the clock input if the enable input (G) is low. A high at G inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs (G and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable set-up and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The CLK, D/$\overline{U}$, and LOAD inputs are buffered to lower the drive requirement, which significantly reduces the loading on, or current required by, clock drivers, etc., for long parallel words.

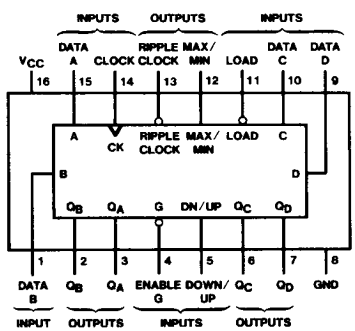
Two outputs have been made available to perform the cascading function; ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Single down/up count control line
- Look-ahead circuitry enhances speed of cascaded counters
- Fully synchronous in count modes
- Asynchronously presettable with load control

Connection Diagram

Dual-In-Line Package



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Order Number DM54ALS190J, DM54ALS191J, DM74ALS190M, DM74ALS191M, DM74ALS190N or DM74ALS191N
See NS Package Number J16A, M16A or N16A

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This document contains information on a device under development. National Semiconductor Corporation reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter			DM54ALS190, 191			DM74ALS190, 191			Units
				Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.8	V
I_{OH}	High Level Output Current					−0.4			−0.4	mA
I_{OL}	Low Level Output Current					4			8	mA
f_{CLOCK}	Clock Frequency	'ALS190		0		20	0		25	MHz
		'ALS191		0		25	0		30	MHz
t_W	Pulse Duration	CLK High or Low	'ALS190	25			20			ns
			'ALS191	20			16.5			ns
		$\overline{LOAD}$ Low		25			20			ns
t_{SU}	Setup Time	Data before $\overline{LOAD}$ ↑		25			20			ns
		G before CLK ↑		45			20			ns
		D/$\overline{U}$ before CLK ↑		45			20			ns
		$\overline{LOAD}$ Inactive before CLK ↑		20			20			ns
t_H	Hold Time	Data after $\overline{LOAD}$ ↑		5			5			ns
		G after CLK ↑		0			0			ns
		D/$\overline{U}$ after CLK ↑		0			0			ns
T_A	Operating Free Air Temperature			−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		DM74ALS190, 191			Units
				Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5V	74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V	G or CLK			−0.2	mA
			All Others			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V (Note 2)		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, All Inputs at 0V			12	22	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

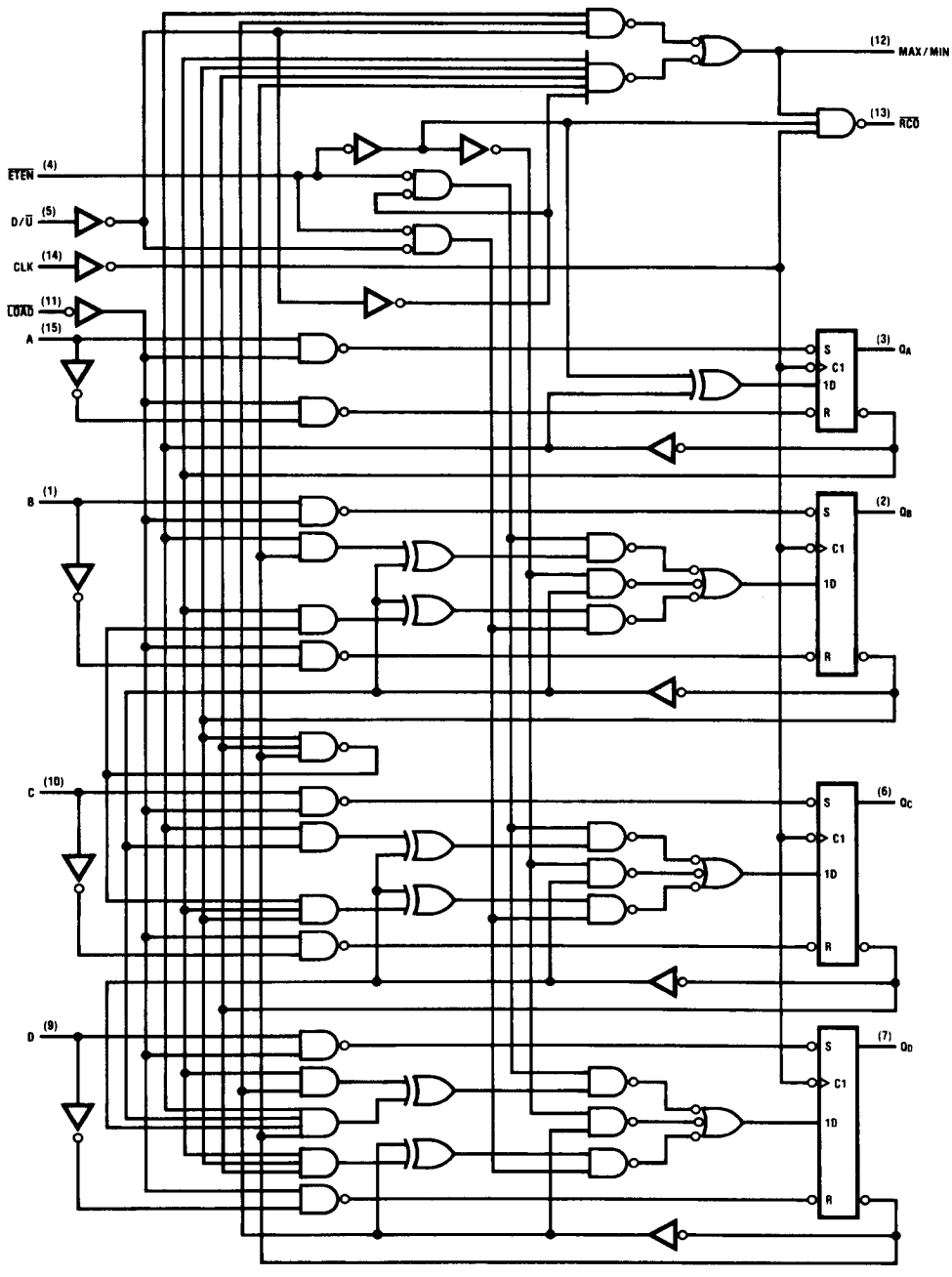
Switching Characteristics (Note 1)

Symbol	Parameter	From (Input) to (Output)	Conditions		DM54ALS190, 191		DM74ALS190, 191		Units
					Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω T_A = Min to Max	'ALS190	20		25		MHz
				'ALS191	25		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	$\overline{LOAD}$ to Any Q			7	37	8	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{LOAD}$ to Any Q			8	34	8	30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C, D to Any Q			4	25	4	21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C, D to Any Q			4	25	4	21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	CLK to $\overline{RCO}$			5	24	5	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	CLK to $\overline{RCO}$			5	24	5	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	CLK to Any Q			3	26	3	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	CLK to Any Q			3	22	3	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	CLK to Max/Min			8	37	8	31	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	CLK to Max/Min			8	34	8	31	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D/$\overline{U}$ to $\overline{RCO}$			12	45	15	37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D/$\overline{U}$ to $\overline{RCO}$			10	36	10	28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D/$\overline{U}$ to Max/Min			8	35	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D/$\overline{U}$ to Max/Min			8	30	8	25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	G to $\overline{RCO}$			4	21	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	G to $\overline{RCO}$			4	23	4	18	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagrams

ALS190



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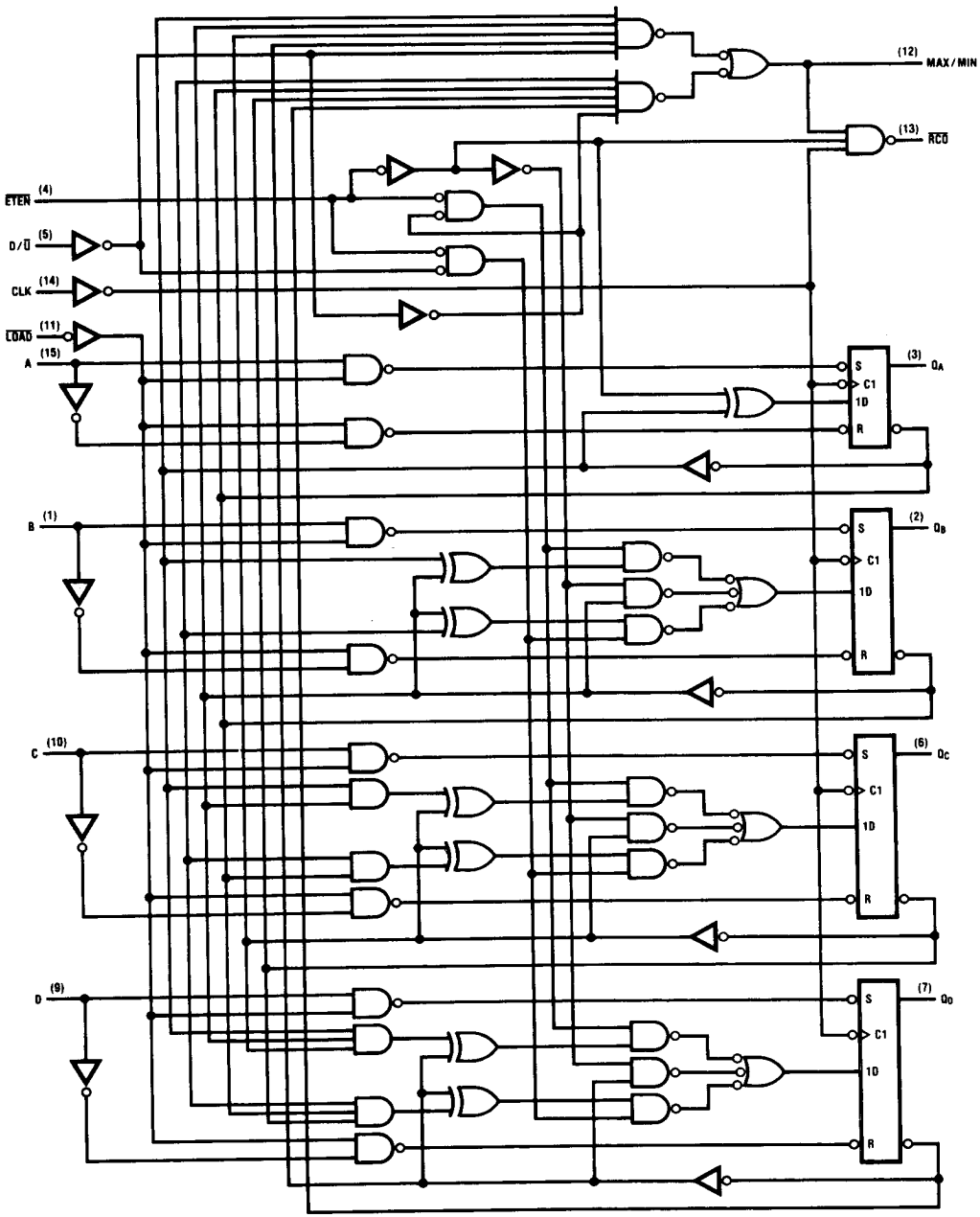
Pin numbers shown are for J and N packages.

Logic Diagrams (Continued)

ALS191



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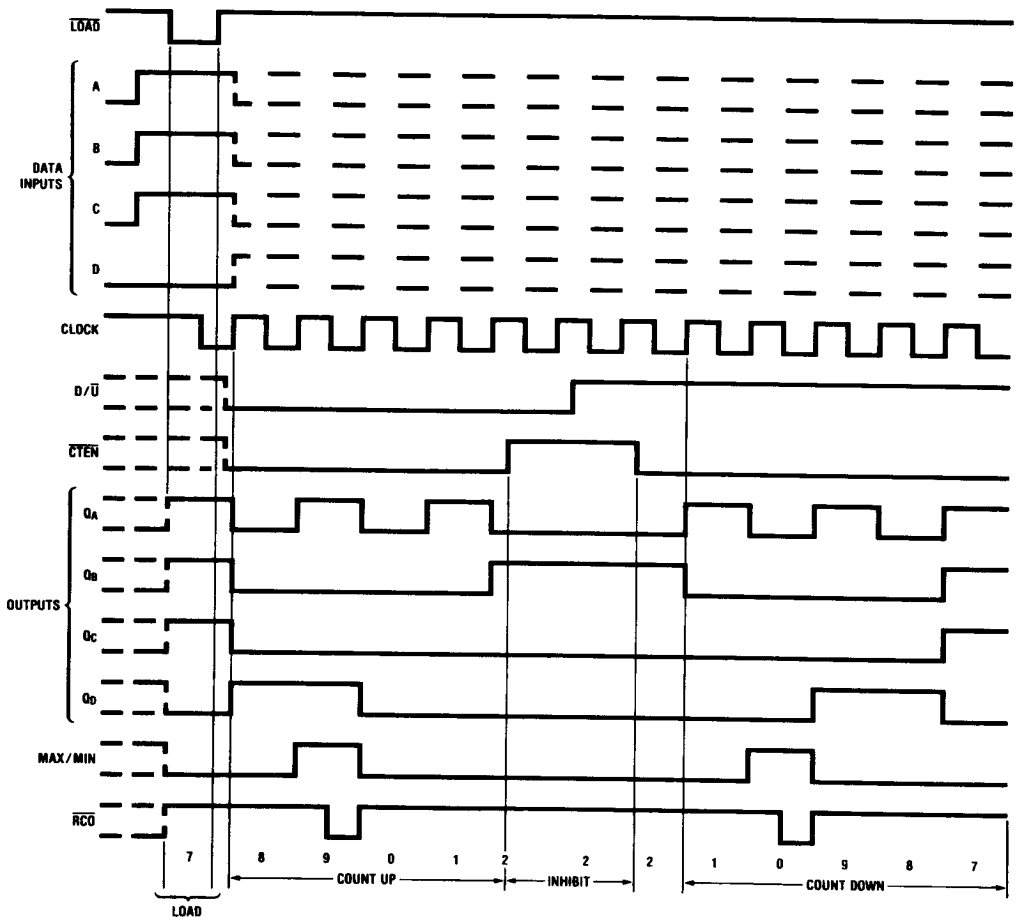
Pin numbers shown are for J and N packages.

Timing Diagrams

'ALS190 Typical Load, Count, and Inhibit Sequences



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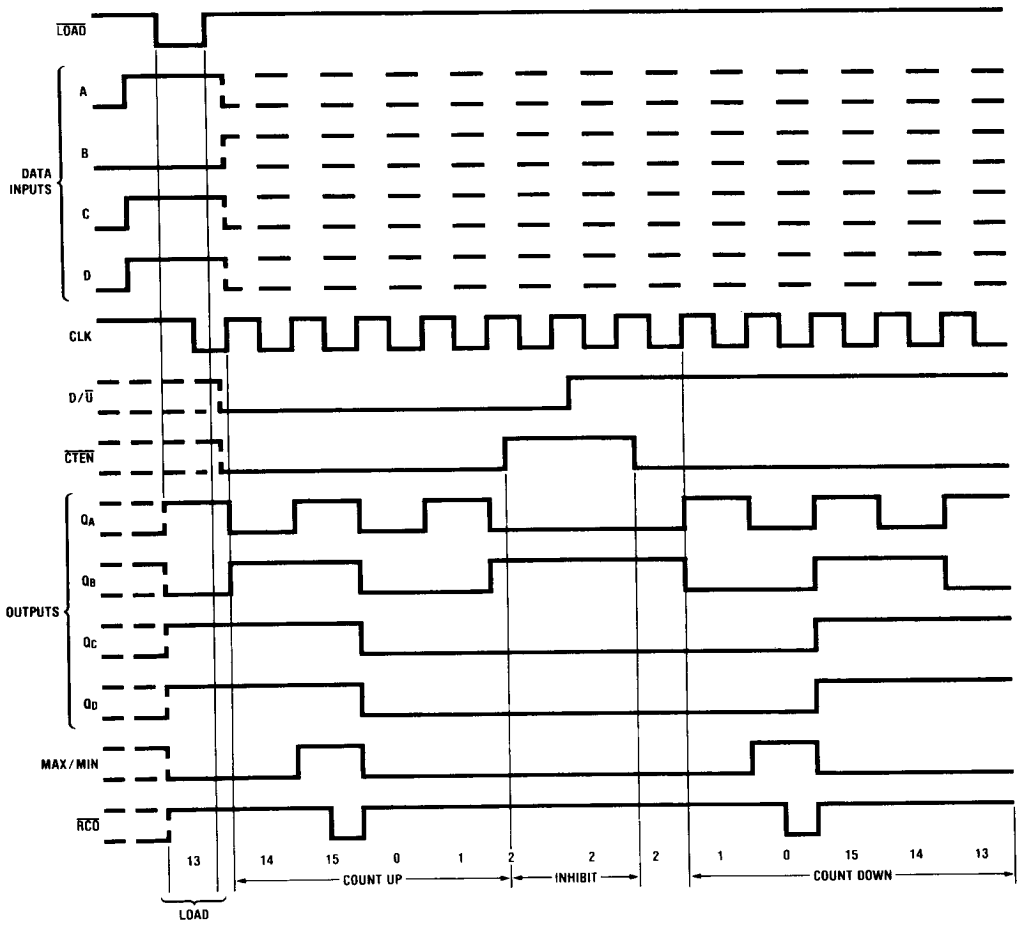
Timing Diagrams (Continued)

'ALS191 Typical Load, Count, and Inhibit Sequences



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