PI90LV14/PI90LVT14

1:5 Clock Distribution

Features

- Meets and Exceeds the Requirements of ANSI TIA/EIA-644-1995
- Designed for clocking rates up to 320MHz
- Operates from a single 3.3V Supply
- Low Voltage Differential Signaling (LVDS) with Output Voltages of ±350mV into a 100-ohm load
- Choice between LVDS or TTL clock input
- Synchronous Enable/Disable
- Clock outputs default LOW when inputs open
- Multiplexed clock input
  - Internal 300kohms pullup resistor on input pins
  - CLK & $\overline{CLK}$ have 110-ohm internal termination (PI90LVT14)
- 50ps Output-to-Output Skew
- 475ps typical propagation delay
- ±22ps Period Jitter
- Bus Pins are high impedance when disabled or with V_{CC} less than 1.5V
- TTL inputs are 5V Tolerant
- Power Dissipation at 400Mbits/s of 150mW
- Function compatible to Motorola (PECL)
  - MC100EL14 and Micrel/Synergy (PECL)
  - SY100EL14V
- >9kV ESD Protection
- 20-pin TSSOP (L) and QSOP (Q) packages

Pin Descriptions

Pin	Funtion
CLK, $\overline{CLK}$	Differential Clock Outputs
SCLK	LVTTL Clock Input
$\overline{EN}$	Synchronous Enable
SEL	Clock Select Input
$CLK1\text{-}5_{OUT\pm}$	Differential Clock Inputs

Function Table

CLK	SCLK	SEL	$\overline{EN}$*	CLKOUT+
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
↓	↓	X	H	Z*

* On next negative transition of CLK, or SCLK

Description

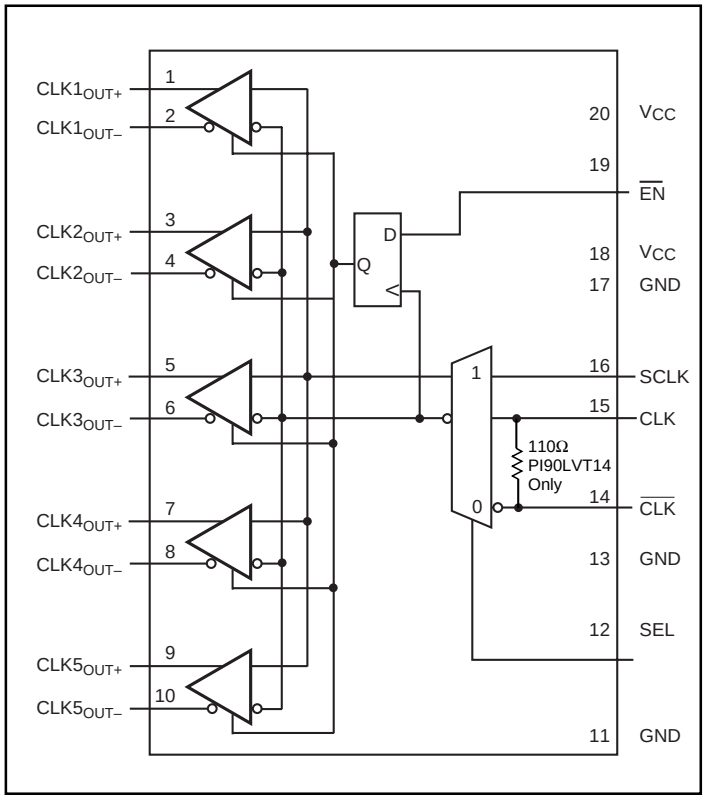
The PI90LV14 implements low voltage differential signaling (LVDS) to achieve clocking rates as high as 320MHz with low skew.

The PI90LV14 is a low-skew 1:5 clock distribution chip which incorporates multiplexed clock inputs to allow for distribution of a lower-speed, single-ended clock or a high-speed system clock. When LOWthe SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. Because the internal flip-flop is clocked on the falling edge of the input clock, all associated specification limits are referenced to the negative edge of the clock input.

The intended application of these devices and signaling technique is for high-speed clock distribution between boards.

PI90LV14 Block Diagram



Electrical Characteristics over Recommended Operating Conditions (unless otherwise noted).

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100Ω See Figures 1 and 2	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states		–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125	1.40	1.7	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			60	100	
I_{CC}	Supply Current	Enabled, R_L = 100Ω V_{IN} = V_{CC} or GND		21	35	mA
		Disabled, V_{IN} = V_{CC} or GND	0.5	2.5	4.0	
I_{IH}	High-level input current	V_{IH} = 2V		3.0	20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8V		5.0	20	
I_{OS}	Short-circuit output current	V_{ODOUT+} or V_{ODOUT-} = 0V			±7.4	mA
		V_{OD} = 0V			±4.7	
I_{OZ}	High-impedance output current	V_O = 0V or V_{CC}			1	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5V, V_O = 2.4V			1	
C_{IN}	Input capacitance,	V_I = 0.4 sin (4E6πt) +0.5V		9		pF
C_O	Output capacitance	V_I = 0.4 sin (4E6πt) +0.5V, Disabled		10		
R_{TERM}	Termination Resistor	PI90LVT14	90	110	132	Ω

Switching Characteristics over Recommended Operating Conditions (unless otherwise noted)[8,9].

Characteristic	Symbol	Min.	Typ.	Max.	Units	Condition
Propagation Delay to Output						
CLK to CLKOUT ±	t_{PLH}		3.0	4.0	ns	
SCLK to CLKOUT ±	t_{PHL}		2.5	3.5		
SEL to CLKOUT ±			2.6	3.6		
Disable Time						
CLK or SCLK to CLKOUT ±	t_{PHZ}		2.7	3.5	ns	2
	t_{PLZ}		2.7	3.5		
	t_{PZH}		4.7	6.0		
	t_{PZL}		3.7	6.0		
Part-to-Part Skew						
CLK (Diff) to Q	t_{skew}			TBD	ps	1
CLK (SE), SCLK to Q	t_{skew}			TBD		
With Device Skew	t_{skew}			TBD		
Cycle-to-Cycle Jitter	$t_{jit(cc)}$	–50		+50		Figure 6
Period Jitter	$t_{jit(per)}$	–22		+22		Figure 7
Setup Time						
$\overline{EN}$x to CLK	t_s	100	–100			2
$\overline{CEN}$ to CLK	t_s	100	–100			
Hold Time						
$\overline{EN}$x, $\overline{CEN}$ to SCLK	t_h		550	720		2
$\overline{EN}$x, $\overline{CEN}$ to CLKx	t_h		500	720		
Minimum Input Swing (CLK)	V_{PP}	0.20		0.800	V	3
Com. Mode Range (CLK)	V_{CMR}	0.125	1.5	V_{CC} - 0.20		4
Rise/Fall Times (20 – 80%)						
SCLK to CLKOUT±	t_r	150		1200	ps	
SCLK to CLKOUT±	t_f	150		1200		
Duty Cycle Distortion Pulse Skew (t_{PLH} - t_{PHL})	t_{SK1R}		200	300		5
Channel-to-Channel Skew, same edge	t_{SK2R}		70	190		6
Maximum Operating Frequency			250		MHz	7

Notes:

1. Within-Device skew is defined for identical transitions on similar paths through a device.
2. Setup, Hold, and Disable times are all relative to a falling edge on CLK or SCLK.
3. Minimum input swing for which AC parameters are guaranteed. Full DC LVDS output swings will be generated with only 50mV input swings.
4. The range in which the high level of the input swing must fall while meeting the V_{PP} spec.
5. t_{SKIR} is the difference in receiver propagation delay (t_{PLH}-t_{PHL}) of one device, and is the duty cycle distortion of the output at any given temperature and V_{CC}. The propagation delay specification is a device-to-device worst case over process, voltage, and temperature.
6. t_{SK2R} is the difference in receiver propagation delay between channels in the same device of any outputs switching in the same direction. This parameter is guaranteed by design and characterization.
7. Generator input conditions: $t_r t_f < 1$ns, 50% duty cycle, differential (1.10V to 1.35V peak-peak). Output Criteria: 60%/40% duty cycle, V_{OL} (max) 0-4V, V_{OH} (min) 2.7V, Load - 7pF (stray plus probes).
8. C_L includes probe and fixture capacitance.
9. Generator waveform for all tests unless otherwise specified: f = 25 MHz, Z_O = 50 ohms, t_r = 1ns, t_f = 1ns (35%-65%). To ensure fastest propagation delay & minimum skew, clock input edge rates should not be slower than 1ns/V; control signals not slower than 3ns/V.

Parameter Measurement Information

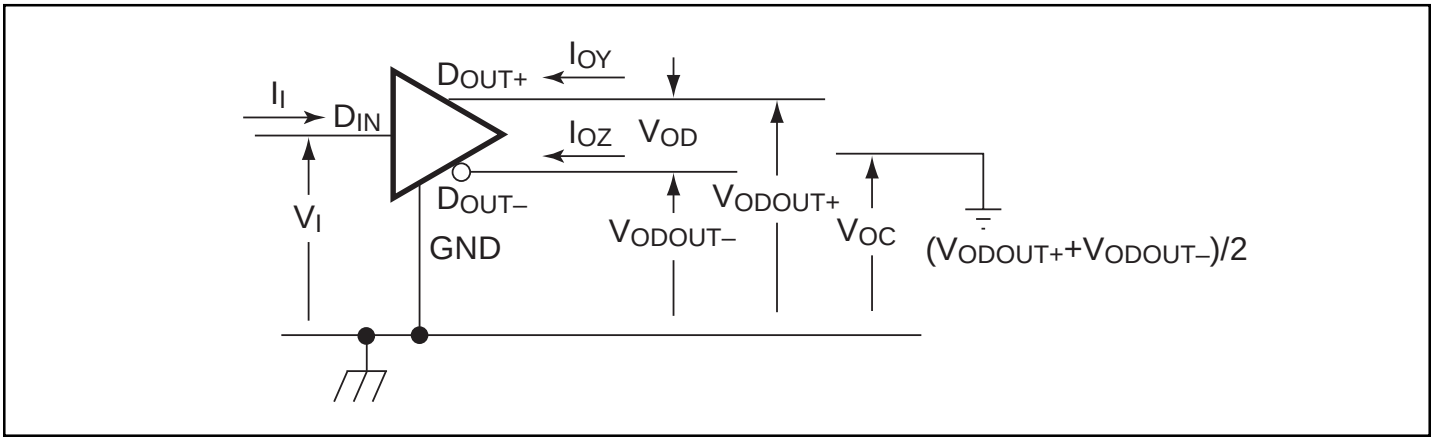


Figure 1. Voltage and Current Definitions

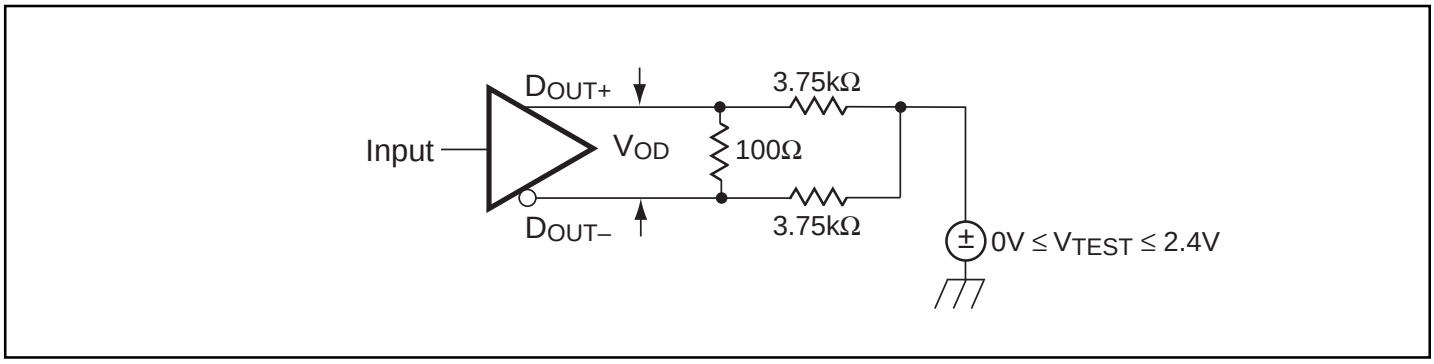
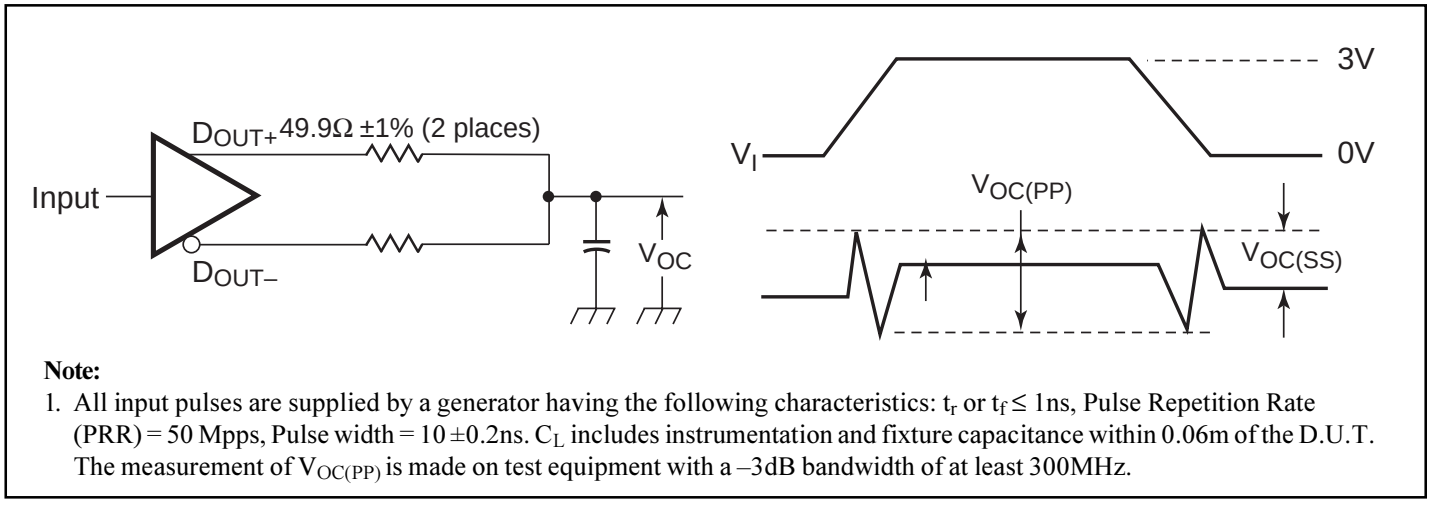


Figure 2. V_{OD} Test Circuit

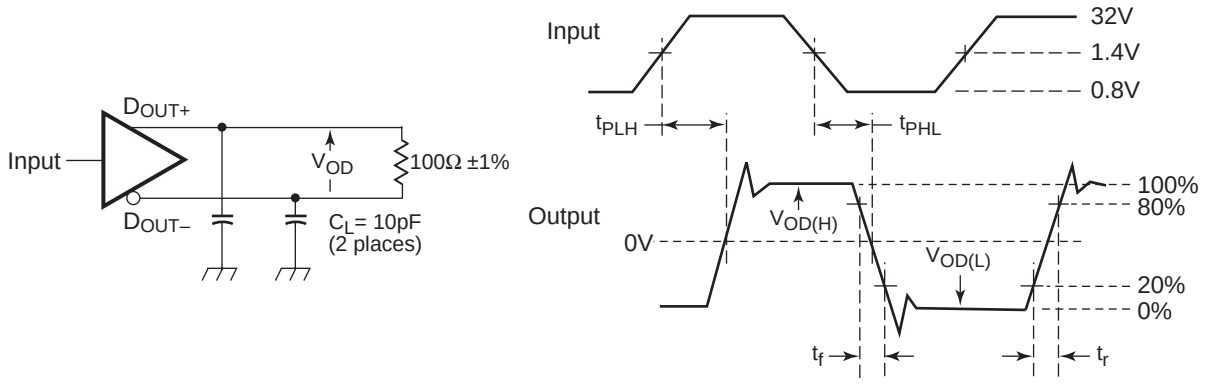


Note:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1ns, Pulse Repetition Rate (PRR) = 50 Mpps, Pulse width = 10 ±0.2ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3dB bandwidth of at least 300MHz.

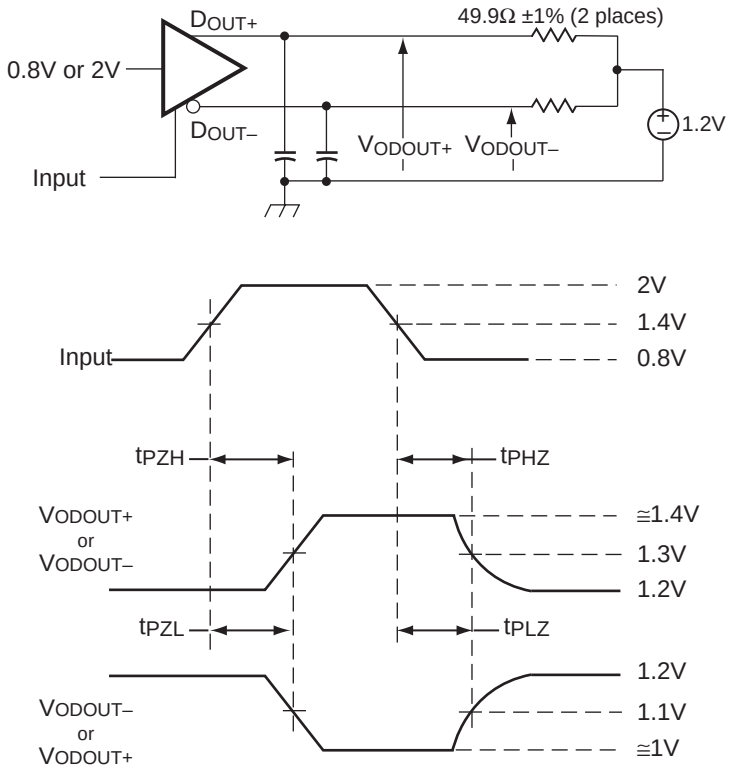
Figure 3. Test Circuit & Definitions for the Driver Common-Mode Output Voltage

Parameter Measurement Information (continued)



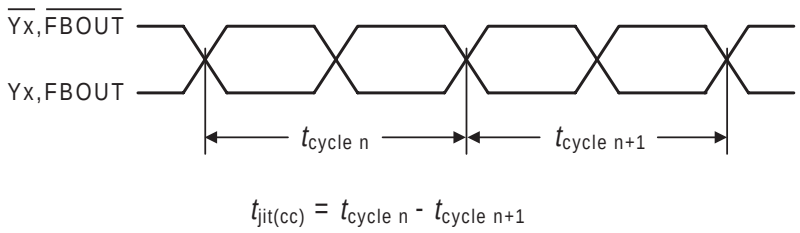
Note:
1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1ns, Pulse Repetition Rate (PRR) = 15 Mpps, Pulse width = 10 ±0.2ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

Figure 4. Test Circuit, Timing, & Voltage Definitions for the Differential Output Signal



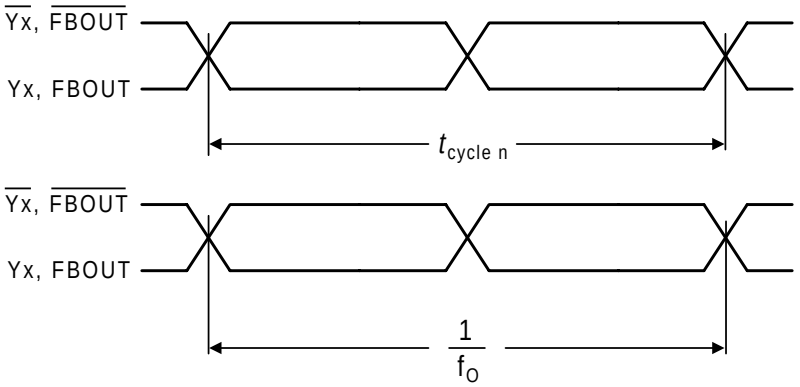
Note:
1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1ns, Pulse Repetition Rate (PRR) = 0.5 Mpps, Pulse width = 500 ±10ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

Figure 5. Enable & Disable Time Circuit & Definitions



$$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$$

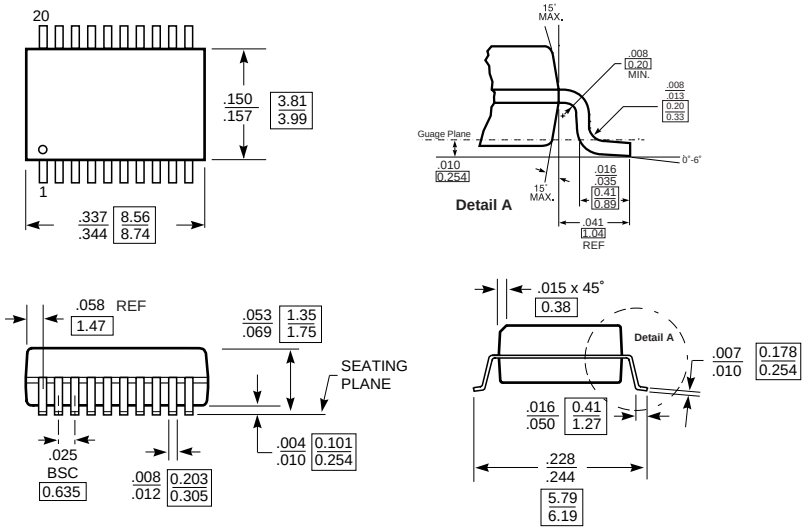
Figure 6. Cycle-to-Cycle Jitter



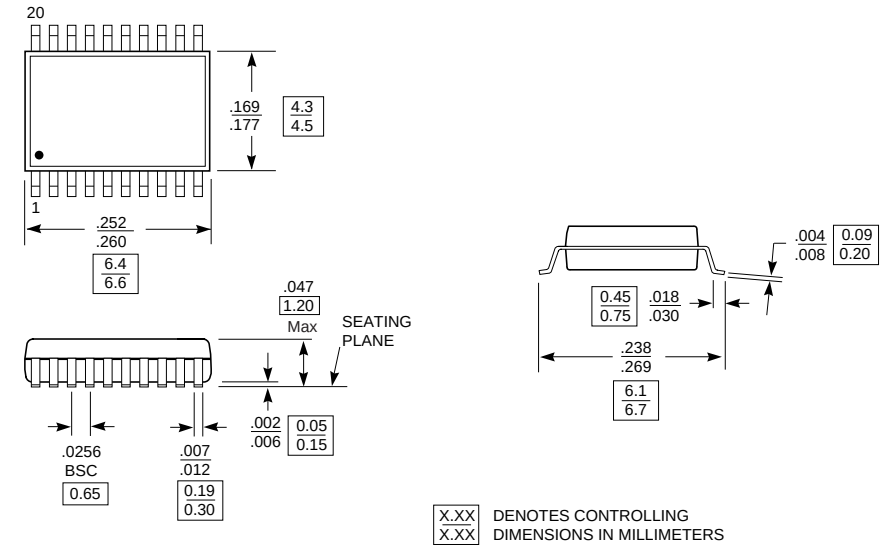
$$t_{jit(per)} = t_{cycle\ n} - \frac{1}{f_O}$$

Figure 7. Period Jitter

20-Pin QSOP (Q) Package



20-Pin TSSOP (L) Package



Ordering Information

Ordering Code	Package Type	Ordering Range
PI90LV14L	20-Pin 173-mil TSSOP	–40°C to 85°C
PI90LVT14L		
PI90LV14Q	20-Pin 150-mil QSOP	
PI90LVT14Q		