74HC299-Q100

8-bit universal shift register; 3-state

Rev. 2 — 5 August 2024 Product data sheet

1. General description

The 74HC299-Q100 is an 8-bit universal shift register with 3-state outputs. It contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift-right, shift-left, parallel load and hold operations. The type of operation is determined by the mode select inputs S0 and S1. Pins I/O0 to I/O7 are flip-flop 3-state buffer outputs which allow them to operate as data inputs in parallel load mode. The serial outputs Q0 and Q7 are used for expansion in serial shifting of longer words. A LOW signal on the asynchronous master reset input $\overline{MR}$ overrides the Sn and clock CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock pulse. Inputs can change when the clock is either state, provided that the recommended set-up and hold times are observed. A HIGH signal on the 3-state output enable inputs $\overline{OE}1$ or $\overline{OE}2$ disables the 3-state buffers and the I/On outputs assume a high-impedance OFF-state. In this condition, the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S0 and S1, when in preparation for a parallel load operation. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- CMOS input levels
- Multiplexed inputs/outputs provide improved bit density
- Four operating modes:
  - Shift left
  - Shift right
  - Hold (store)
  - Load data
- Operates with output enable or at high-impedance OFF-state
- 3-state outputs drive bus lines directly
- Cascadable for n-bit word lengths
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC299D-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4. Functional diagram

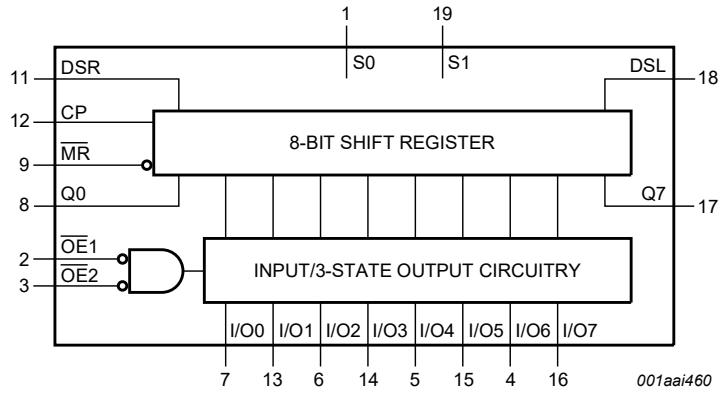


Fig. 1. Functional diagram

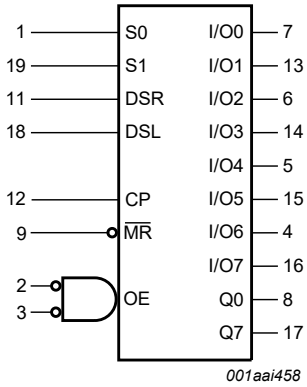


Fig. 2. Logic symbol

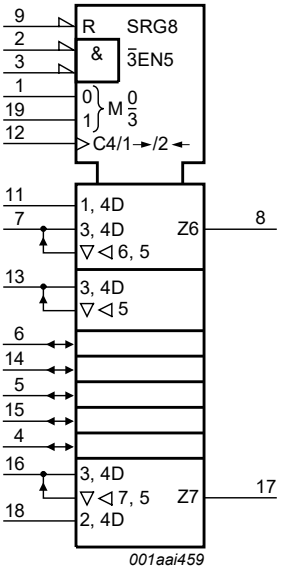


Fig. 3. IEC logic symbol

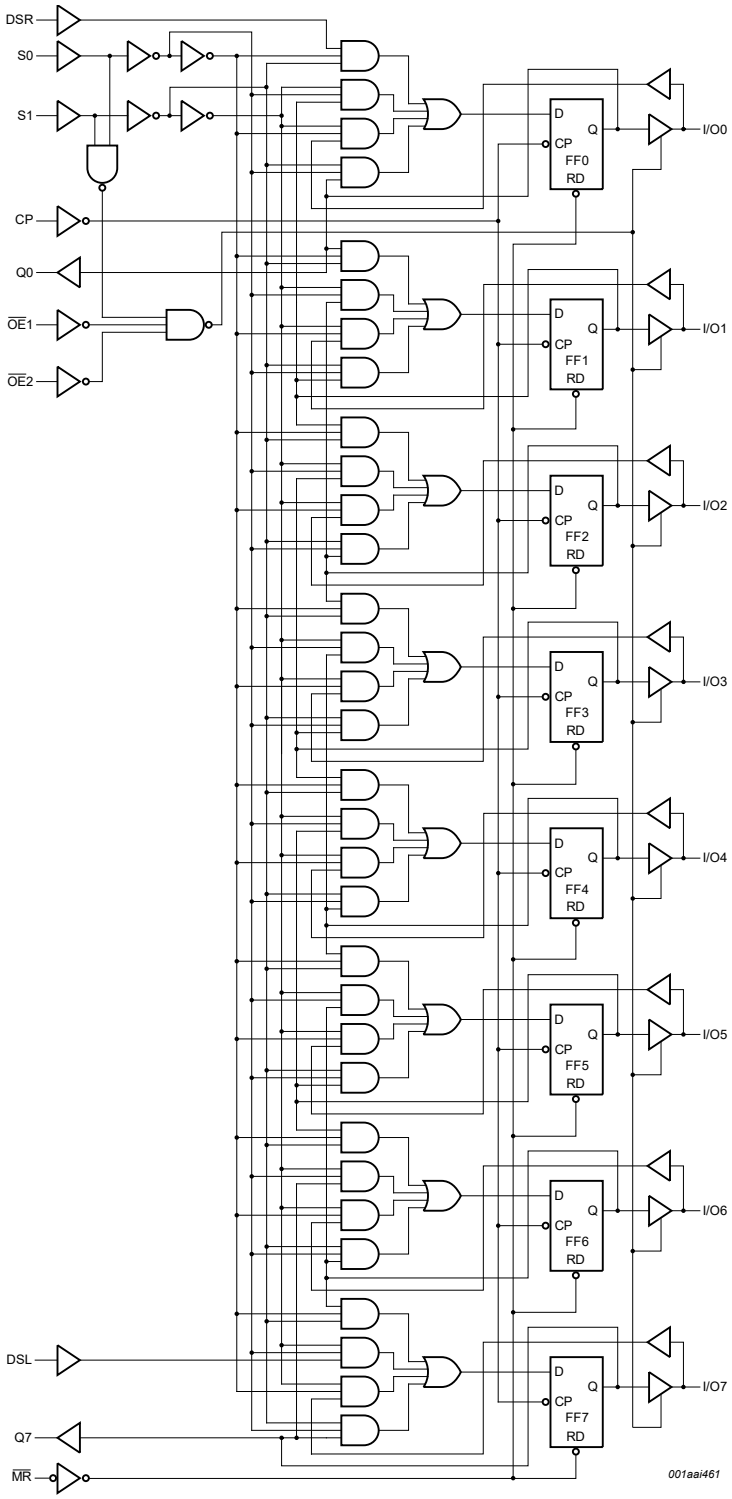
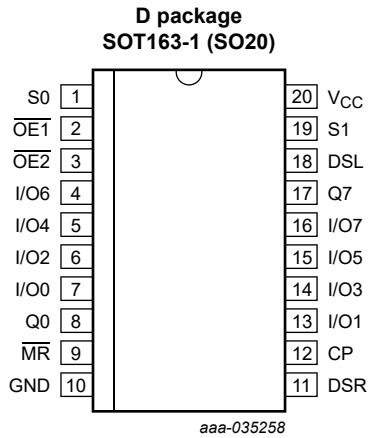


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
S0, S1	1, 19	mode select input
$\overline{OE}1$, $\overline{OE}2$	2, 3	3-state output enable input (active LOW)
I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7	7, 13, 6, 14, 5, 15, 4, 16	parallel data input or 3-state parallel output (bus driver)
Q0, Q7	8, 17	serial output (standard output)
$\overline{MR}$	9	asynchronous master reset input (active LOW)
GND	10	ground (0 V)
DSR	11	serial data shift-right input
CP	12	clock input (LOW to HIGH, edge-triggered)
DSL	18	serial data shift-left input
V_{CC}	20	positive supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; ↑ = LOW to HIGH CP transition; X = don't care.

Input				Response
$\overline{MR}$	S1	S0	CP	
L	X	X	X	asynchronous reset; Q0 to Q7 = LOW
H	H	H	↑	parallel load; I/On → Qn
H	L	H	↑	shift right; DSR → Q0, Q0 → Q1, etc.
H	H	L	↑	shift left; DSL → Q7, Q7 → Q6, etc.
H	L	L	X	hold

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V				
		standard outputs		-	±25	mA
		bus driver outputs		-	±35	mA
I_{CC}	supply current	standard outputs		-	50	mA
		bus driver outputs		-	70	mA
I_{GND}	ground current	standard outputs		-50	-	mA
		bus driver outputs		-70	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		all outputs								
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		standard outputs								
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
		bus driver outputs								
		I_O = -6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		all outputs								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		standard outputs								
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
		bus driver outputs								
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_{CC} = 6.0 V; V_O = V_{CC} or GND	-	-	±0.5	-	±5.0	-	±10.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
$C_{I/O}$	input/output capacitance		-	10	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [1]	-	120	-	-	-	-	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); for test circuit, see Fig. 9.

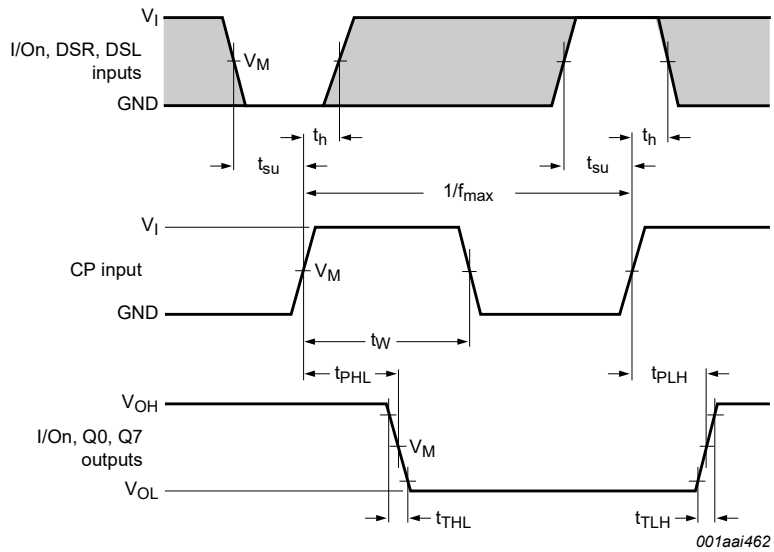
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	CP to Q0, Q7; see Fig. 5 [1]								
		V_{CC} = 2.0 V	-	66	200	-	250	-	300	ns
		V_{CC} = 4.5 V	-	24	40	-	50	-	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	19	34	-	43	-	51	ns
		CP to I/On; see Fig. 5								
		V_{CC} = 2.0 V	-	66	200	-	250	-	300	ns
		V_{CC} = 4.5 V	-	24	40	-	50	-	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	19	34	-	43	-	51	ns
		$\overline{MR}$ to Q0, Q7 or I/On; see Fig. 6 [2]								
		V_{CC} = 2.0 V	-	66	200	-	250	-	300	ns
		V_{CC} = 4.5 V	-	24	40	-	50	-	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	19	34	-	43	-	51	ns
t_t	transition time	bus driver (I/On); see Fig. 5 [3]								
		V_{CC} = 2.0 V	-	14	60	-	75	-	90	ns
		V_{CC} = 4.5 V	-	5	12	-	15	-	18	ns
		V_{CC} = 6.0 V	-	4	10	-	13	-	15	ns
		standard (Q0, Q7); see Fig. 5								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_W	pulse width	CP HIGH or LOW; see Fig. 5								
		V_{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	5	-	17	-	20	-	ns
		$\overline{MR}$ LOW; see Fig. 6								
		V_{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$n to I/On; see Fig. 8 [4]								
		V_{CC} = 2.0 V	-	50	155	-	195	-	235	ns
		V_{CC} = 4.5 V	-	18	31	-	39	-	47	ns
		V_{CC} = 6.0 V	-	14	26	-	33	-	40	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$n to I/On; see Fig. 8								
		V_{CC} = 2.0 V	-	41	130	-	165	-	195	ns
		V_{CC} = 4.5 V	-	15	26	-	33	-	39	ns
		V_{CC} = 6.0 V	-	12	22	-	28	-	33	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$n to I/On; see Fig. 8 [5]								
		V_{CC} = 2.0 V	-	66	185	-	230	-	280	ns
		V_{CC} = 4.5 V	-	24	37	-	46	-	56	ns
		V_{CC} = 6.0 V	-	19	31	-	39	-	48	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$n to I/On; see Fig. 8								
		V_{CC} = 2.0 V	-	55	155	-	195	-	235	ns
		V_{CC} = 4.5 V	-	20	31	-	39	-	47	ns
		V_{CC} = 6.0 V	-	16	26	-	33	-	40	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Fig. 6								
		V_{CC} = 2.0 V	5	-14	-	5	-	5	-	ns
		V_{CC} = 4.5 V	5	-5	-	5	-	5	-	ns
		V_{CC} = 6.0 V	5	-4	-	5	-	5	-	ns
t_{su}	set-up time	DSR, DSL to CP; see Fig. 5								
		V_{CC} = 2.0 V	100	33	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	12	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	10	-	21	-	26	-	ns
		S0, S1 to CP; see Fig. 7								
		V_{CC} = 2.0 V	100	33	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	12	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	10	-	21	-	26	-	ns
		I/On to CP; see Fig. 5								
		V_{CC} = 2.0 V	125	39	-	155	-	190	-	ns
		V_{CC} = 4.5 V	25	14	-	31	-	38	-	ns
		V_{CC} = 6.0 V	21	11	-	26	-	32	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_h	hold time	I/On, DSR, DSL to CP; see Fig. 5								
		V_{CC} = 2.0 V	0	-14	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	-5	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	-4	-	0	-	0	-	ns
		S0, S1 to CP; see Fig. 7								
		V_{CC} = 2.0 V	0	-28	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	-10	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	-8	-	0	-	0	-	ns
f_{max}	maximum frequency	CP input; see Fig. 5								
		V_{CC} = 2.0 V	5.0	15	-	4.0	-	3.4	-	MHz
		V_{CC} = 4.5 V	25	45	-	20	-	17	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	50	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	29	54	-	24	-	20	-	MHz

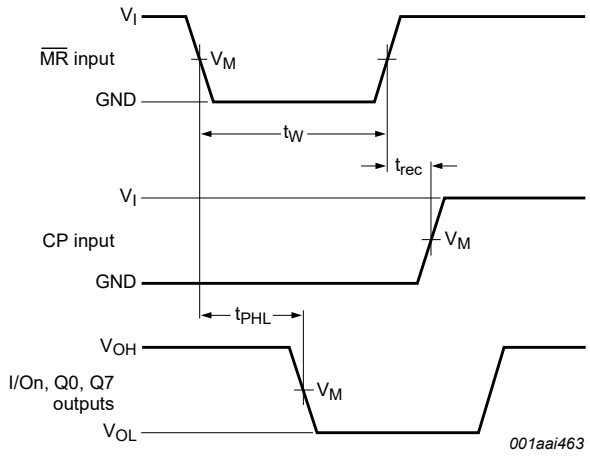
[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_{pd} is the same as t_{PHL}.
[3] t_t is the same as t_{THL} and t_{TLH}.
[4] t_{en} is the same as t_{PZH} and t_{PZL}.
[5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

10.1. Waveforms and test circuit



The shaded areas indicate when the input is permitted to change for predictable output performance.
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

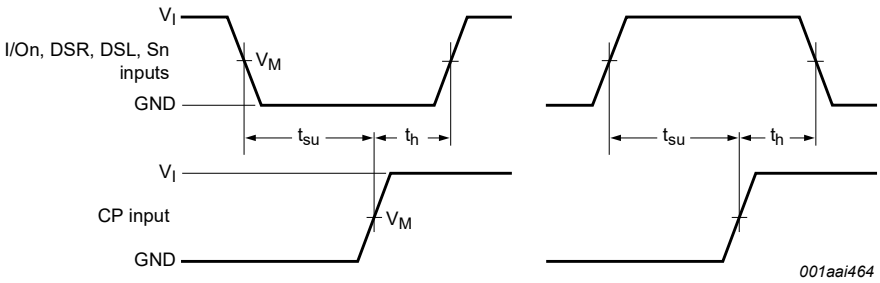
Fig. 5. Clock pulse to outputs I/On, Q0, Q7 propagation delays, the clock pulse width, the I/On, DSR and DSL to clock pulse set-up and hold times, the output transition times and the maximum clock frequency



Measurement points are given in Table 8.

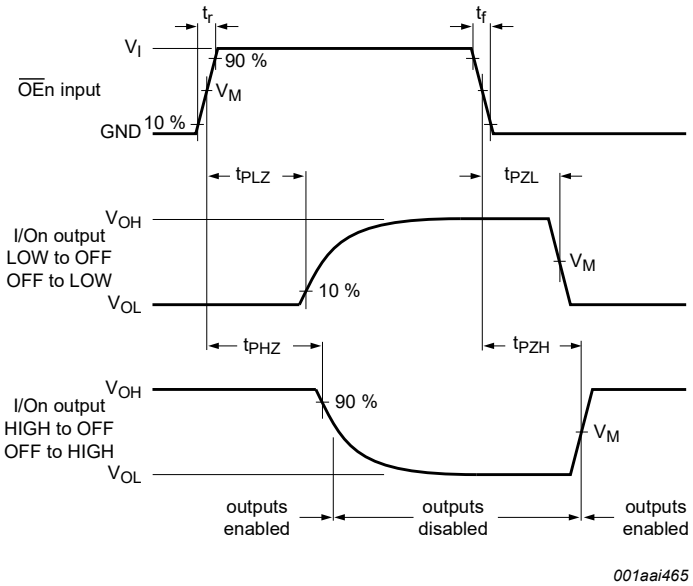
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. The master reset pulse width (LOW), the master reset to outputs I/On, Q0, Q7 propagation delays and the master reset to clock pulse removal time



Measurement points are given in Table 8.

Fig. 7. Set-up and hold times from the mode control inputs S0, S1 to the clock pulse



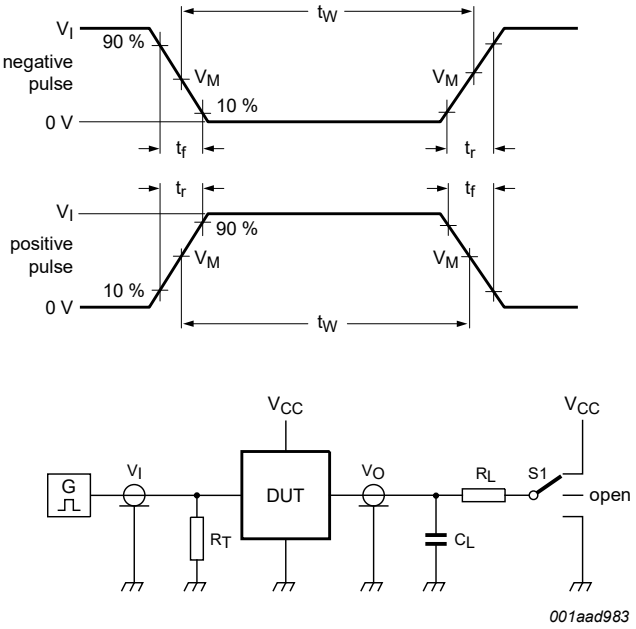
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. 3-state enable and disable times for $\overline{OE}$n inputs

Table 8. Measurement points

Input		Output
V_I	V_M	V_M
V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

S1 = Test selection switch.

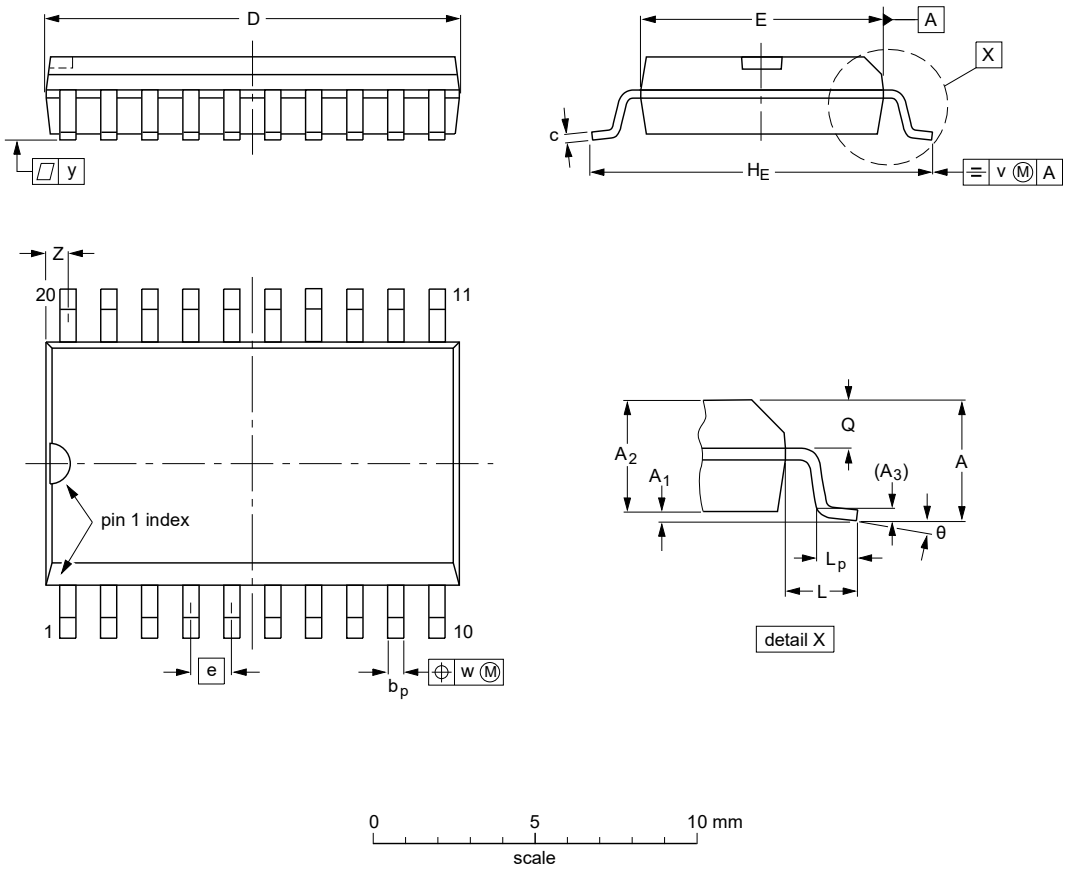
Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig. 10. Package outline SOT163-1 (SO20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC299_Q100 v.2	20240805	Product data sheet	-	74HC299_Q100 v.1
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC299_Q100 v.1	20200302	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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