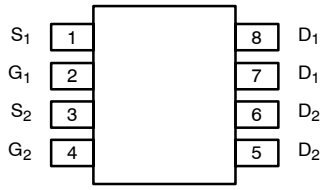
Dual P-Channel 2.5-V (G-S) MOSFET

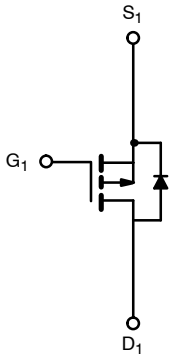
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–20	0.032 @ V_{GS} = –4.5 V	–6.5
	0.050 @ V_{GS} = –2.5 V	–5.2

SO-8

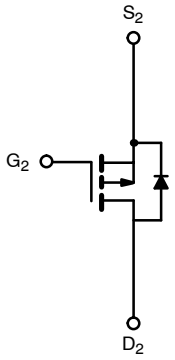


Top View

Ordering Information: Si4963BDY—E3 (Lead Free)
Si4963BDY-T1—E3 (Lead Free with Tape and Reel)



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	–20		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	–6.5	–4.9	A
	T_A = 70°C		–5.2	–3.9	
Pulsed Drain Current		I_{DM}	–40		
continuous Source Current (Diode Conduction)[a]		I_S	–1.7	–0.9	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	1.1	W
	T_A = 70°C		1.3	0.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	58	62.5	°C/W
	Steady State		91	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	34	40	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm

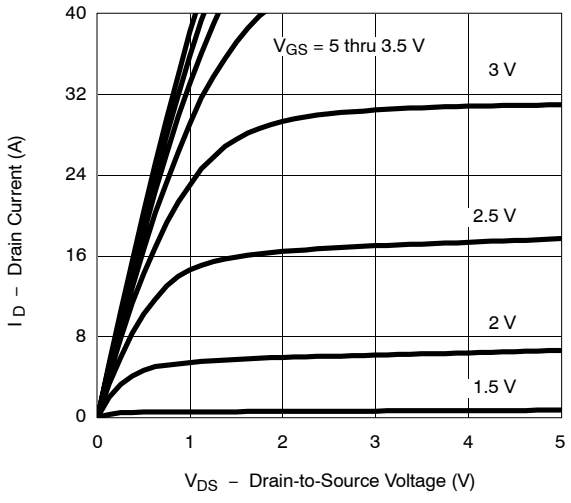
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA	−0.6		−1.4	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −20 V, V_{GS} = 0 V			−1	μA
		V_{DS} = −20 V, V_{GS} = 0 V, T_J = 55°C			−5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −4.5 V, I_D = −6.5 A		0.025	0.032	Ω
		V_{GS} = −2.5 V, I_D = −2 A		0.040	0.050	
Forward Transconductance[a]	g_{fs}	V_{DS} = −10 V, I_D = −6.5 A		18		S
Diode Forward Voltage[a]	V_{SD}	I_S = −1.7 A, V_{GS} = 0 V		−0.75	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −4.5 V, I_D = −6.5 A		14	21	nC
Gate-Source Charge	Q_{gs}			2.6		
Gate-Drain Charge	Q_{gd}			4.6		
Gate Resistance	R_g	f = 1 MHz		8.3		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −4.5 V, R_g = 6 Ω		30	45	ns
Rise Time	t_r			40	60	
Turn-Off Delay Time	$t_{d(off)}$			80	120	
Fall Time	t_f			55	85	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −1.7 A, di/dt = 100 A/μs		40	80	

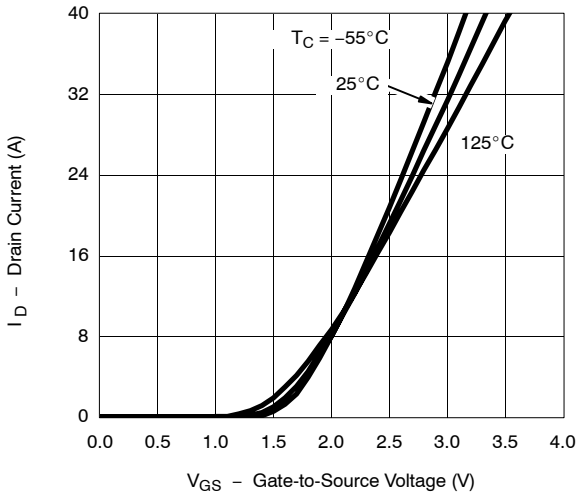
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

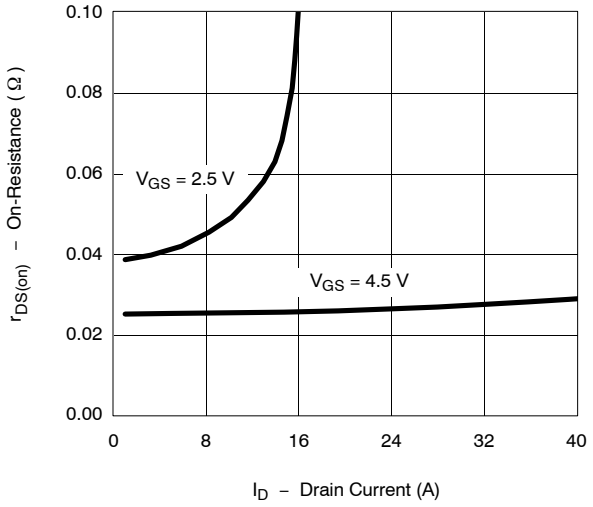


Transfer Characteristics

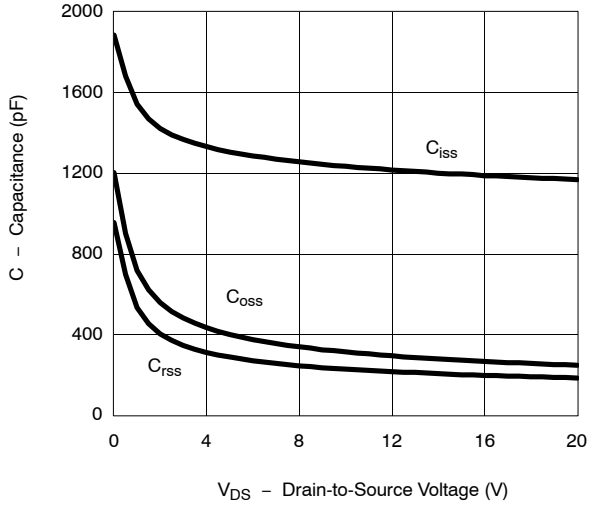


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

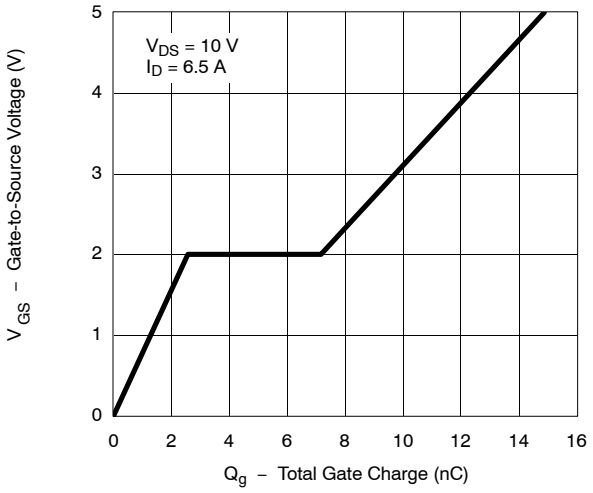
On-Resistance vs. Drain Current



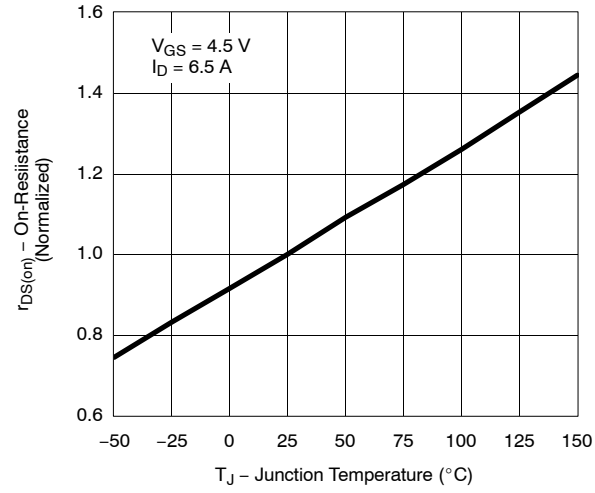
Capacitance



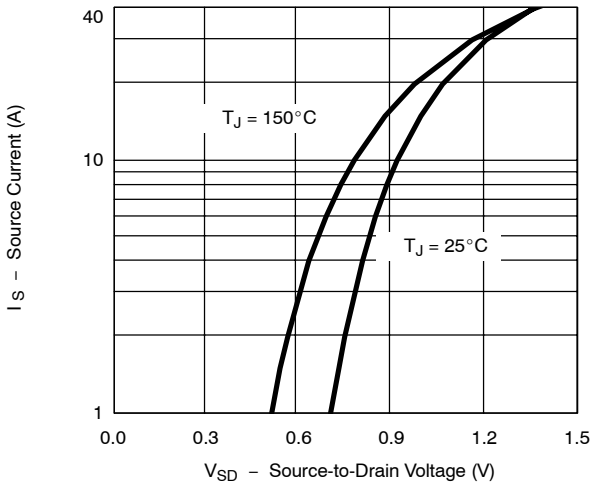
Gate Charge



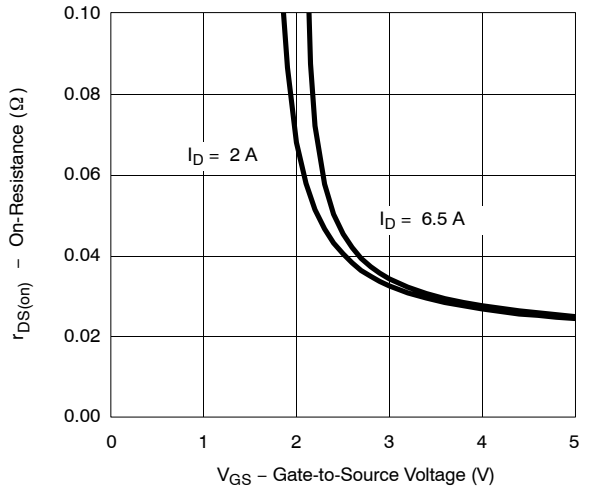
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

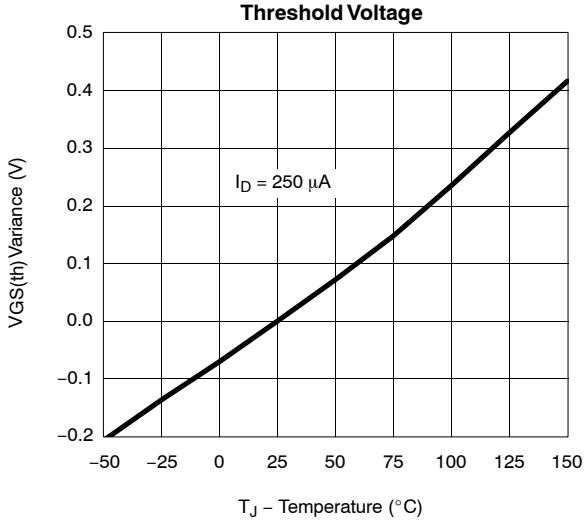


On-Resistance vs. Gate-to-Source Voltage

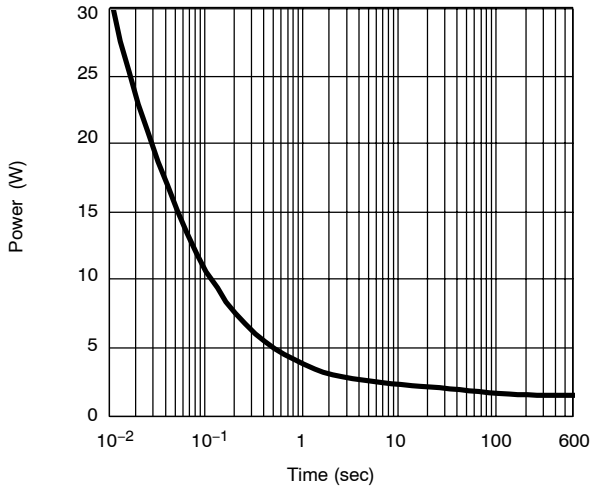


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

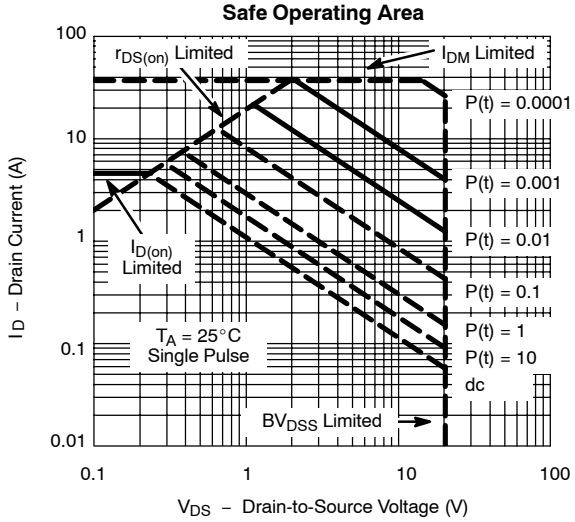
Threshold Voltage



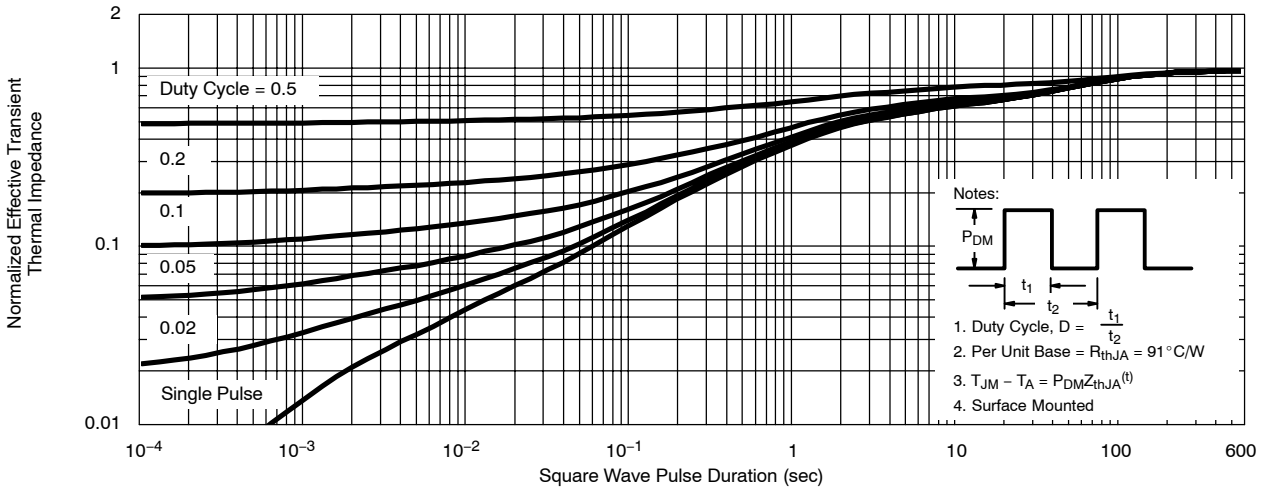
Single Pulse Power



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)