

## 2.5-W MONO FILTER-FREE CLASS-D AUDIO POWER AMPLIFIER

### FEATURES

- Pin-to-Pin Compatibility with TPA2010D1
- 32 ms Start-up Time Eliminates CODEC Click/Pop noise
- Maximum Battery Life and Minimum Heat
  - Efficiency With an 8-Ω Speaker:
    - 88% at 400 mW
    - 2.8-mA Quiescent Current
    - 0.5-μA Shutdown Current
- Only Three External Components
  - Optimized PWM Output Stage Eliminates LC Output Filter
  - Improved PSRR (–75 dB) and Wide Supply Voltage (2.5 V to 5.5 V) Eliminates Need for a Voltage Regulator
  - Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor
  - Improved CMRR Eliminates Two Input Coupling Capacitors
- Wafer Chip Scale Packaging (WCSP)
  - NanoFree™ (YZF)

### APPLICATIONS

- Ideal for Wireless or Cellular Handsets and PDAs

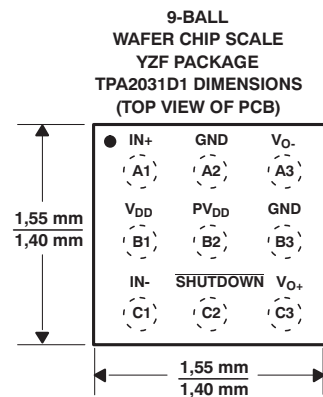
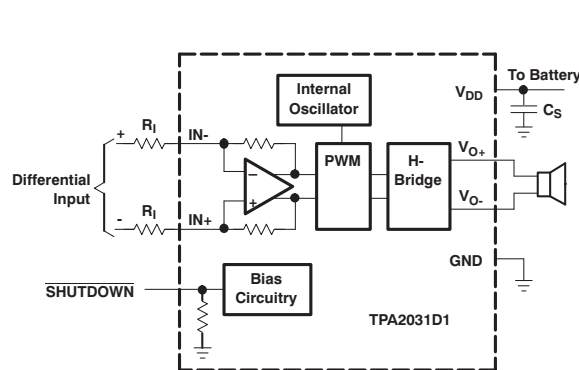
### DESCRIPTION

The TPA2031D1 is a 2.5-W high efficiency filter-free class-D audio power amplifier in a 1,45 mm × 1,45 mm wafer chip scale package (WCSP) that requires only three external components.

Features like 88% efficiency, –75-dB PSRR, improved RF-rectification immunity, and 8 mm<sup>2</sup> total PCB area make the TPA2031D1 class-D amp ideal for cellular handsets. 32 ms start-up time allows the TPA2031D1 to share the same GPIO enable/shutdown control as the CODEC without passing through the CODEC turn-on pop.

In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the TPA2031D1. The TPA2031D1 allows independent gain while summing signals from separate sources, and has a low 36 μV noise floor, A-weighted.

### APPLICATION CIRCUIT



Note: Pin A1 is marked with a "0" for Pb-free (YZF).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE	PART NUMBER	SYMBOL
–40°C to 85°C	Wafer chip scale packaging – Lead free (YZF)	TPA2031D1YZF <sup>(1)</sup>	CEI

- (1) The YZF package is only available taped and reeled. Add the suffix *R* to the end of the part number for a reel of 3000 (e.g., TPA2031D1YZFR); or, add the suffix *T* for a reel of 250 (e.g., TPA2031D1YZFT).

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

TPA2031D1		
V <sub>DD</sub>	Supply voltage	In active mode
		In <u>SHUTDOWN</u> mode
V <sub>I</sub>	Input voltage	–0.3 V to V <sub>DD</sub> + 0.3 V
	Continuous total power dissipation	See Dissipation Rating Table
T <sub>A</sub>	Operating free-air temperature	–40°C to 85°C
T <sub>J</sub>	Operating junction temperature	–40°C to 150°C
T <sub>stg</sub>	Storage temperature	–65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these are any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage	2.5		5.5	V
V <sub>IH</sub>	High-level input voltage	1.3		V <sub>DD</sub>	V
V <sub>IL</sub>	Low-level input voltage	0		0.35	V
R <sub>I</sub>	Input resistor	15			kΩ
V <sub>IC</sub>	Common mode input voltage range	0.5		V <sub>DD</sub> –0.8	V
T <sub>A</sub>	Operating free-air temperature	–40		85	°C

## PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING FACTOR <sup>(1)</sup>	T <sub>A</sub> ≤ 25°C POWER RATING	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
YZF	7.8 mW/°C	975 mW	624 mW	507 mW

- (1) Derating factor measured with High-K board.

## ELECTRICAL CHARACTERISTICS

 $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OS} $ Output offset voltage (measured differentially)	$V_I = 0\text{ V}$ , $A_V = 2\text{ V/V}$ , $V_{DD} = 2.5\text{ V to }5.5\text{ V}$		1	25	mV
PSRR Power supply rejection ratio	$V_{DD} = 2.5\text{ V to }5.5\text{ V}$		–75	–55	dB
CMRR Common mode rejection ratio	$V_{DD} = 2.5\text{ V to }5.5\text{ V}$ , $V_{IC} = V_{DD}/2\text{ to }0.5\text{ V}$ , $V_{IC} = V_{DD}/2\text{ to }V_{DD} - 0.8\text{ V}$		–68	–49	dB
$ I_{IH} $ High-level input current	$V_{DD} = 5.5\text{ V}$ , $V_I = 5.8\text{ V}$			100	$\mu\text{A}$
$ I_{IL} $ Low-level input current	$V_{DD} = 5.5\text{ V}$ , $V_I = -0.3\text{ V}$			5	$\mu\text{A}$
$I_{(Q)}$ Quiescent current	$V_{DD} = 5.5\text{ V}$ , no load		3.4	4.9	mA
	$V_{DD} = 3.6\text{ V}$ , no load		2.8		
	$V_{DD} = 2.5\text{ V}$ , no load		2.2	3.2	
$I_{(SD)}$ Shutdown current	$V_{(\overline{\text{SHUTDOWN}})} = 0.35\text{ V}$ , $V_{DD} = 2.5\text{ V to }5.5\text{ V}$		0.5	2	$\mu\text{A}$
$r_{DS(on)}$ Static drain-source on-state resistance	$V_{DD} = 2.5\text{ V}$		700		m $\Omega$
	$V_{DD} = 3.6\text{ V}$		500		
	$V_{DD} = 5.5\text{ V}$		400		
Output impedance in $\overline{\text{SHUTDOWN}}$	$V_{(\overline{\text{SHUTDOWN}})} = 0.4\text{ V}$		>1		k $\Omega$
$f_{(sw)}$ Switching frequency	$V_{DD} = 2.5\text{ V to }5.5\text{ V}$	200	250	300	kHz
Gain	$V_{DD} = 2.5\text{ V to }5.5\text{ V}$	$\frac{285\text{ k}\Omega}{R_I}$	$\frac{300\text{ k}\Omega}{R_I}$	$\frac{315\text{ k}\Omega}{R_I}$	$\frac{\text{V}}{\text{V}}$
Resistance from shutdown to GND			300		k $\Omega$

## OPERATING CHARACTERISTICS

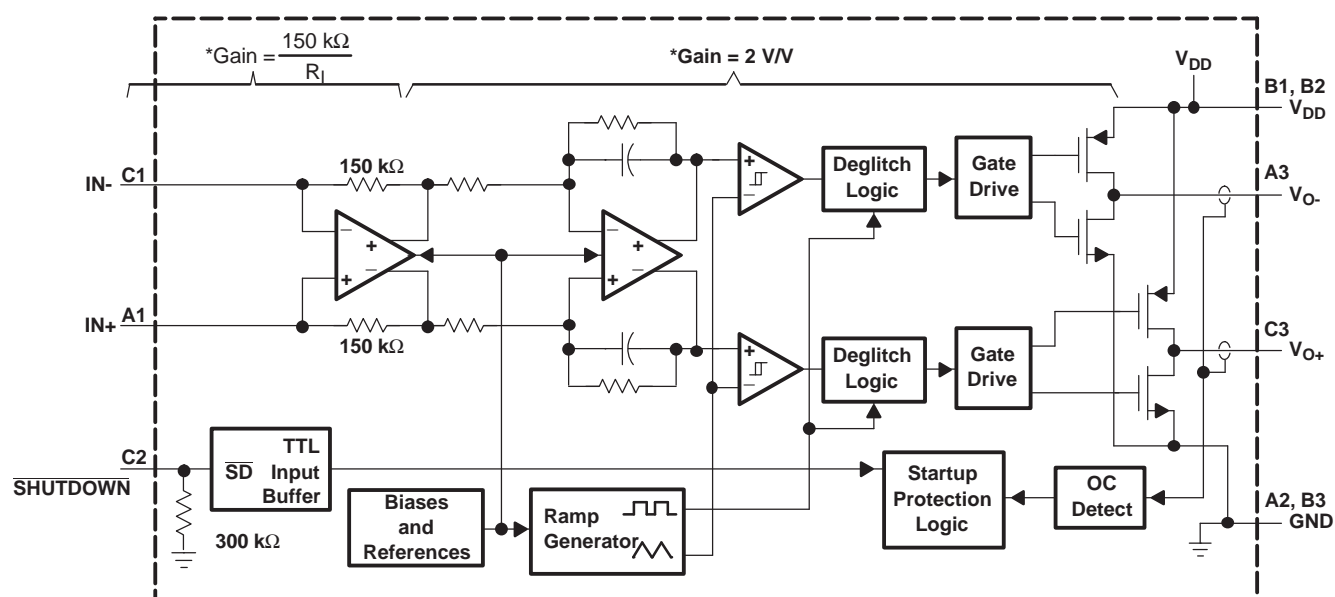
 $T_A = 25^\circ\text{C}$ , Gain = 2 V/V,  $R_L = 8\text{ }\Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P <sub>O</sub>	Output power	THD + N = 10%, f = 1 kHz, R <sub>L</sub> = 4 Ω	V <sub>DD</sub> = 5 V	2.5		W	
			V <sub>DD</sub> = 3.6 V	1.3			
			V <sub>DD</sub> = 2.5 V	0.52			
		THD + N = 1%, f = 1 kHz, R <sub>L</sub> = 4 Ω	V <sub>DD</sub> = 5 V	2.08		W	
			V <sub>DD</sub> = 3.6 V	1.06			
			V <sub>DD</sub> = 2.5 V	0.42			
		THD + N = 10%, f = 1 kHz, R <sub>L</sub> = 8 Ω	V <sub>DD</sub> = 5 V	1.45		W	
			V <sub>DD</sub> = 3.6 V	0.73			
			V <sub>DD</sub> = 2.5 V	0.33			
		THD + N = 1%, f = 1 kHz, R <sub>L</sub> = 8 Ω	V <sub>DD</sub> = 5 V	1.19		W	
			V <sub>DD</sub> = 3.6 V	0.59			
			V <sub>DD</sub> = 2.5 V	0.26			
THD+N	Total harmonic distortion plus noise	V <sub>DD</sub> = 5 V, P <sub>O</sub> = 1 W, R <sub>L</sub> = 8 Ω, f = 1 kHz		0.18%			
		V <sub>DD</sub> = 3.6 V, P <sub>O</sub> = 0.5 W, R <sub>L</sub> = 8 Ω, f = 1 kHz		0.19%			
		V <sub>DD</sub> = 2.5 V, P <sub>O</sub> = 200 mW, R <sub>L</sub> = 8 Ω, f = 1 kHz		0.20%			
k <sub>SVR</sub>	Supply ripple rejection ratio	V <sub>DD</sub> = 3.6 V, Inputs ac-grounded with C <sub>I</sub> = 2 μF	f = 217 Hz, V <sub>(RIPPLE)</sub> = 200 mV <sub>pp</sub>	–67		dB	
SNR	Signal-to-noise ratio	V <sub>DD</sub> = 5 V, P <sub>O</sub> = 1 W, R <sub>L</sub> = 8 Ω		97		dB	
V <sub>n</sub>	Output voltage noise	V <sub>DD</sub> = 3.6 V, f = 20 Hz to 20 kHz, Inputs ac-grounded with C <sub>I</sub> = 2 μF	No weighting	48		μV <sub>RMS</sub>	
			A weighting	36			
CMRR	Common mode rejection ratio	V <sub>DD</sub> = 3.6 V, V <sub>IC</sub> = 1 V <sub>pp</sub>	f = 217 Hz	–63		dB	
Z <sub>I</sub>	Input impedance			142	150	158	kΩ
	Start-up time from shutdown	V <sub>DD</sub> = 3.6 V		32		ms	

## Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	YZF		
IN–	C1	I	Negative differential input
IN+	A1	I	Positive differential input
V <sub>DD</sub>	B1	I	Power supply
V <sub>O+</sub>	C3	O	Positive BTL output
GND	A2, B3	I	High-current ground
V <sub>O–</sub>	A3	O	Negative BTL output
SHUTDOWN	C2	I	Shutdown terminal (active low logic)
PVDD	B2	I	Power supply

## FUNCTIONAL BLOCK DIAGRAM



Notes:

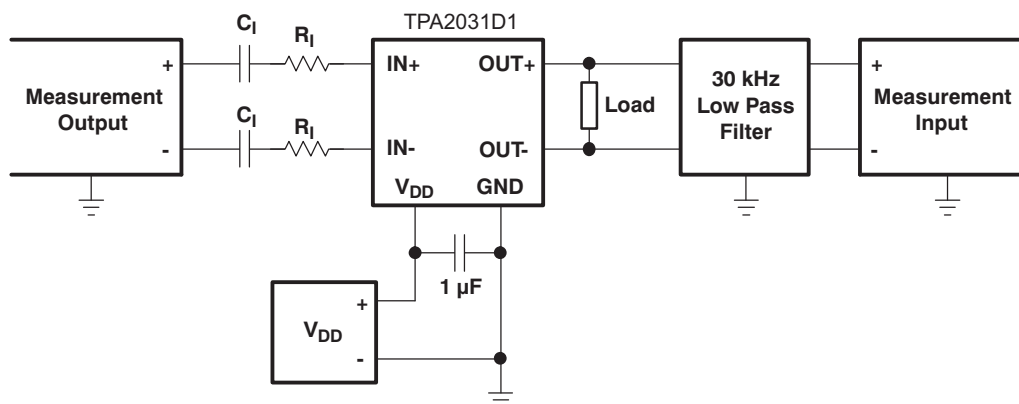
$$* \text{ Total gain} = 2 \times \frac{150 \text{ k}\Omega}{R_I}$$

## TYPICAL CHARACTERISTICS

### TABLE OF GRAPHS

			FIGURE
Efficiency	vs Output power		1, 2
$P_D$	Power dissipation	vs Output power	3, 4
Supply current	vs Output power		5, 6
$I_{(Q)}$	Quiescent current	vs Supply voltage	7
$I_{(SD)}$	Shutdown current	vs Shutdown voltage	8
$P_O$	Output power	vs Supply voltage	9
		vs Load resistance	10, 11
THD+N	Total harmonic distortion plus noise	vs Output power	12, 13
		vs Frequency	14, 15, 16, 17
		vs Common-mode input voltage	18
$K_{SVR}$	Supply voltage rejection ratio	vs Frequency	19, 20, 21
GSM	power supply rejection	vs Time	22
		vs Frequency	23
$K_{SVR}$	Supply voltage rejection ratio	vs Common-mode input voltage	24
CMRR	Common-mode rejection ratio	vs Frequency	25
		vs Common-mode input voltage	26
Voltage	vs Start-up time		27

### TEST SET-UP FOR GRAPHS



Notes:

- (1)  $C_1$  was Shorted for any Common-Mode input voltage measurement
- (2) A 33- $\mu$ H inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.
- (3) The 30-kHz low-pass filter is required even if the analyzer has an internal low-pass filter. An RC low pass filter (100  $\Omega$ , 47 nF) is used on each output for the data sheet graphs.

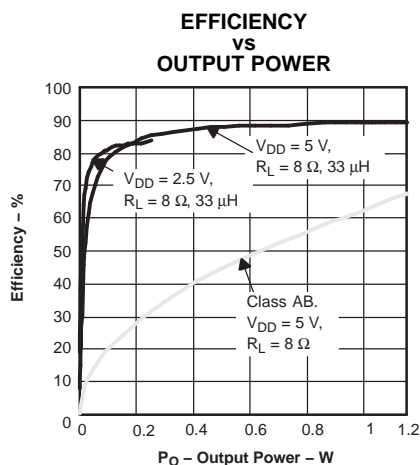


Figure 1.

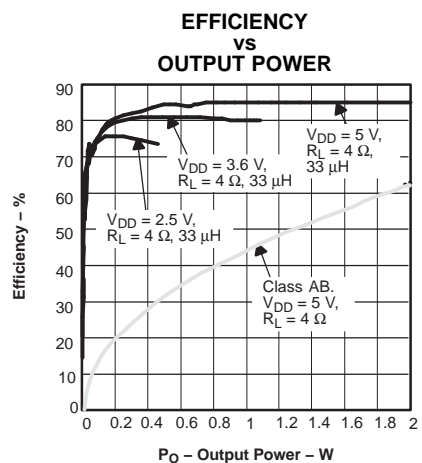


Figure 2.

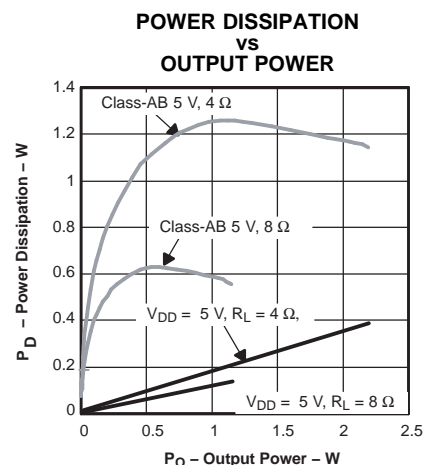


Figure 3.

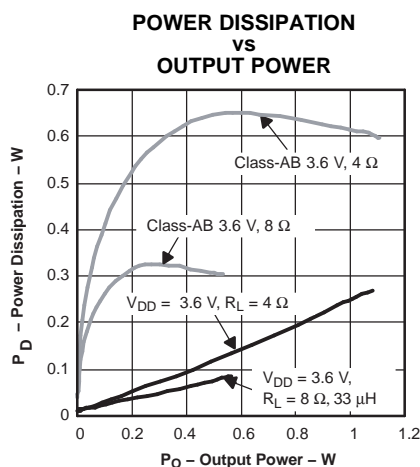


Figure 4.

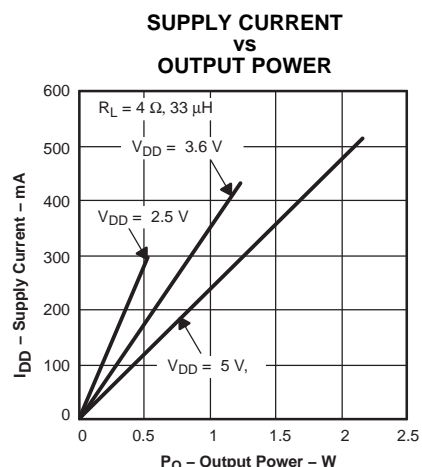


Figure 5.

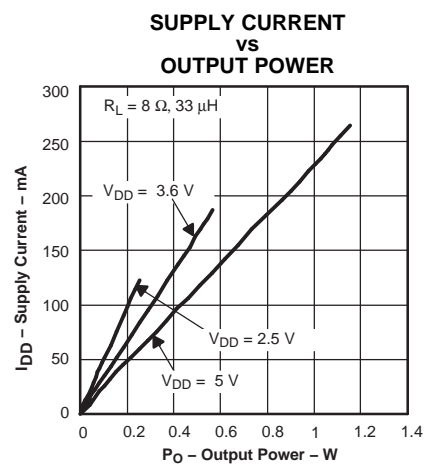


Figure 6.

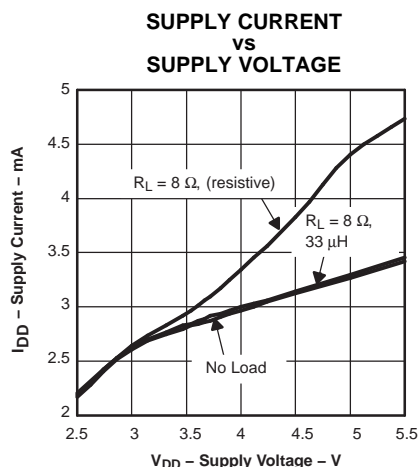


Figure 7.

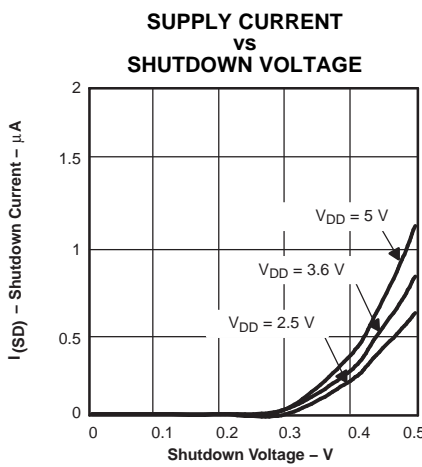


Figure 8.

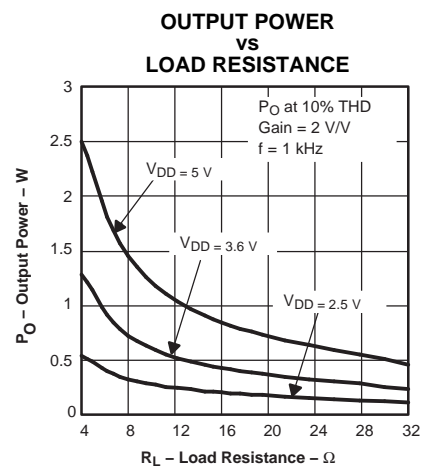


Figure 9.

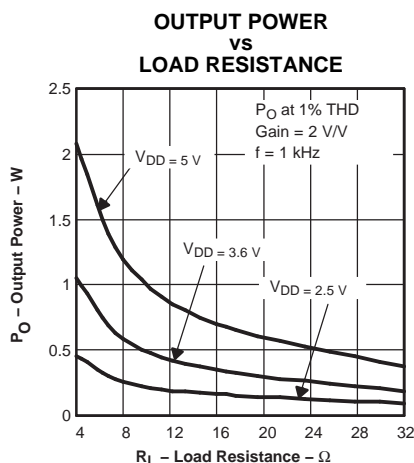


Figure 10.

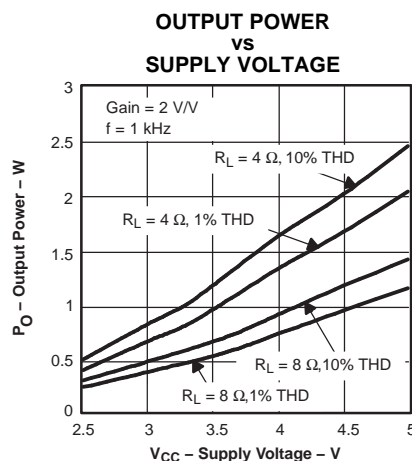


Figure 11.

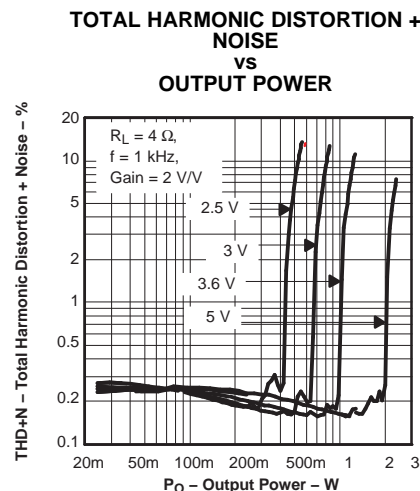


Figure 12.

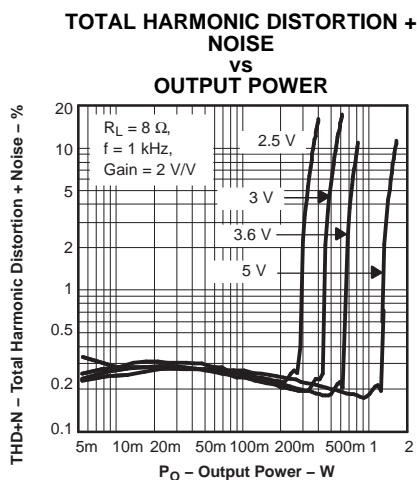


Figure 13.

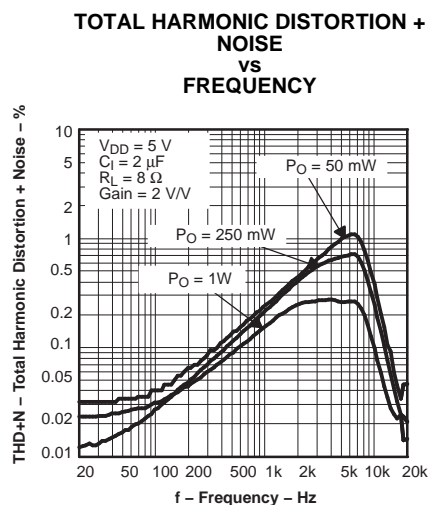


Figure 14.

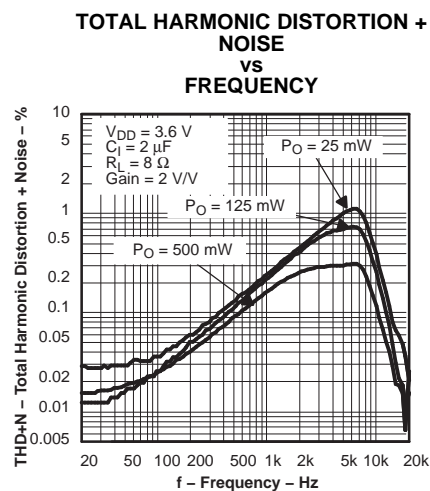


Figure 15.

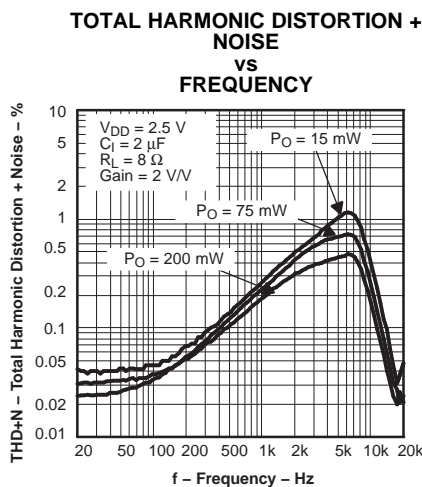


Figure 16.

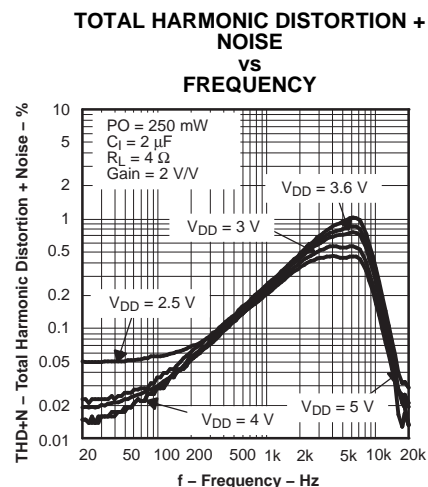


Figure 17.

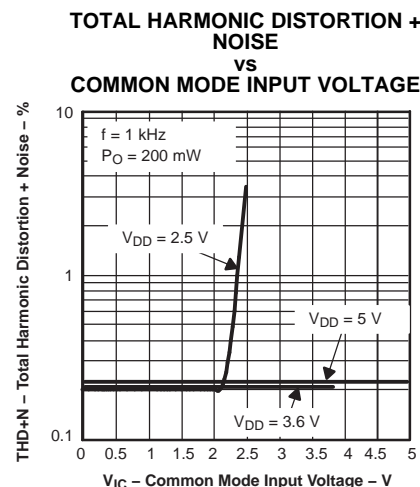


Figure 18.

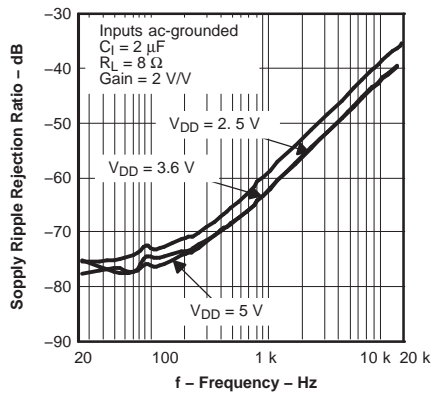
**SUPPLY RIPPLE REJECTION RATIO  
VS  
FREQUENCY**


Figure 19.

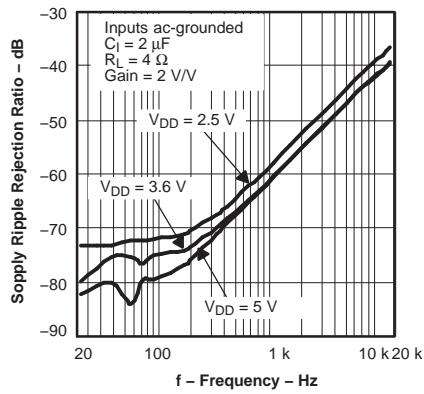
**SUPPLY RIPPLE REJECTION RATIO  
VS  
FREQUENCY**


Figure 20.

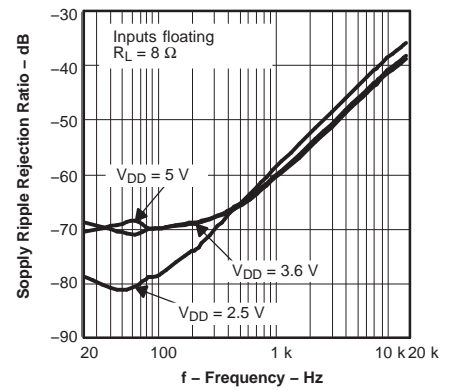
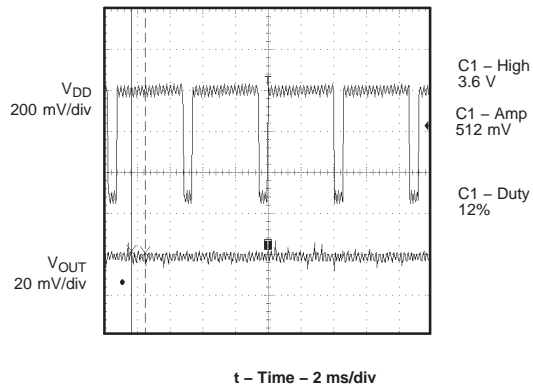
**SUPPLY RIPPLE REJECTION RATIO  
VS  
FREQUENCY**

**GSM POWER SUPPLY REJECTION  
VS  
TIME**


Figure 22.

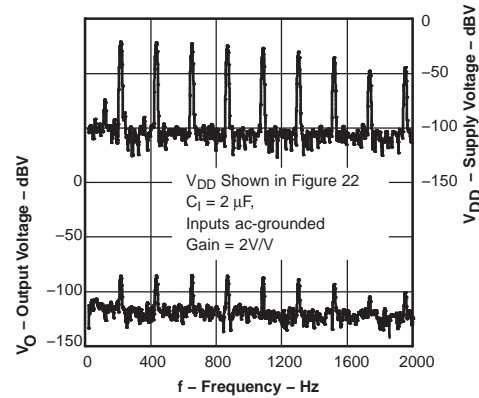
**GSM POWER SUPPLY REJECTION  
VS  
FREQUENCY**


Figure 23.

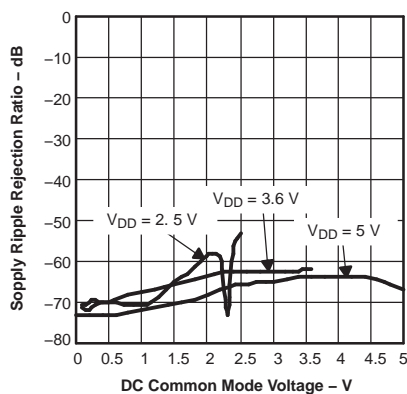
**SUPPLY RIPPLE REJECTION RATIO  
VS  
DC COMMON MODE VOLTAGE**


Figure 24.

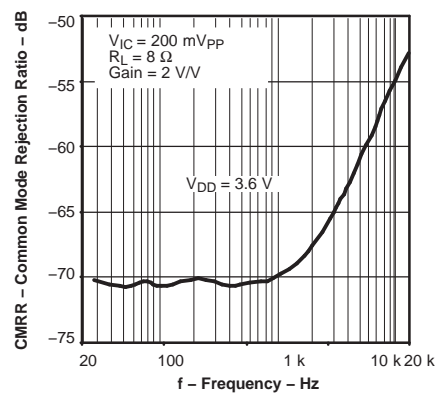
**COMMON-MODE REJECTION RATIO  
VS  
FREQUENCY**


Figure 25.

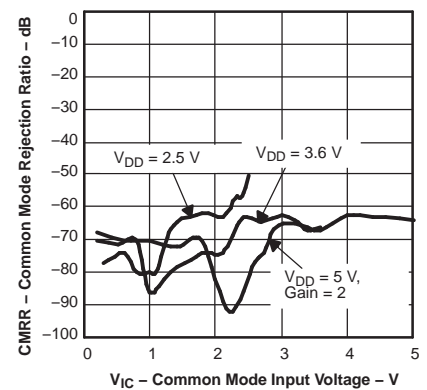
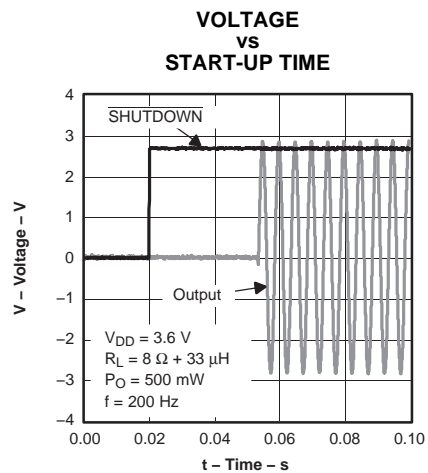
**COMMON-MODE REJECTION RATIO  
VS  
COMMON-MODE INPUT VOLTAGE**


Figure 26.





## APPLICATION INFORMATION

### FULLY DIFFERENTIAL AMPLIFIER

The TPA2031D1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around  $V_{DD}/2$  regardless of the common-mode voltage at the input. The fully differential TPA2031D1 can still be used with a single-ended input; however, the TPA2031D1 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

#### Advantages of Fully Differential Amplifiers

- Input-coupling capacitors not required:
  - The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply voltage. For example, if a codec has a mid-supply voltage lower than the mid-supply voltage of the TPA2031D1, the common-mode feedback circuit adjusts, and the TPA2031D1 outputs are still biased at mid-supply voltage of the TPA2031D1. The inputs of the TPA2031D1 can be biased from 0.5 V to  $V_{DD} - 0.8$  V. If the inputs are biased outside of that range, input-coupling capacitors are required.
- Mid-supply bypass capacitor,  $C_{(BYPASS)}$ , not required:
  - The fully differential amplifier does not require a bypass capacitor. This is because any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.
- Better RF-immunity:
  - GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

### COMPONENT SELECTION

Figure 28 shows the TPA2031D1 typical schematic with differential inputs and Figure 29 shows the TPA2031D1 with differential inputs and input capacitors, and Figure 30 shows the TPA2031D1 with single-ended inputs. Differential inputs should be used whenever possible because the single-ended inputs are much more susceptible to noise.

**Table 1. Typical Component Values**

REF DES	VALUE	EIA SIZE	MANUFACTURER	PART NUMBER
$R_I$	150 k $\Omega$ ( $\pm 0.5\%$ )	0402	Panasonic	ERJ2RHD154V
$C_S$	1 $\mu$ F (+22%, –80%)	0402	Murata	GRP155F50J105Z
$C_I^{(1)}$	3.3 nF ( $\pm 10\%$ )	0201	Murata	GRP033B10J332K

(1)  $C_I$  is only needed for single-ended input, or if  $V_{ICM}$  is not between 0.5 V and  $V_{DD} - 0.8$  V.  $C_I = 3.3$  nF (with  $R_I = 150$  k $\Omega$ ) gives a high-pass corner frequency of 321 Hz.

#### Input Resistors ( $R_I$ )

The input resistors ( $R_I$ ) set the gain of the amplifier according to Equation 1.

$$\text{Gain} = \frac{2 \times 150 \text{ k}\Omega}{R_I} \left( \frac{V}{V} \right) \quad (1)$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the TPA2031D1 to limit noise injection on the high-impedance nodes.

For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the TPA2031D1 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

### Decoupling Capacitor (C<sub>S</sub>)

The TPA2031D1 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device V<sub>DD</sub> lead works best. Placing this decoupling capacitor close to the TPA2031D1 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10 µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

### Input Capacitors (C<sub>I</sub>)

The TPA2031D1 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to V<sub>DD</sub> – 0.8 V (shown in Figure 28). If the input signal is not biased within the recommended common-mode input range, if needing to use the input as a high pass filter (shown in Figure 29), or if using a single-ended source (shown in Figure 30), input coupling capacitors are required.

The input capacitors and input resistors form a high-pass filter with the corner frequency, f<sub>c</sub>, determined in Equation 2.

$$f_c = \frac{1}{(2\pi \times R_I \times C_I)} \quad (2)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

Equation 3 is reconfigured to solve for the input coupling capacitance.

$$C_I = \frac{1}{(2\pi \times R_I \times f_c)} \quad (3)$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For a flat low-frequency response, use large input coupling capacitors (1 µF). However, in a GSM phone the ground signal is fluctuating at 217 Hz, but the signal from the codec does not have the same 217 Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217 Hz hum.

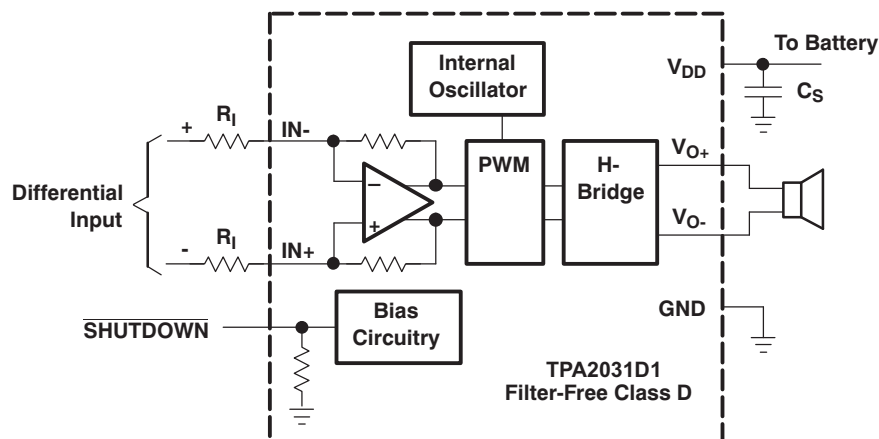
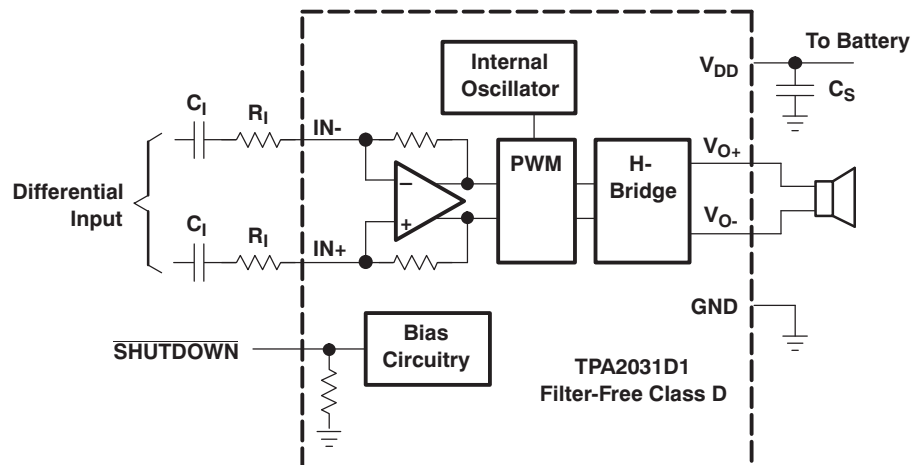
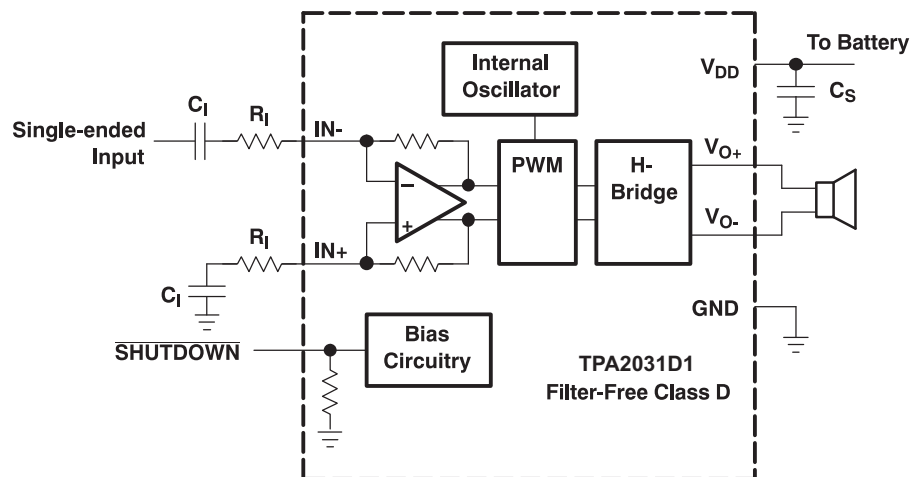


Figure 28. Typical TPA2031D1 Application Schematic With Differential Input for a Wireless Phone



**Figure 29. TPA2031D1 Application Schematic With Differential Input and Input Capacitors**



**Figure 30. TPA2031D1 Application Schematic With Single-Ended Input**

## SUMMING INPUT SIGNALS WITH THE TPA2031D1

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The TPA2031D1 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

### Summing Two Differential Input Signals

Two extra resistors are needed for summing differential signals (a total of 5 components). The gain for each input source can be set independently (see [Equation 4](#) and [Equation 5](#), and [Figure 31](#)).

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = \frac{2 \times 150 \text{ k}\Omega}{R_{I1}} \left( \frac{\text{V}}{\text{V}} \right) \quad (4)$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = \frac{2 \times 150 \text{ k}\Omega}{R_{I2}} \left( \frac{\text{V}}{\text{V}} \right) \quad (5)$$

If summing left and right inputs with a gain of 1 V/V, use  $R_{I1} = R_{I2} = 300 \text{ k}\Omega$ .

If summing a ring tone and a phone signal, set the ring-tone gain to Gain 2 = 2 V/V, and the phone gain to gain 1 = 0.1 V/V. The resistor values would be. . .

$R_{I1} = 3 \text{ M}\Omega$ , and  $R_{I2} = 150 \text{ k}\Omega$ .

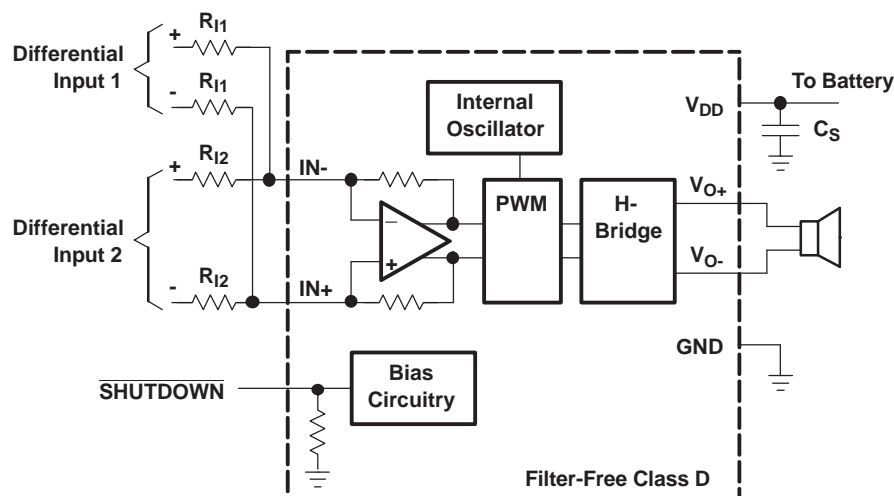


Figure 31. Application Schematic With TPA2031D1 Summing Two Differential Inputs

### Summing a Differential Input Signal and a Single-Ended Input Signal

Figure 32 shows how to sum a differential input signal and a single-ended input signal. Ground noise can couple in through IN+ with this method. It is better to use differential inputs. The corner frequency of the single-ended input is set by  $C_{I2}$ , shown in Equation 8. To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = \frac{2 \times 150 \text{ k}\Omega}{R_{I1}} \left( \frac{\text{V}}{\text{V}} \right) \quad (6)$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = \frac{2 \times 150 \text{ k}\Omega}{R_{I2}} \left( \frac{\text{V}}{\text{V}} \right) \quad (7)$$

$$C_{I2} = \frac{1}{(2\pi R_{I2} f_{c2})} \quad (8)$$

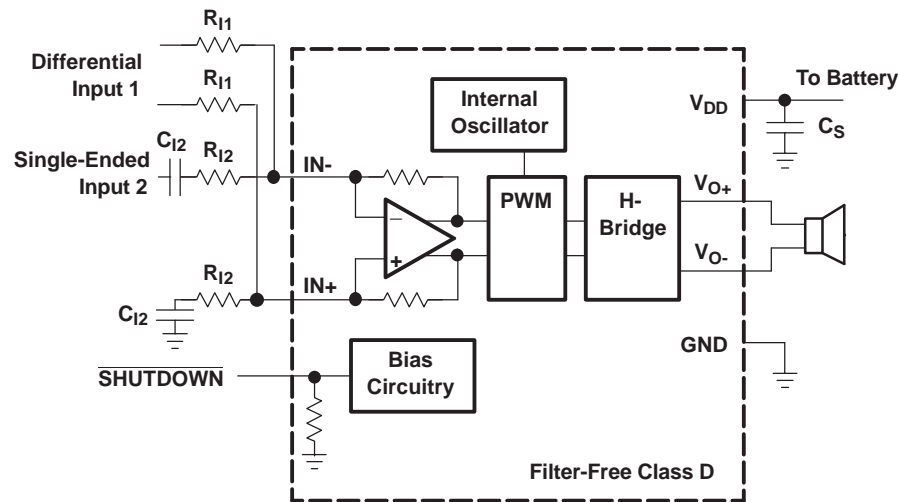
If summing a ring tone and a phone signal, the phone signal should use a differential input signal while the ring tone might be limited to a single-ended signal. Phone gain is set at gain 1 = 0.1 V/V, and the ring-tone gain is set to gain 2 = 2 V/V, the resistor values would be...

$R_{I1} = 3 \text{ M}\Omega$ , and  $R_{I2} = 150 \text{ k}\Omega$ .

The high pass corner frequency of the single-ended input is set by  $C_{I2}$ . If the desired corner frequency is less than 20 Hz...

$$C_{I2} > \frac{1}{(2\pi \cdot 150\text{k}\Omega \cdot 20\text{Hz})} \quad (9)$$

$$C_{I2} > 53 \text{ nF} \quad (10)$$



**Figure 32. Application Schematic With TPA2031D1 Summing Differential Input and Single-Ended Input Signals**

### Summing Two Single-Ended Input Signals

Four resistors and three capacitors are needed for summing single-ended input signals. The gain and corner frequencies ( $f_{c1}$  and  $f_{c2}$ ) for each input source can be set independently (see [Equation 11](#) through [Equation 14](#), and [Figure 33](#)). Resistor,  $R_P$ , and capacitor,  $C_P$ , are needed on the IN+ terminal to match the impedance on the IN- terminal. The single-ended inputs must be driven by low impedance sources even if one of the inputs is not outputting an ac signal.

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = \frac{2 \times 150 \text{ k}\Omega}{R_{I1}} \left( \frac{\text{V}}{\text{V}} \right) \quad (11)$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = \frac{2 \times 150 \text{ k}\Omega}{R_{I2}} \left( \frac{\text{V}}{\text{V}} \right) \quad (12)$$

$$C_{I1} = \frac{1}{(2\pi R_{I1} f_{c1})} \quad (13)$$

$$C_{I2} = \frac{1}{(2\pi R_{I2} f_{c2})} \quad (14)$$

$$C_P = C_{I1} + C_{I2} \quad (15)$$

$$R_P = \frac{R_{I1} \times R_{I2}}{(R_{I1} + R_{I2})} \quad (16)$$

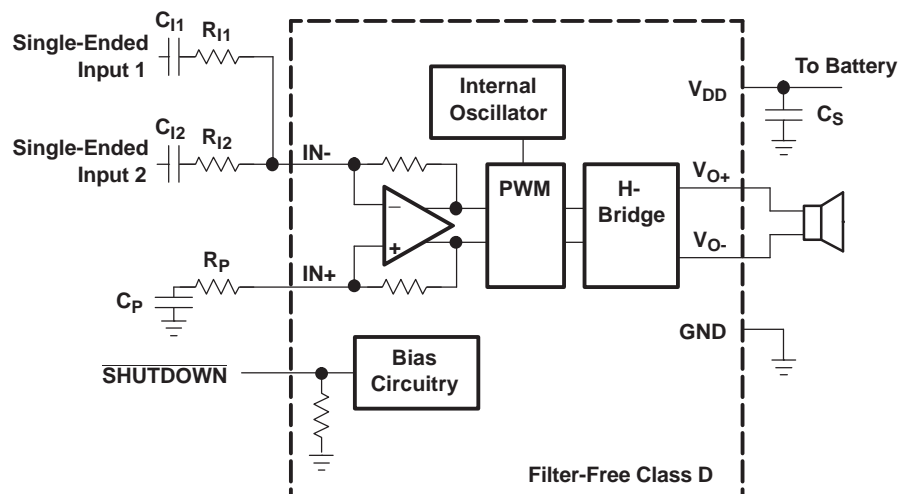


Figure 33. Application Schematic With TPA2031D1 Summing Two Single-Ended Inputs

## BOARD LAYOUT

In making the pad size for the WCSP balls, it is recommended that the layout use non-solder-mask-defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 34 and Table 2 show the appropriate diameters for a WCSP layout. The TPA2031D1 evaluation module (EVM) layout is shown in the next section as a layout example.

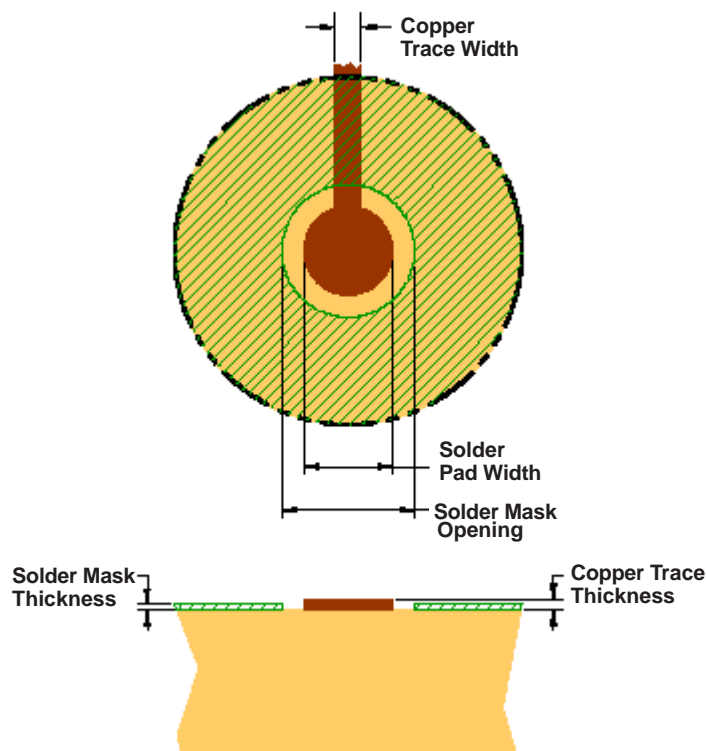


Figure 34. Land Pattern Dimensions

**Table 2. Land Pattern Dimensions**

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK OPENING	COPPER THICKNESS	STENCIL OPENING	STENCIL THICKNESS
Non-solder-mask defined (NSMD)	275 $\mu\text{m}$ (+0.0, -25 $\mu\text{m}$ )	375 $\mu\text{m}$ (+0.0, -25 $\mu\text{m}$ )	1 oz max (32 $\mu\text{m}$ )	275 $\mu\text{m}$ x 275 $\mu\text{m}$ Sq. (rounded corners)	125 $\mu\text{m}$ thick

**NOTES:**

1. Circuit traces from NSMD defined PWB lands should be 75  $\mu\text{m}$  to 100  $\mu\text{m}$  wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
2. Recommend solder paste is Type 3 or Type 4.
3. Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
4. For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5  $\mu\text{m}$  to avoid a reduction in thermal fatigue performance.
5. Solder mask thickness should be less than 20  $\mu\text{m}$  on top of the copper circuit pattern.
6. Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
7. Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

**Component Location**

Place all the external components very close to the TPA2031D1. The input resistors need to be very close to the TPA2031D1 input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the TPA2031D1. Placing the decoupling capacitor, CS, close to the TPA2031D1 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

**Trace Width**

Recommended trace width at the solder balls is 75  $\mu\text{m}$  to 100  $\mu\text{m}$  to prevent solder wicking onto wider PCB traces. [Figure 35](#) shows the layout of the TPA2031D1 evaluation module (EVM).

For high current pins ( $V_{DD}$ , GND,  $V_{O+}$ , and  $V_{O-}$ ) of the TPA2031D1, use 100- $\mu\text{m}$  trace widths at the solder balls and at least 500- $\mu\text{m}$  PCB traces to ensure proper performance and output power for the device.

For input pins (IN $_{-}$ , IN $_{+}$ , and SHUTDOWN) of the TPA2031D1, use 75- $\mu\text{m}$  to 100- $\mu\text{m}$  trace widths at the solder balls. IN $_{-}$  and IN $_{+}$  pins need to run side-by-side to maximize common-mode noise cancellation. Placing input resistors, R $_{IN}$ , as close to the TPA2031D1 as possible is recommended.



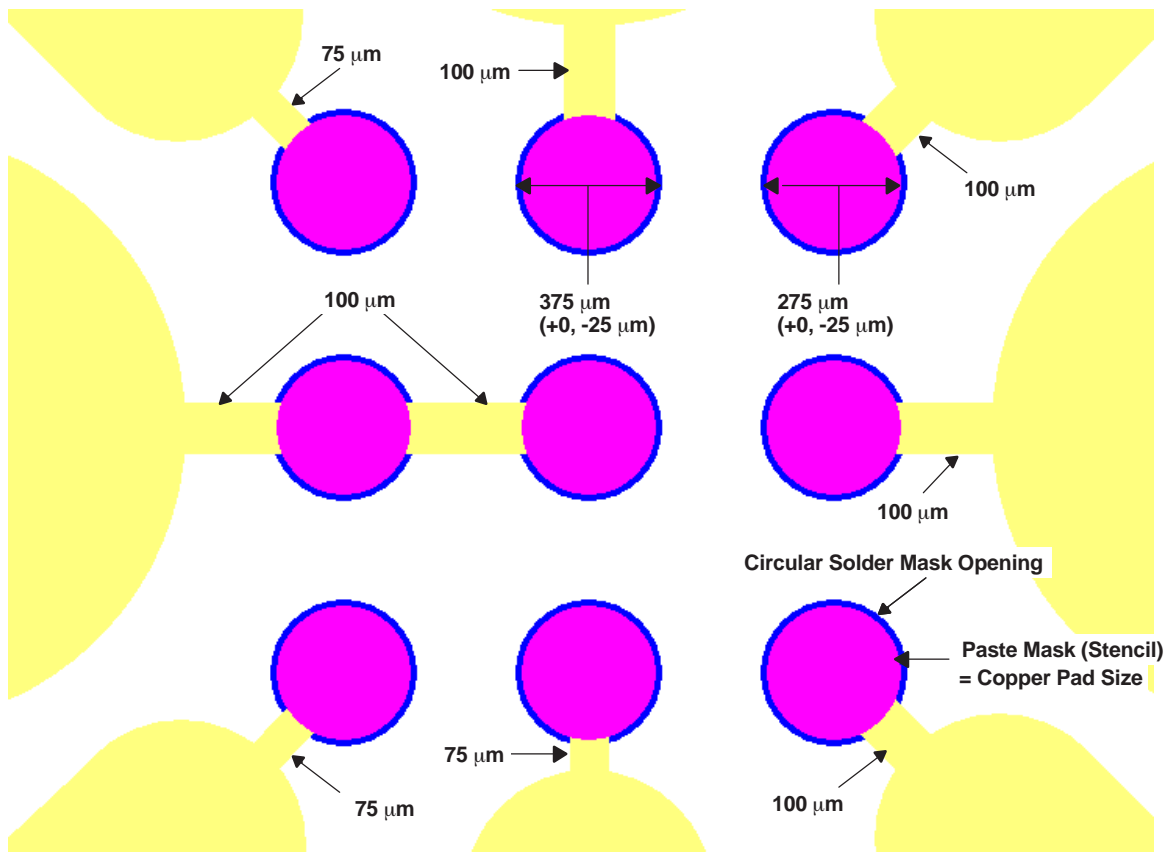


Figure 35. Close Up of TPA2031D1 Land Pattern From TPA2031D1 EVM

## EFFICIENCY AND THERMAL INFORMATION

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the YZF package is shown in the dissipation rating table. Converting this to  $\theta_{JA}$ :

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.0078} = 128.2^{\circ}\text{C/W} \quad (17)$$

Given  $\theta_{JA}$  of 128.2°C/W, the maximum allowable junction temperature of 150°C, and the maximum internal dissipation of 0.4 W (2.25 W, 4-Ω load, 5-V supply, from Figure 3), the maximum ambient temperature can be calculated with the following equation.

$$T_{A\text{Max}} = T_{J\text{Max}} - \theta_{JA} P_{D\text{max}} = 150 - 128.2 (0.4) = 98.72^{\circ}\text{C} \quad (18)$$

Equation 18 shows that the calculated maximum ambient temperature is 98.7°C at maximum power dissipation with a 5-V supply and 4-Ω a load, see Figure 3. The TPA2031D1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using speakers more resistive than 4-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

## ELIMINATING THE OUTPUT FILTER WITH THE TPA2031D1

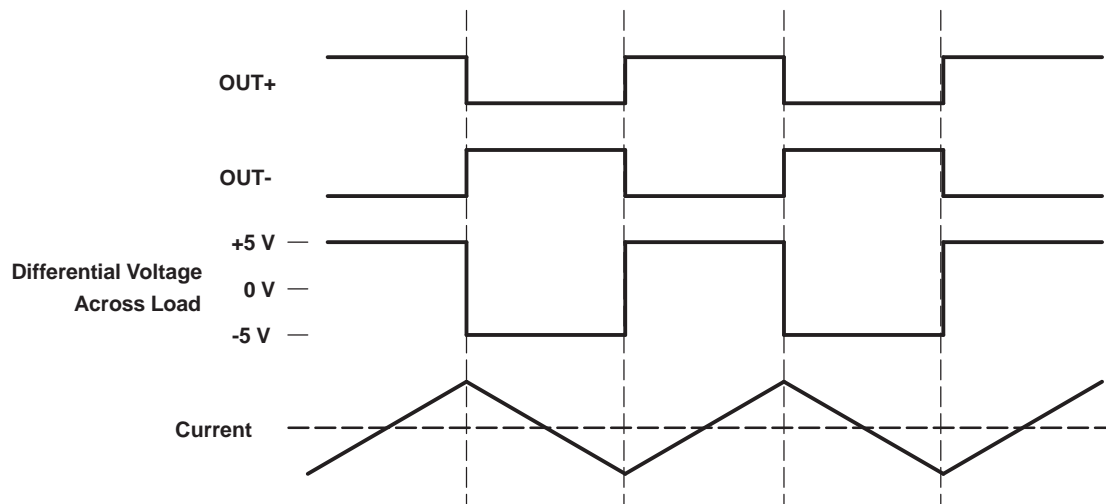
This section focuses on why the user can eliminate the output filter with the TPA2031D1.

## Effect on Audio

The class-D amplifier outputs a pulse-width modulated (PWM) square wave that is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

## Traditional Class-D Modulation Scheme

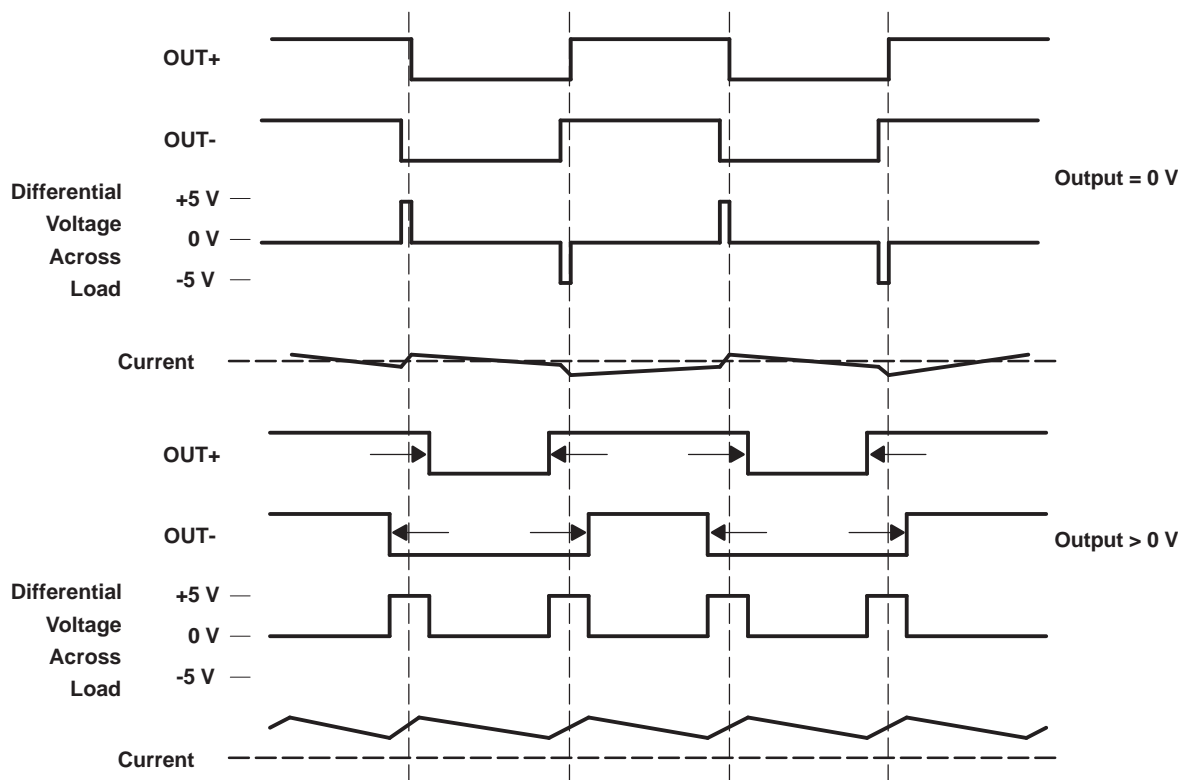
The traditional class-D modulation scheme, which is used in the TPA005Dxx family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage,  $V_{DD}$ . Therefore, the differential pre-filtered output varies between positive and negative  $V_{DD}$ , where filtered 50% duty cycle yields 0 volts across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 36. Note that even at an average of 0 volts across the load (50% duty cycle), the current to the load is high causing a high loss and thus causing a high supply current.



**Figure 36. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With no Input**

## TPA2031D1 Modulation Scheme

The TPA2031D1 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUT+ and OUT- are now in phase with each other with no input. The duty cycle of OUT+ is greater than 50% and OUT- is less than 50% for positive voltages. The duty cycle of OUT+ is less than 50% and OUT- is greater than 50% for negative voltages. The voltage across the load sits at 0 volts throughout most of the switching period greatly reducing the switching current, which reduces any  $I^2R$  losses in the load.



**Figure 37. The TPA2031D1 Output Voltage and Current Waveforms Into an Inductive Load**

### Efficiency: Why You Must Use a Filter With the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is  $2 \times V_{DD}$  and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA2031D1 modulation scheme has very little loss in the load without a filter because the pulses are very short and the change in voltage is  $V_{DD}$  instead of  $2 \times V_{DD}$ . As the output power increases, the pulses widen making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker that results in less power dissipated, which increases efficiency.

### Effects of Applying a Square Wave Into a Speaker

If the amplitude of a square wave is high enough and the frequency of the square wave is within the bandwidth of the speaker, a square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, is not significant because the speaker cone movement is proportional to  $1/f^2$  for frequencies beyond the audio band. Therefore, the amount of cone movement at the switching frequency is very small. However, damage could occur to the speaker if the voice coil is not designed to handle the additional power. To size the speaker for added power, the ripple current dissipated in the load needs to be calculated by subtracting the theoretical supplied power,  $P_{SUP, THEORETICAL}$ , from the actual supply power,  $P_{SUP}$ , at maximum output power,  $P_{OUT}$ . The switching power dissipated in the speaker is the inverse of the measured efficiency,  $\eta_{MEASURED}$ , minus the theoretical efficiency,  $\eta_{THEORETICAL}$ .

$$P_{\text{SPKR}} = P_{\text{SUP}} - P_{\text{SUP THEORETICAL}} \quad (\text{at max output power}) \quad (19)$$

$$P_{\text{SPKR}} = \frac{P_{\text{SUP}}}{P_{\text{OUT}}} - \frac{P_{\text{SUP THEORETICAL}}}{P_{\text{OUT}}} \quad (\text{at max output power}) \quad (20)$$

$$P_{\text{SPKR}} = P_{\text{OUT}} \left( \frac{1}{\eta_{\text{MEASURED}}} - \frac{1}{\eta_{\text{THEORETICAL}}} \right) \quad (\text{at max output power}) \quad (21)$$

$$\eta_{\text{THEORETICAL}} = \frac{R_L}{R_L + 2r_{\text{DS(on)}}} \quad (\text{at max output power}) \quad (22)$$

The maximum efficiency of the TPA2031D1 with a 3.6 V supply and an 8-Ω load is 86% from Equation 22. Using equation Equation 21 with the efficiency at maximum power (84%), we see that there is an additional 17 mW dissipated in the speaker. The added power dissipated in the speaker is not an issue as long as it is taken into account when choosing the speaker.

### When to Use an Output Filter

Design the TPA2031D1 without an output filter if the traces from amplifier to speaker are short. The TPA2031D1 passed FCC and CE radiated emissions with no shielding with speaker trace wires 100 mm long or less. Wireless handsets and PDAs are great applications for class-D without a filter.

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter, and the frequency sensitive circuit is greater than 1 MHz. This is good for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

Figure 38 and Figure 39 show typical ferrite bead and LC output filters.

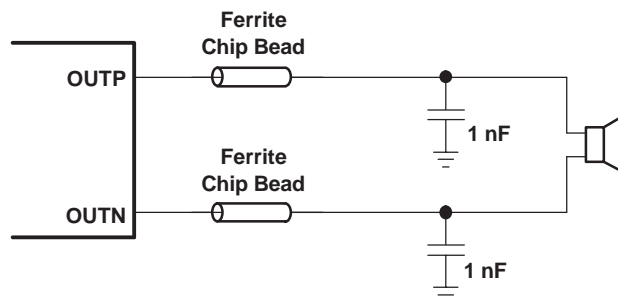


Figure 38. Typical Ferrite Chip Bead Filter (Chip bead example: NEC/Tokin: N2012ZPS121)

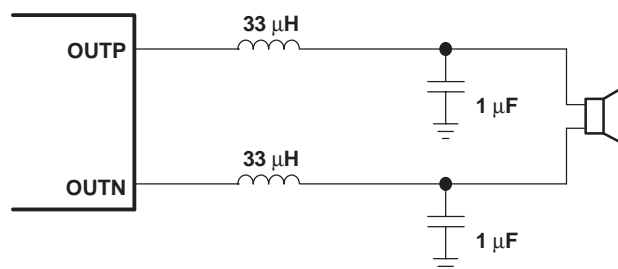


Figure 39. Typical LC Output Filter, Cutoff Frequency of 27 kHz

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPA2031D1YZFR</a>	Active	Production	DSBGA (YZF)   9	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CEI
TPA2031D1YZFR.B	Active	Production	DSBGA (YZF)   9	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CEI
<a href="#">TPA2031D1YZFT</a>	Active	Production	DSBGA (YZF)   9	250   SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CEI
TPA2031D1YZFT.B	Active	Production	DSBGA (YZF)   9	250   SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CEI

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2031D1YZFR	DSBGA	YZF	9	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
TPA2031D1YZFT	DSBGA	YZF	9	250	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2031D1YZFR	DSBGA	YZF	9	3000	182.0	182.0	20.0
TPA2031D1YZFT	DSBGA	YZF	9	250	182.0	182.0	20.0



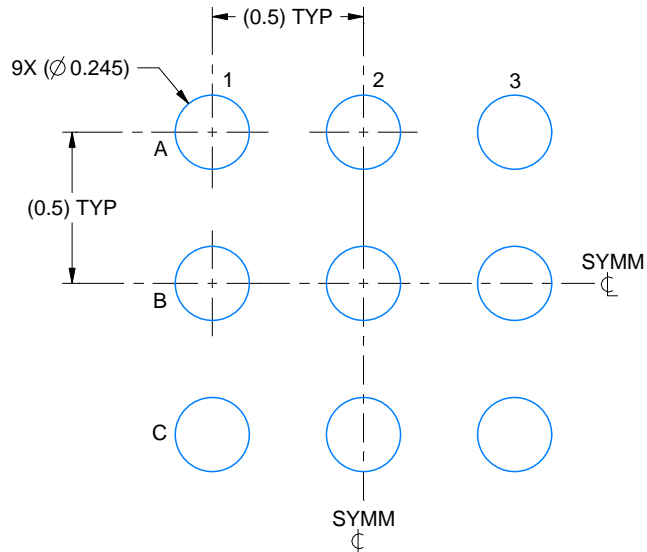


# EXAMPLE BOARD LAYOUT

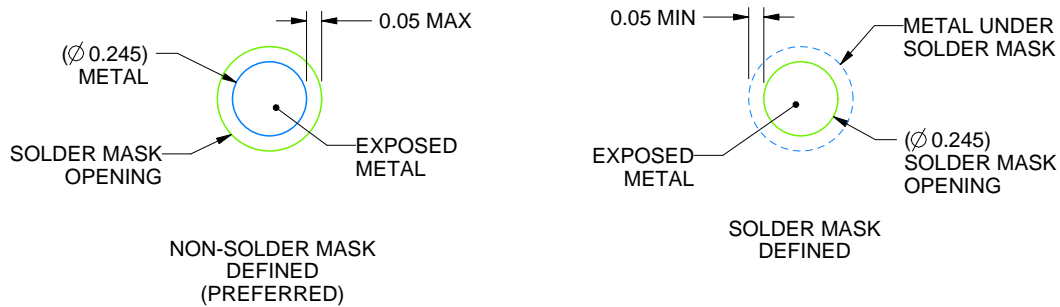
YZF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219558/A 10/2018

NOTES: (continued)

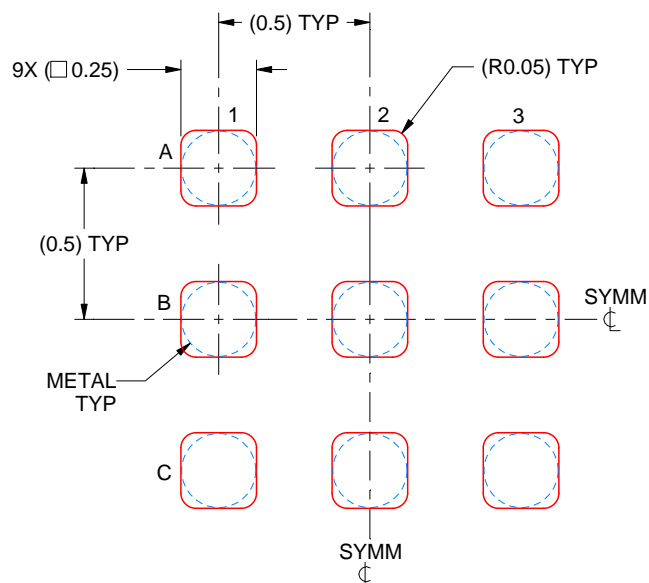
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

## EXAMPLE STENCIL DESIGN

YZF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 40X

4219558/A 10/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated