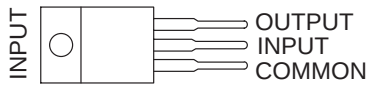
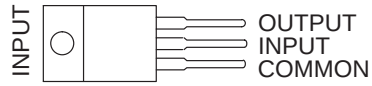
SLVS060K − JUNE 1976 − REVISED APRIL 2005

- **3-Terminal Regulators**
- **Output Current Up To 500 mA**
- **No External Components**
- **High Power-Dissipation Capability**
- **Internal Short-Circuit Current Limiting**
- **Output Transistor Safe-Area Compensation**

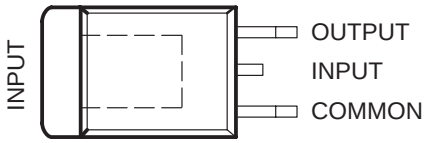
μA79M05 . . . KC (TO-220) PACKAGE
(TOP VIEW)



μA79M05 . . . KCS (TO-220) PACKAGE
(TOP VIEW)



μA79M05, μA79M08 . . . KTP PACKAGE
(TOP VIEW)



description/ordering information

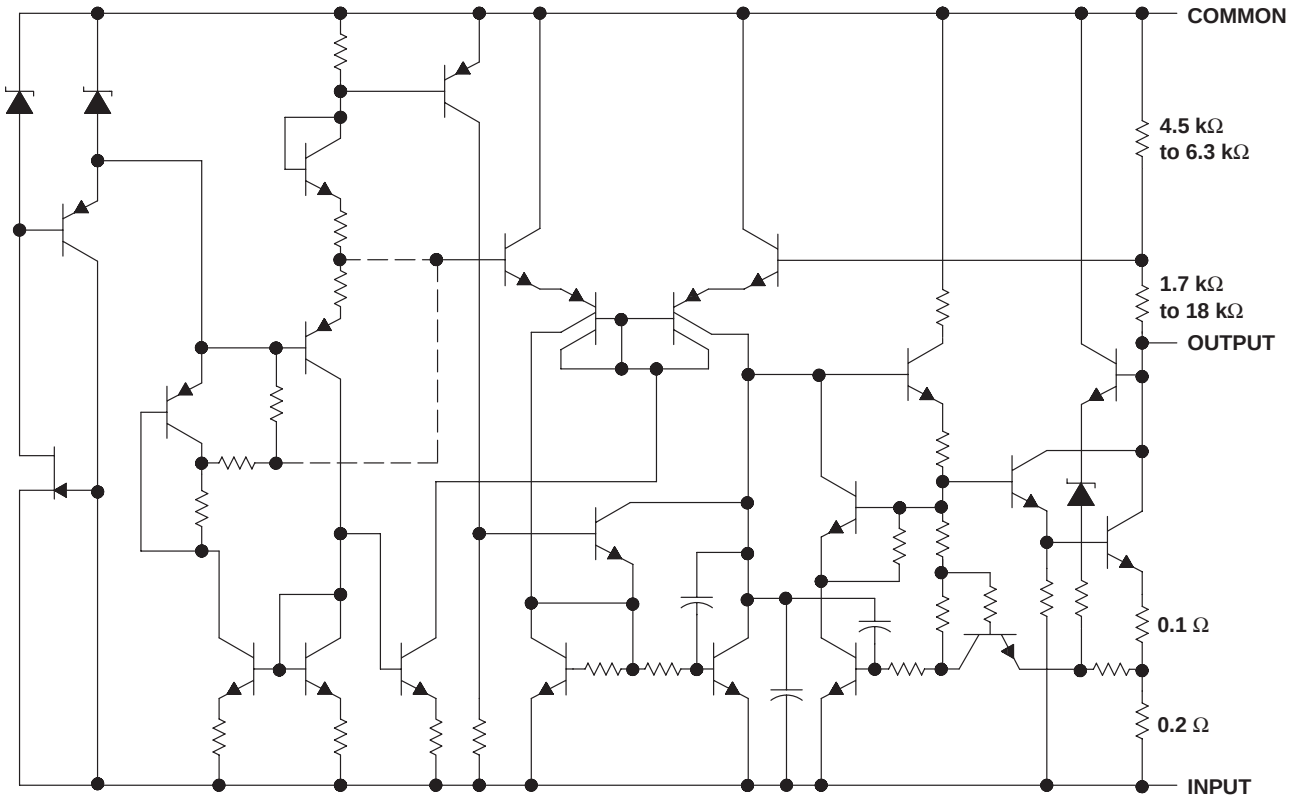
This series of fixed-negative-voltage integrated-circuit voltage regulators is designed to complement the μA78M00 series in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators delivers up to 500 mA of output current. The internal current-limiting and thermal-shutdown features of these regulators essentially make them immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents, and also as the power-pass element in precision regulators.

ORDERING INFORMATION

T_J	V_O(NOM) (V)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	−5	PowerFLEX™ (KTP)	Reel of 3000	μA79M05CKTPR	μA79M05C
		TO-220 (KC)	Tube of 50	μA79M05CKC	μA79M05C
		TO-220, short shoulder (KCS)	Tube of 20	μA79M05CKCS	
	−8	PowerFLEX (KTP)	Reel of 3000	μA79M08CKTPR	μA79M08C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematic



Resistor values shown are nominal.

absolute maximum ratings over virtual junction temperature range (unless otherwise noted)†

Input voltage, V_I	35 V
Operating virtual junction temperature, T_J	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

package thermal data (see Note 1)

PACKAGE	BOARD	θ_{JC}	θ_{JA}	θ_{JP}‡
PowerFLEX (KTP)	High K, JESD 51-5	19°C/W	28°C/W	1.4°C/W
TO-220 (KC/KCS)	High K, JESD 51-5	17°C/W	19°C/W	3°C/W

NOTE 1: Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

‡ For packages with exposed thermal pads, such as QFN, PowerPAD, or PowerFLEX, θ_{JP} is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

recommended operating conditions

			MIN	MAX	UNIT
V_I	Input voltage	μA79M05C	−7	−25	V
		μA79M08C	−10.5	−25	
I_O	Output current			500	mA
T_J	Operating virtual junction temperature		0	125	°C

electrical characteristics at specified virtual junction temperature, V_I = −10 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			μA79M05C			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = −7 V to −25 V,	I_O = 5 mA to 350 mA		−4.8	−5	−5.2	V
			T_J = 0°C to 125°C	−4.75		−5.25	
Input voltage regulation	V_I = −7 V to −25 V				7	50	mV
	V_I = −8 V to −18 V				3	30	
Ripple rejection	V_I = −8 V to −18 V, f = 120 Hz	I_O = 100 mA,	T_J = 0°C to 125°C	50			dB
		I_O = 300 mA		54	60		
Output voltage regulation	I_O = 5 mA to 500 mA				75	100	mV
	I_O = 5 mA to 350 mA				50		
Temperature coefficient of output voltage	I_O = 5 mA,	T_J = 0°C to 125°C			−0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz				125		μV
Dropout voltage					1.1		V
Bias current					1	2	mA
Bias current change	V_I = −8 V to −18 V,	T_J = 0°C to 125°C				0.4	mA
	I_O = 5 mA to 350 mA,	T_J = 0°C to 125°C				0.4	
Short-circuit output current	V_I = −30 V				140		mA
Peak output current					0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, V_I = −19 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			μA79M08C			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = −10.5 V to −25 V,	I_O = 5 mA to 350 mA		−7.7	−8	−8.3	V
			T_J = 0°C to 125°C	−7.6		−8.4	
Input voltage regulation	V_I = −10.5 V to −25 V				8	80	mV
	V_I = −11 V to −21 V				4	50	
Ripple rejection	V_I = −11.5 V to −21.5 V, f = 120 Hz	I_O = 100 mA,	T_J = 0°C to 125°C	50			dB
		I_O = 300 mA		54	59		
Output voltage regulation	I_O = 5 mA to 500 mA				90	160	mV
	I_O = 5 mA to 350 mA				60		
Temperature coefficient of output voltage	I_O = 5 mA,	T_J = 0°C to 125°C			−0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz				200		μV
Dropout voltage	I_O = 5 mA				1.1		V
Bias current					1	2	mA
Bias current change	V_I = −10.5 V to −25 V,	T_J = 0°C to 125°C				0.4	mA
	I_O = 5 mA to 350 mA,	T_J = 0°C to 125°C				0.4	
Short-circuit output current	V_I = −30 V				140		mA
Peak output current					0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
7704001HA	OBSOLETE	CFP	U	10		TBD	Call TI	Call TI	-55 to 125		
UA79M05CKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	0 to 125	UA79M05C	
UA79M05CKCE3	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	0 to 125	UA79M05C	
UA79M05CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA79M05C	Samples
UA79M05CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA79M05C	Samples
UA79M05CKTPR	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI	0 to 125	UA79M05C	
UA79M05CKTPRG3	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI	0 to 125	UA79M05C	
UA79M05CKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	79M05C	Samples
UA79M05MUB	OBSOLETE	CFP	U	10		TBD	Call TI	Call TI	-55 to 125		
UA79M08CKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	0 to 125		
UA79M08CKTPR	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI	0 to 125	UA79M08C	
UA79M08CKTPRG3	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI	0 to 125	UA79M08C	
UA79M08CKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	79M08C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

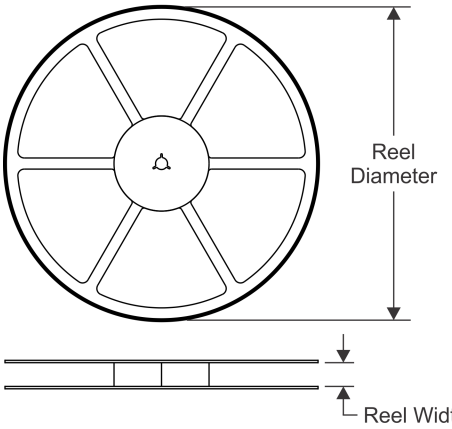
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

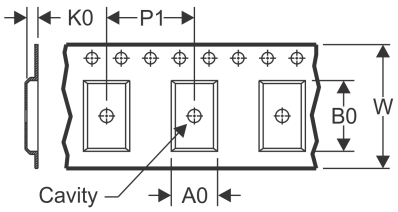
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

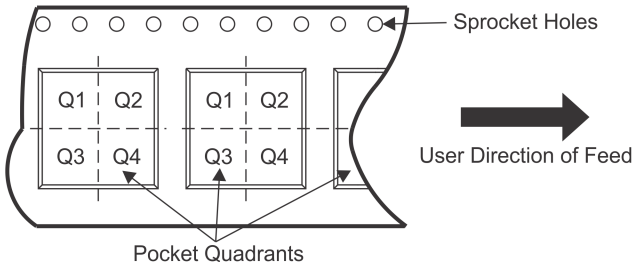


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

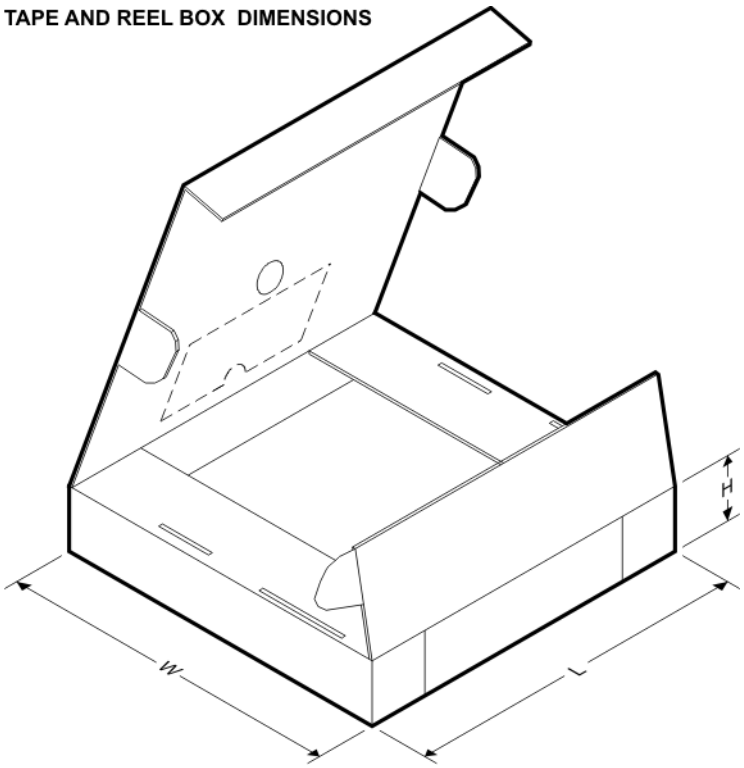
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA79M05CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
UA79M08CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

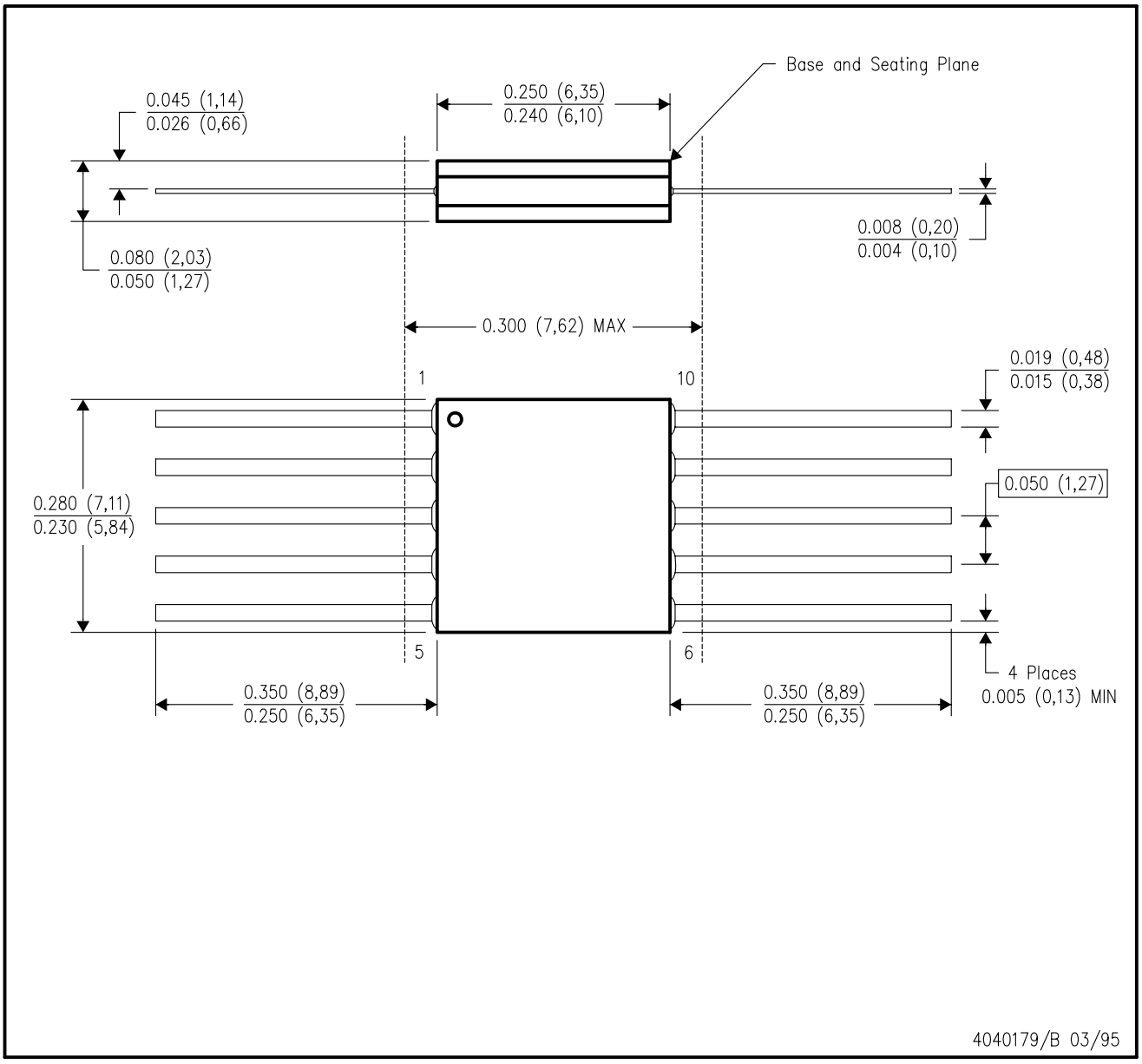
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA79M05CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
UA79M08CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0

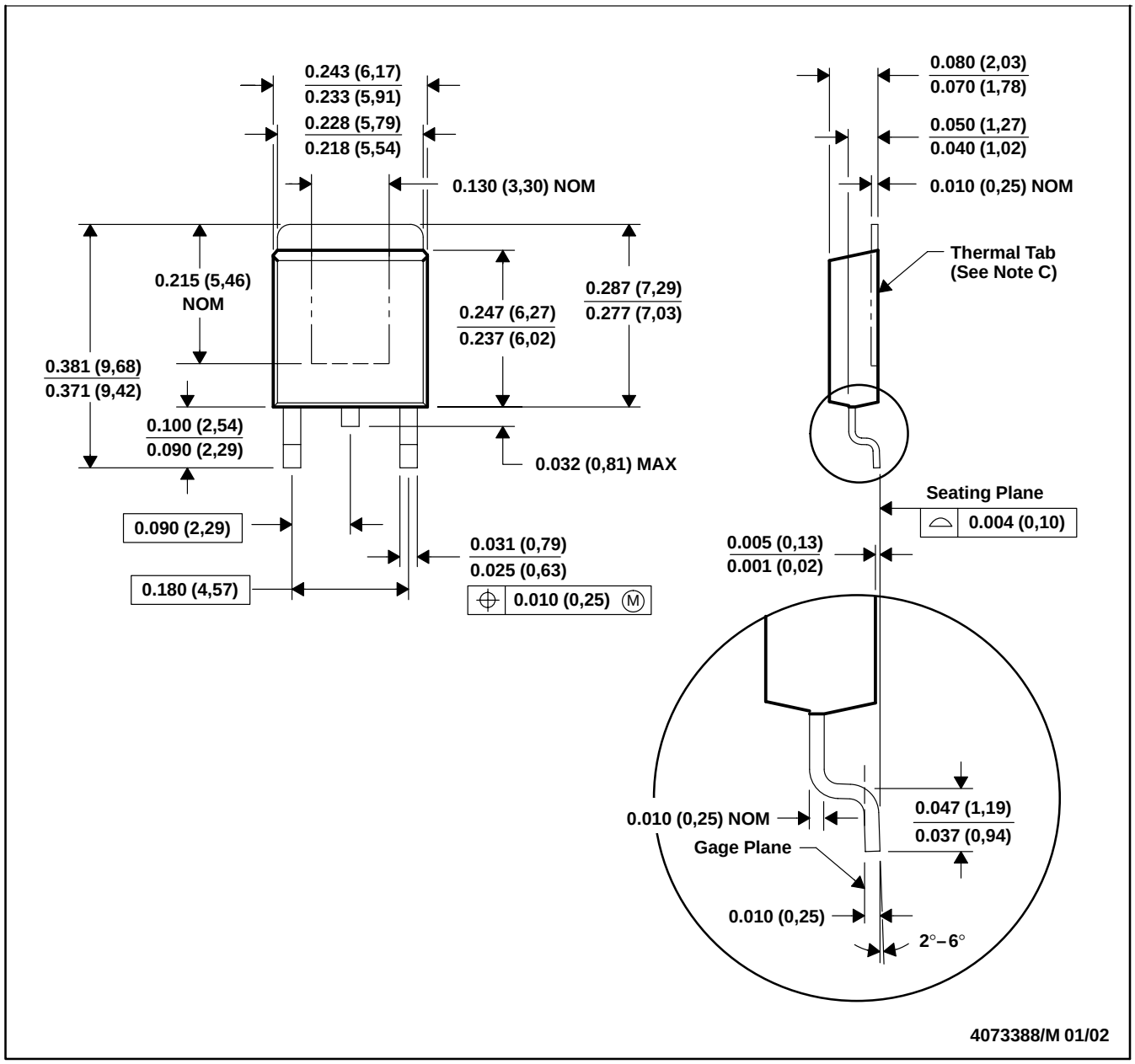
U (S–GDFP–F10) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

MPSF001F – JANUARY 1996 – REVISED JANUARY 2002

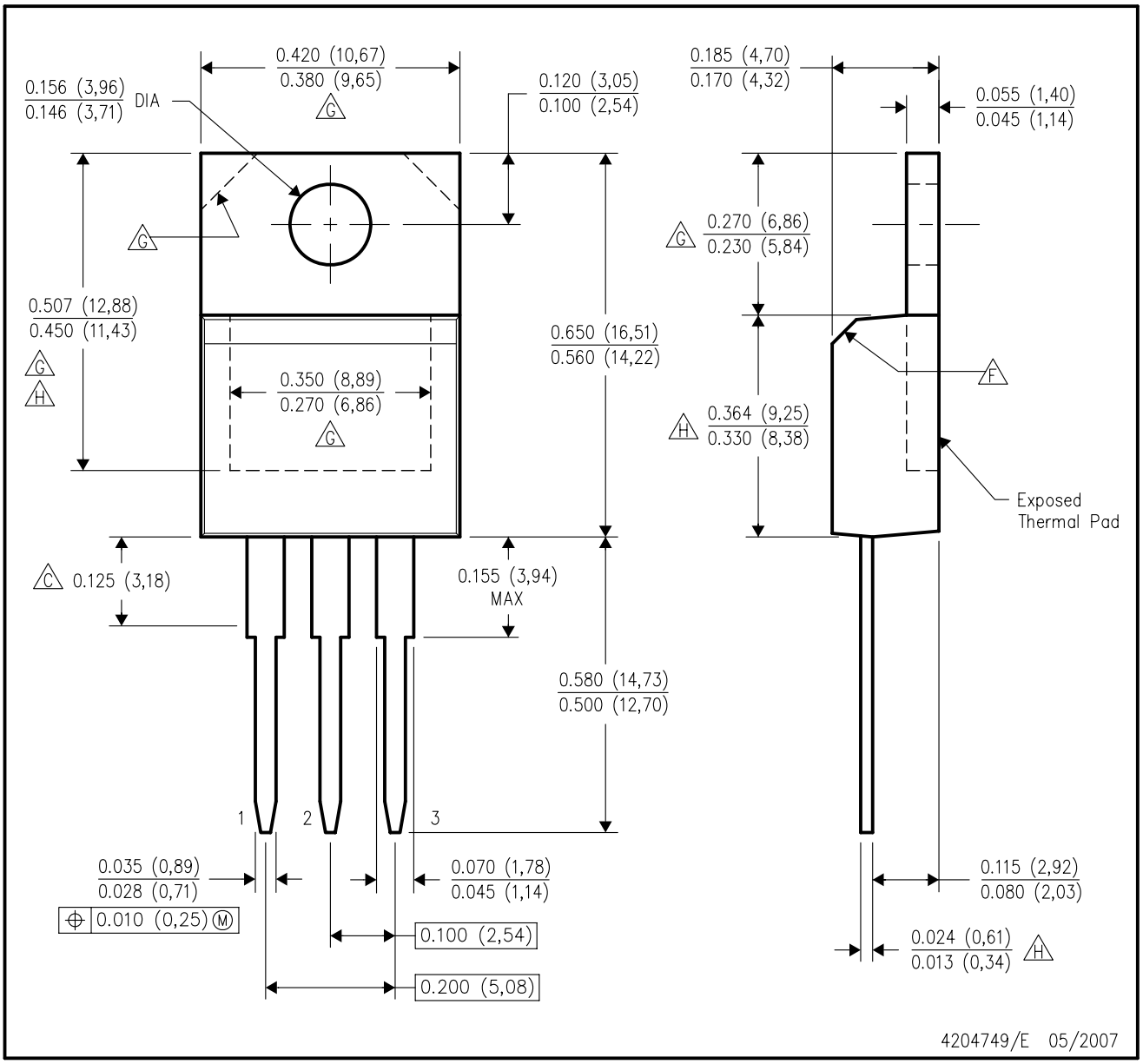
KTP (R-PSFM-G2) **PowerFLEX™ PLASTIC FLANGE-MOUNT PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the thermal tab.
D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
E. Falls within JEDEC TO-252 variation AC.

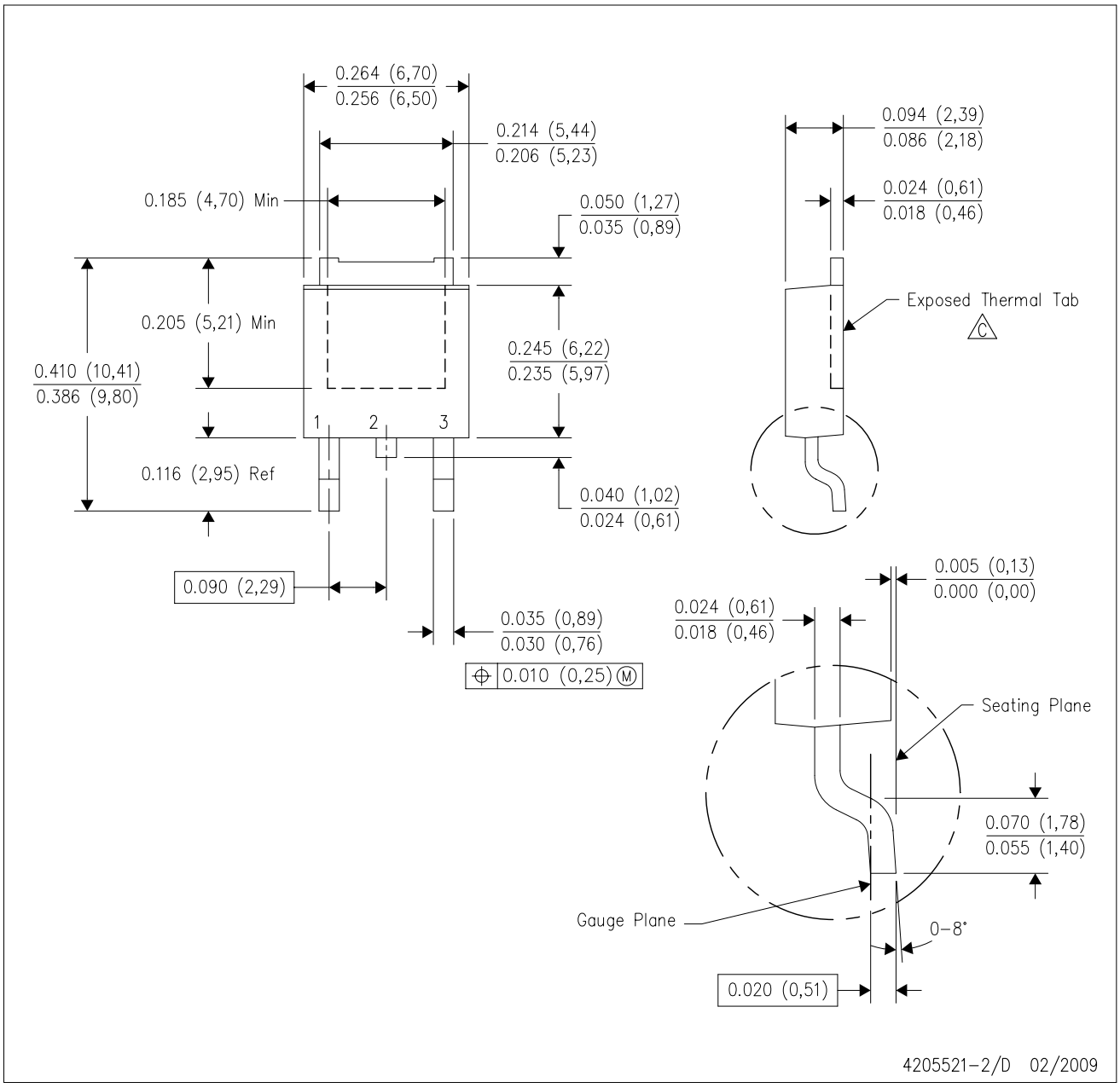
PowerFLEX is a trademark of Texas Instruments.

KCS (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



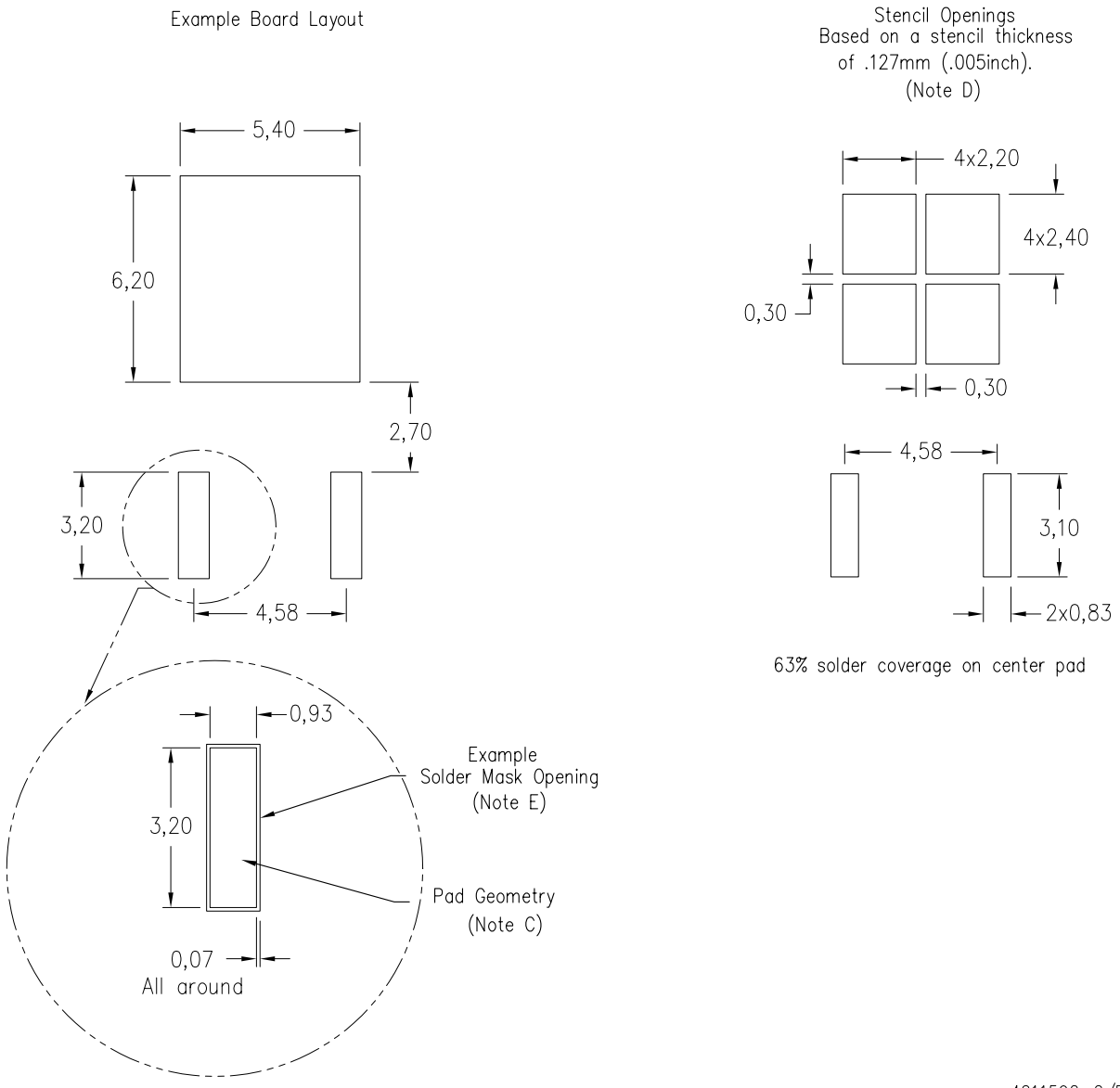
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Thermal pad contour optional within these dimensions.
- H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

KVU (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



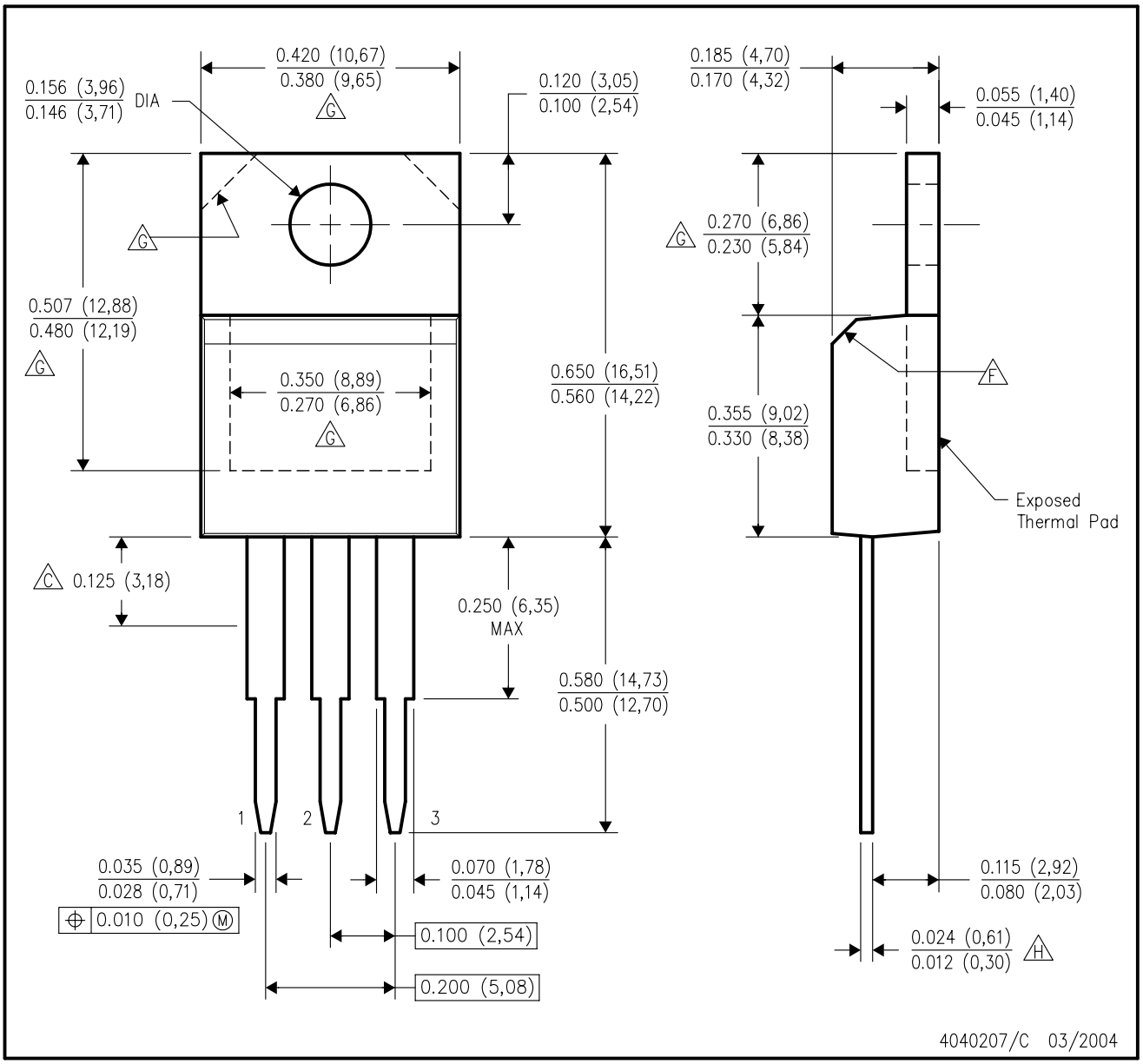
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AA.

KVU (R–PSFM–G3) PLASTIC FLANGE MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

KC (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Thermal pad contour optional within these dimensions.
- H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness.

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