

2-Series, 3-Series, and 4-Series Li-Ion Battery Pack Manager

Check for Samples: [bq30z554-R1](#)

FEATURES

- Fully Integrated 2-Series, 3-Series, and 4-Series Li-Ion or Li-Polymer Cell Battery Pack Manager and Protection
- High Side N-CH Protection FET Drive
- Impedance Track™ Gas Gauging
- Integrated Cell Balancing While Charging or At Rest
- PF Snapshot and Black Box Technology Analyze Returned Packs
- AC Peak Power Information Capability (TURBO Mode)
- SBS v1.1 Interface
- Low Power Modes
 - Low Power: < 180 μ A
 - Sleep < 76 μ A
- Complete Set of Advanced Protections:
 - Internal Cell Short
 - Cell Imbalance
 - Cell Voltage
 - Overcurrent
 - Temperature
 - FET Protection
- Sophisticated Charge Algorithms
 - JEITA
 - Enhanced Charging
 - Adaptive Charging
 - Cell Balancing While Charging or At Rest
- General Purpose Output for Power Interrupt
- Diagnostic Lifetime Data Monitor
- SHA-1 Authentication
- Small Package: TSSOP

APPLICATIONS

- Notebook/Netbook PCs
- Medical and Test Equipment
- Portable Instrumentation

DESCRIPTION

The bq30z554-R1 device is a fully integrated Impedance Track™ gas gauge and analog monitoring single-package solution that provides protection and monitoring with authentication for 2-series, 3-series, and 4-series cell Li-Ion battery packs. The bq30z554-R1 device incorporates sophisticated algorithms that offer cell balancing while charging or at rest.

The device communicates via an SBS v1.1 interface, providing high accuracy cell parameter reporting and control of battery pack operation, and can be designed into systems that require AC peak power (TURBO mode), using a method to ensure that system performance is not disrupted.

An optimum balance of quick response hardware-based protection along with intelligent CPU control delivers an ideal pack solution. The device has flexible user-programmable settings of critical system parameters, such as voltage, current, temperature, and cell imbalance, among other conditions.

The bq30z554-R1 device has advanced charge algorithms, including JEITA support, enhanced cell charging, and adaptive charging compensating charge losses, enabling faster charging. In addition, the bq30z554-R1 device can monitor critical parameters over the life of the battery pack, tracking usage conditions.

A general purpose output is used for power interruption, employing an external push button switch.

The advanced snapshot and black box functionality show critical information for analysis of returned battery packs.

SHA-1 authentication with secure memory for authentication keys enables identification for genuine battery packs beyond doubt.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Impedance Track is a trademark of Texas Instruments.

bq30z554-R1

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

| T _A | PART NUMBER | PACKAGE | PACKAGE DESIGNATOR | PACKAGE MARKING | ORDERING INFORMATION ⁽¹⁾ | |
|----------------|-------------|----------|--------------------|-----------------|-------------------------------------|------------------------------|
| | | | | | TUBE ⁽²⁾ | TAPE AND REEL ⁽³⁾ |
| –40°C to 85°C | bq30z554-R1 | TSSOP–30 | DBT | bq30z554-R1 | bq30z554DBT-R1 | bq30z554DBTR-R1 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of the document, or see the TI website at www.ti.com.

(2) A single tube quantity is 50 units.

(3) A single reel quantity is 2000 units.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | bq30z554-R1 | UNITS |
|-------------------------------|---|-------------|-------|
| | | TSSOP | |
| | | 30 PINS | |
| $\theta_{JA, \text{ High K}}$ | Junction-to-ambient thermal resistance ⁽²⁾ | 73.1 | °C/W |
| $\theta_{JC(\text{top})}$ | Junction-to-case(top) thermal resistance ⁽³⁾ | 17.5 | |
| θ_{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | 34.5 | |
| Ψ_{JT} | Junction-to-top characterization parameter ⁽⁵⁾ | 0.3 | |
| Ψ_{JB} | Junction-to-board characterization parameter ⁽⁶⁾ | 30.3 | |
| $\theta_{JC(\text{bottom})}$ | Junction-to-case(bottom) thermal resistance ⁽⁷⁾ | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/SPRA953).

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

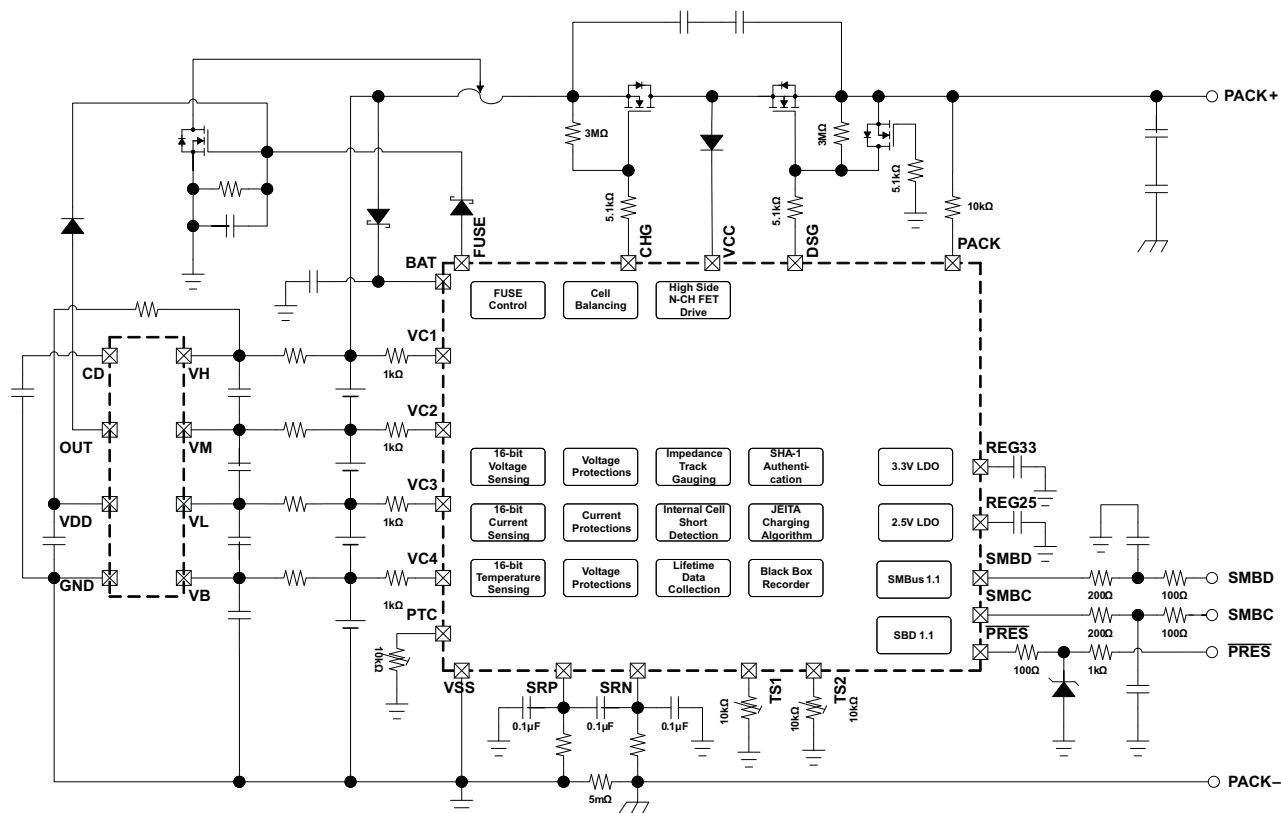
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-top characterization parameter, Ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter, Ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.



TERMINAL FUNCTIONS

| PIN NAME | PIN NUMBER | TYPE | DESCRIPTION |
|--------------------------|-------------|------|---|
| CHG | 1 | O | Discharge N-FET gate drive |
| BAT | 2 | P | Alternate power source |
| VC1 | 3 | I | Sense input for positive voltage of the top-most cell in the series, and cell balancing input for the top-most cell in the series |
| VC2 | 4 | I | Sense input for positive voltage of the third lowest cell in the series, and cell balancing input for the third lowest cell in the series |
| VC3 | 5 | I | Sense input for positive voltage of the second lowest cell in the series, and cell balancing input for the second lowest cell in the series |
| VC4 | 6 | I | Sense input for positive voltage of the lowest cell in the series, and cell balancing input for the lowest cell in the series |
| VSS | 7 | P | Device ground |
| TS1 | 8 | AI | Temperature sensor 1 thermistor input |
| SRP | 9 | AI | Differential coulomb counter input |
| TS2 | 11 | AI | Temperature sensor 2 thermistor input |
| SRN | 10 | AI | Differential coulomb counter input |
| $\overline{\text{PRES}}$ | 12 | I | Host system present input |
| SMBD | 13 | I/OD | SBS 1.1 data line |
| NC | 14 | — | Not connected, connect to VSS |
| SMBC | 15 | I/OD | SBS 1.1 clock line |
| GPIO | 16 | I/OD | General Purpose Input-Output |
| NC | 17,18,19,20 | — | Not connected |
| RBI | 21 | P | RAM backup |
| REG25 | 22 | P | 2.5-V regulator output |
| VSS | 23 | P | Device ground |
| REG33 | 24 | P | 3.3-V regulator output |
| PTC | 25 | — | Test pin connect to VSS |
| FUSE | 26 | O | Fuse drive |
| VCC | 27 | P | Power supply voltage |
| GPOD | 28 | I/OD | High voltage general purpose I/O |
| PACK | 29 | P | Alternate power source |
| DSG | 30 | O | Charge N-FET gate drive |

PINOUT DIAGRAM

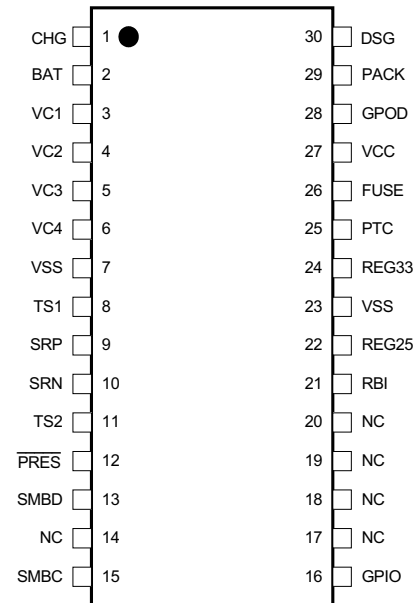


Figure 2. bq30z554-R1 Pinout Diagram

PIN EQUIVALENT DIAGRAMS

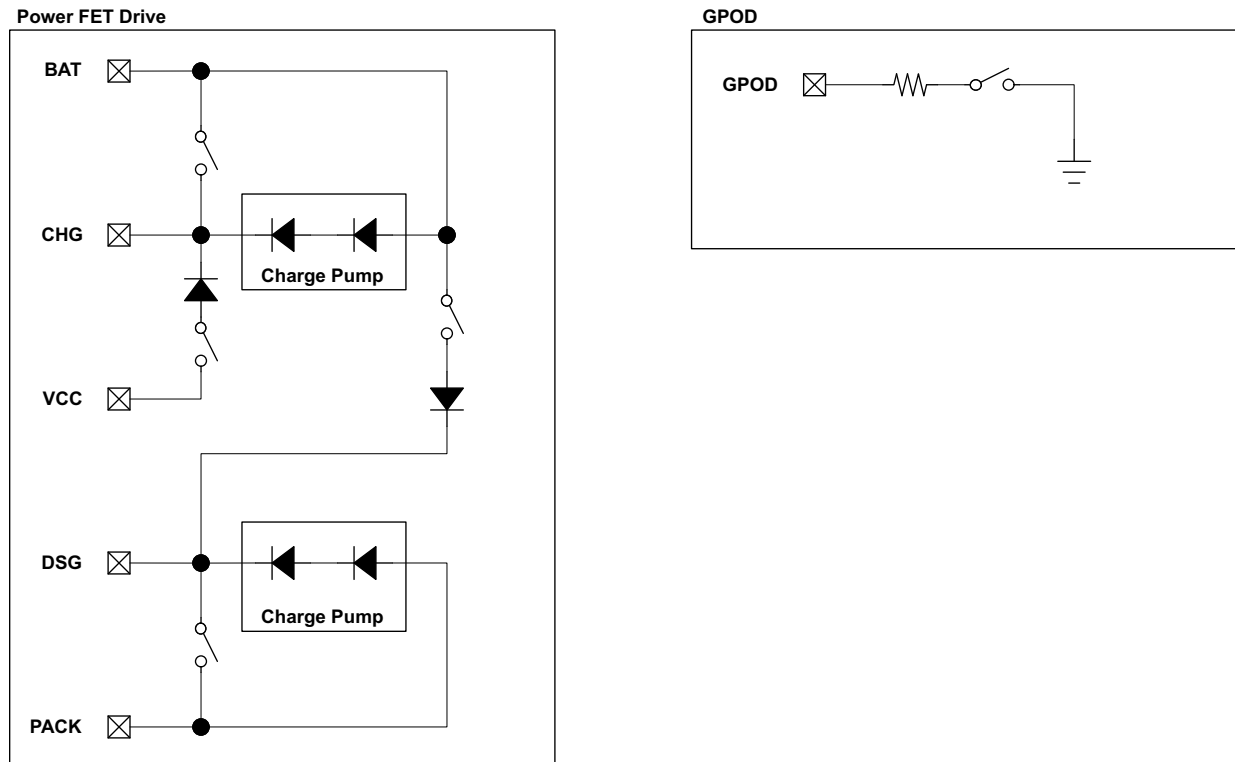


Figure 3. Pin Equivalent Diagram 1

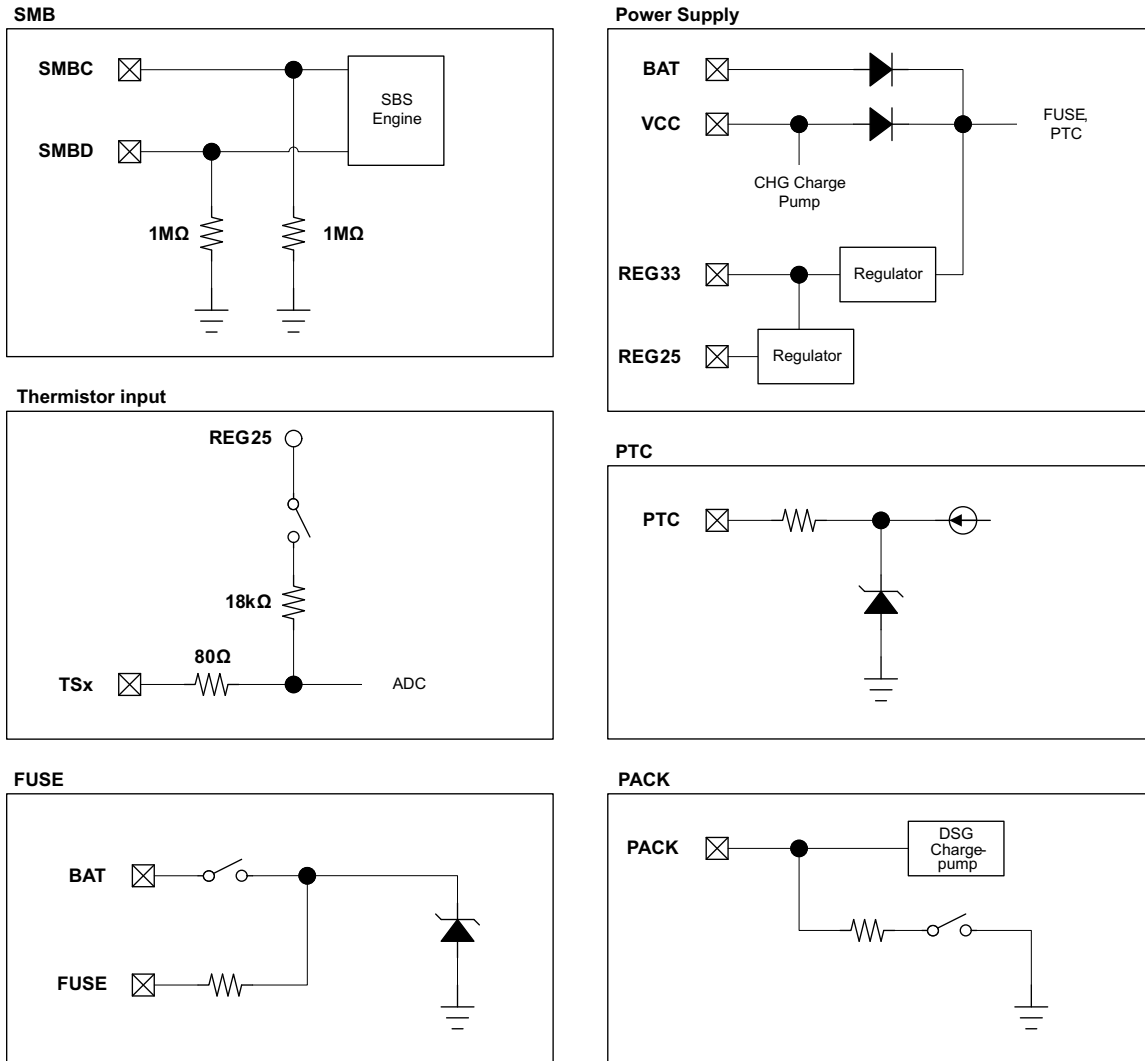


Figure 4. Pin Equivalent Diagram 2

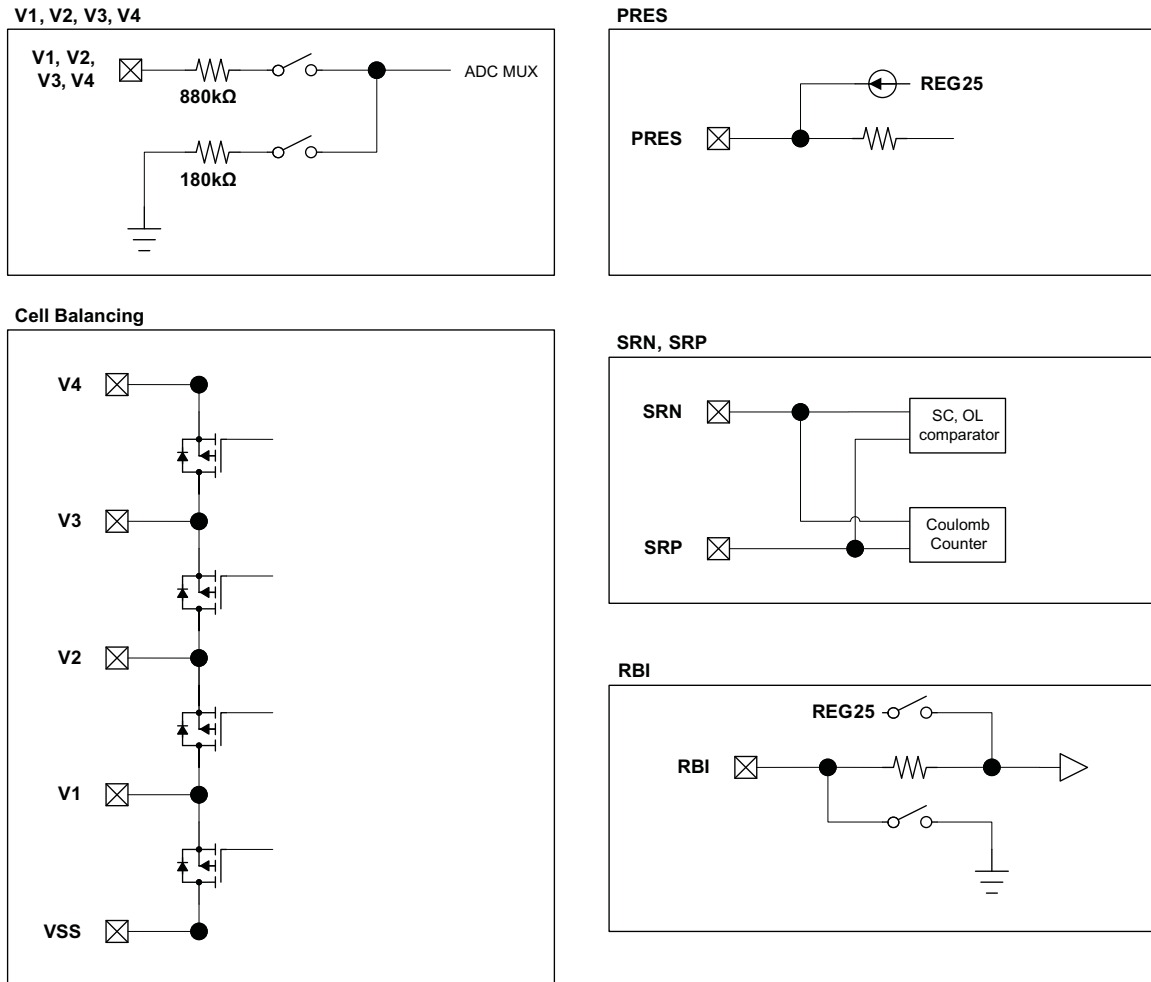


Figure 5. Pin Equivalent Diagram 3

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| DESCRIPTION | PINS | VALUE |
|--|------------------------------------|--|
| Supply voltage range, V_{MAX} | VCC, PTC, PACK w.r.t. V_{SS} | –0.3 V to 34 V |
| Input voltage range, V_{IN} | VC1, BAT | $V_{VC2} - 0.3$ V to $V_{VC2} + 8.5$ or 34 V, whichever is lower |
| | VC2 | $V_{VC3} - 0.3$ V to $V_{VC3} + 8.5$ V |
| | VC3 | $V_{VC4} - 0.3$ V to $V_{VC4} + 8.5$ V |
| | VC4 | $V_{SRP} - 0.3$ V to $V_{SRP} + 8.5$ V |
| | SRP, SRN | –0.3 V to 0.3 V |
| | SMBC, SMBD | $V_{SS} - 0.3$ V to 6.0 V |
| | TS1, TS2, \overline{PRES} , GPIO | –0.3 V to $V_{REG25} + 0.3$ V |
| Output voltage range, V_O | DSG | –0.3 V to $V_{PACK} + 20$ V or $V_{SS} + 34$ V, whichever is lower |
| | CHG | –0.3 V to $V_{BAT} + 20$ V or $V_{SS} + 34$ V, whichever is lower |
| | GPOD, FUSE | –0.3 V to 34 V |
| | RBI, REG25 | –0.3 V to 2.75 V |
| | REG33 | –0.3 V to 5.0 V |
| Maximum V_{SS} current, I_{SS} | | 50 mA |
| Current for cell balancing, I_{CB} | | 10 mA |
| ESD Rating | HBM, VCx Only | 1 kV |
| Functional Temperature, T_{FUNC} | | –40 to 110 °C |
| Storage temperature range, T_{STG} | | –65 to 150 °C |
| Lead temperature (soldering, 10 s), T_{SOLDER} | | 300 °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Typical values stated where $T_A = 25$ °C and $V_{CC} = 14.4$ V, Min/Max values stated where $T_A = -40$ °C to 85 °C and $V_{CC} = 3.8$ V to 25 V (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|--|----------------------------------|-----------|-----|-----------------|------|
| Supply voltage | VCC, PACK | | | 25 | V |
| | BAT | 3.8 | | $V_{VC2} + 5.0$ | |
| $V_{STARTUP}$ | Start up voltage at PACK | 3.0 | | 5.5 | V |
| V_{IN} Input voltage range | VC1, BAT | V_{VC2} | | $V_{VC2} + 5.0$ | V |
| | VC2 | V_{VC3} | | $V_{VC3} + 5.0$ | |
| | VC3 | V_{VC4} | | $V_{VC4} + 5.0$ | |
| | VC4 | V_{SRP} | | $V_{SRP} + 5.0$ | |
| | $VCn - VC(n+1)$, (n=1, 2, 3, 4) | 0 | | 5.0 | |
| | PACK | | | 25 | |
| | PTC | 0 | | 2 | V |
| | SRP to SRN | –0.2 | | 0.2 | V |
| C_{REG33} External 3.3-V REG capacitor | | 1 | | | μF |
| C_{REG25} External 2.5-V REG capacitor | | 1 | | | μF |
| T_{OPR} Operating temperature | | –40 | | 85 | °C |

ELECTRICAL CHARACTERISTICS: Supply Current

Typical values stated where $T_A = 25\text{ }^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|----------|--|-----|-----|-----|---------------|
| I_{CC} | Normal | CHG on, DSG on, no Flash write | | 410 | | μA |
| | Sleep | CHG off, DSG on, no SBS Communication | | 129 | | μA |
| | | CHG off, DSG off, no SBS Communication | | 83 | | μA |
| | Shutdown | | | | 1 | μA |

ELECTRICAL CHARACTERISTICS: Power On Reset (POR)

Typical values stated where $T_A = 25\text{ }^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|------------------------------|-----------------|-----|-----|-----|------|
| V_{IT-} | Negative-going voltage input | At REG25 | 1.9 | 2.0 | 2.1 | V |
| V_{HYS} | POR Hysteresis | At REG25 | 65 | 125 | 165 | mV |

ELECTRICAL CHARACTERISTICS: WAKE FROM SLEEP

Typical values stated where $T_A = 25\text{ }^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--|----------------------------|-----|-----|-----|-----------------------|
| V_{WAKE} | V_{WAKE} Threshold | $V_{WAKE} = 1.2\text{ mV}$ | 0.2 | 1.2 | 2.0 | mV |
| | | $V_{WAKE} = 2.4\text{ mV}$ | 0.4 | 2.4 | 3.6 | |
| | | $V_{WAKE} = 5\text{ mV}$ | 2.0 | 5.0 | 6.8 | |
| | | $V_{WAKE} = 10\text{ mV}$ | 5.3 | 10 | 13 | |
| V_{WAKE_TCO} | Temperature drift of V_{WAKE} accuracy | | | 0.5 | | $\%/^{\circ}\text{C}$ |
| t_{WAKE} | Time from application of current and wake of bq30z554-R1 | | | 0.2 | 1 | ms |

ELECTRICAL CHARACTERISTICS: RBI RAM Backup

Typical values stated where $T_A = 25\text{ }^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|----------------------------------|--|-----|-----|------|------|
| $I_{(RBI)}$ | RBI data-retention input current | $V_{RB} > V_{(RB)MIN}$, $V_{CC} < V_{IT}$ | | 20 | 1100 | nA |
| | | $V_{RB} > V_{(RB)MIN}$, $V_{CC} < V_{IT}$, $T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ | | | 500 | |
| $V_{(RBI)}$ | RBI data-retention voltage | | 1 | | | V |

ELECTRICAL CHARACTERISTICS: 3.3-V Regulator

Typical values stated where $T_A = 25\text{ }^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|--------------------------|--|-----|-----|-----|------|
| V_{REG33} | Regulator output voltage | $3.8\text{ V} < V_{CC}$ or $BAT \leq 5\text{ V}$, $I_{CC} \leq 4\text{ mA}$ | 2.4 | | 3.5 | V |
| | | $5\text{ V} < V_{CC}$ or $BAT \leq 6.8\text{ V}$, $I_{CC} \leq 13\text{ mA}$ | 3.1 | 3.3 | 3.5 | V |
| | | $6.8\text{ V} < V_{CC}$ or $BAT \leq 20\text{ V}$, $I_{CC} \leq 30\text{ mA}$ | 3.1 | 3.3 | 3.5 | V |
| I_{REG33} | Regulator Output Current | | 2 | | | mA |

ELECTRICAL CHARACTERISTICS: 3.3-V Regulator (continued)

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|-----|-----|-----|------|
| $V_{(VDDTEMP)}$ | Regulator output change with temperature | 0.2 | | | % |
| $\Delta V_{(VDDLIN)}$ | Line regulation | 1 | | | mV |
| $\Delta V_{(VDDLLOAD)}$ | Load regulation | 5 | | | mV |
| $I_{(REG33MAX)}$ | Current limit | 70 | | | mA |
| | | 33 | | | |

ELECTRICAL CHARACTERISTICS: 2.5-V Regulator

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|------|-----|------|------|
| V_{REG25} | Regulator output voltage | 2.35 | 2.5 | 2.55 | V |
| I_{REG25} | Regulator Output Current | 3 | | | mA |
| $\Delta V_{(VDDTEMP)}$ | Regulator output change with temperature | 0.25 | | | % |
| $\Delta V_{(VDDLIN)}$ | Line regulation | 1 | | | mV |
| $\Delta V_{(VDDLLOAD)}$ | Load regulation | 20 | | | mV |
| $I_{(REG33MAX)}$ | Current limit | 65 | | | mA |
| | | 23 | | | |

ELECTRICAL CHARACTERISTICS: $\overline{\text{PES}}$, SMBD, SMBC, GPIO

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|--------------------------|--|-----|-----|---------------|
| V_{IH} | High-level input | $\overline{\text{PES}}$, SMBD, SMBC, GPIO | | | V |
| V_{IL} | Low-level input | $\overline{\text{PES}}$, SMBD, SMBC, GPIO $I_L = -0.5\text{ mA}$ | | | V |
| V_{OL} | Low-level output voltage | SMBD, SMBC, GPIO, $I_L = 7\text{ mA}$ | | | V |
| C_{IN} | Input capacitance | $\overline{\text{PES}}$, SMBD, SMBC, GPIO | | | pF |
| I_{LKG} | Input leakage current | $\overline{\text{PES}}$, SMBD, SMBC, GPIO | | | μA |
| I_{WPU} | Weak Pull Up Current | $\overline{\text{PES}}$, GPIO, $V_{OH} = V_{REG25} - 0.5\text{ V}$ | | | μA |
| $R_{PD(SMBx)}$ | SMBC, SMBD Pull-Down | $T_A = -40^\circ\text{C}$ to 100°C | | | k Ω |

ELECTRICAL CHARACTERISTICS: CHG, DSG FET Drive

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|--|------|-----|------|---------------|
| $V_{(FETON)}$ | $V_{O(FETONDSG)} = V_{(DSG)} - V_{PACK}$, VGS connect 10 M Ω , $V_{CC} 3.8\text{ V}$ to 8.4 V | 8.0 | 9.7 | 12 | V |
| | $V_{O(FETONDSG)} = V_{(DSG)} - V_{PACK}$, VGS connect 10 M Ω , $V_{CC} > 8.4\text{ V}$ | 9.0 | 11 | 12 | V |
| | $V_{O(FETONCHG)} = V_{(CHG)} - V_{BAT}$, V_{GS} connect 10 M Ω , $V_{CC} 3.8\text{ V}$ to 8.4 V | 8.0 | 9.7 | 12 | V |
| | $V_{O(FETONCHG)} = V_{(CHG)} - V_{BAT}$, V_{GS} connect 10 M Ω , $V_{CC} > 8.4\text{ V}$ | 9.0 | 11 | 12 | V |
| $V_{(FETOFF)}$ | $V_{O(FETOFFDSG)} = V_{(DSG)} - V_{PACK}$ | -0.4 | | 0.4 | V |
| | $V_{O(FETOFFCHG)} = V_{(CHG)} - V_{BAT}$ | -0.4 | | 0.4 | V |
| t_r | $C_L = 4700\text{ pF}$ $R_G = 5.1\text{ k}\Omega$ $V_{CC} < 8.4$ $V_{DSG}: V_{BAT}$ to $V_{BAT} + 4\text{ V}$, $V_{CHG}: V_{PACK}$ to $V_{PACK} + 4\text{ V}$ | | 800 | 1400 | μs |
| | $C_L = 4700\text{ pF}$ $R_G = 5.1\text{ k}\Omega$ $V_{CC} > 8.4$ $V_{DSG}: V_{BAT}$ to $V_{BAT} + 4\text{ V}$, $V_{CHG}: V_{PACK}$ to $V_{PACK} + 4\text{ V}$ | | 200 | 500 | μs |
| t_f | $C_L = 4700\text{ pF}$ $R_G = 5.1\text{ k}\Omega$ $V_{DSG}: V_{BAT} + V_{O(FETONDSG)}$ to $V_{BAT} + 1\text{ V}$ $V_{CHG}: V_{PACK} + V_{O(FETONCHG)}$ to $V_{PACK} + 1\text{ V}$ | | 80 | 200 | μs |

ELECTRICAL CHARACTERISTICS: GPOD

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|-------------------------|------------------------|-----|----------|------|
| V_{PU_GPOD} | GPOD Pull Up Voltage | | | V_{CC} | V |
| V_{OL_GPOD} | GPOD Output Voltage Low | $I_{OL} = 1\text{ mA}$ | 0.3 | | V |

ELECTRICAL CHARACTERISTICS: FUSE

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|-----------------------------------|---|-----|-----|---------------|
| $V_{OH(FUSE)}$ | High Level FUSE Output | $V_{CC} = 3.8\text{ V}$ to 9 V | 2.4 | 8.5 | V |
| | | $V_{CC} = 9\text{ V}$ to 25 V | 7 | 8 | V |
| $V_{IH(FUSE)}$ | | 2.8 | | | V |
| | Weak Pull Up Current in off state | Ensured by design. Not production tested. | 100 | | nA |
| $t_{R(FUSE)}$ | FUSE Output Rise Time | $C_L = 1\text{ nF}$, $V_{CC} = 9\text{ V}$ to 25 V , $V_{OH(FUSE)} = 0\text{ V}$ to 5 V | 5 | 20 | μs |
| $Z_{O(FUSE)}$ | FUSE Output Impedance | | 2 | 5 | k Ω |

ELECTRICAL CHARACTERISTICS: PTC Thermistor Support

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|--------------------|--|------|------|------|------------------|
| R_{PTC} | PTC | $V_{PTC} = 0$ to 2 V , | | | | |
| | | $T_A = -40^{\circ}\text{C}$ to 110°C | 1.3 | 2 | 2.7 | $\text{M}\Omega$ |
| $I_{O(PTC)}$ | PTC | $V_{PTC} = 0$ to 2 V | | | | |
| | | $T_A = -40^{\circ}\text{C}$ to 110°C | -450 | -370 | -230 | nA |
| t_{PTC} | PTC Blanking Delay | $T_A = -40^{\circ}\text{C}$ to 110°C | 60 | 80 | 110 | ms |

ELECTRICAL CHARACTERISTICS: COULOMB COUNTER

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-------------------------------|---------------------------|-------|------|------|--------------------------------|
| V_{IN} | Input voltage range | SRP – SRN | -0.20 | | 0.25 | V |
| | Conversion time | Single conversion | | 250 | | ms |
| | Resolution (no missing codes) | | 16 | | | bits |
| | Effective resolution | Single conversion, signed | 15 | | | bits |
| | Offset error | Post Calibrated | | 10 | | μV |
| | Offset error drift | | | 0.3 | 0.5 | $\mu\text{V}/^{\circ}\text{C}$ |
| | Full-scale error | | -0.8% | 0.2% | 0.8% | |
| | Full-scale error drift | | | | 150 | PPM/ $^{\circ}\text{C}$ |
| | Effective input resistance | | 2.5 | | | $\text{M}\Omega$ |

ELECTRICAL CHARACTERISTICS: VC1, VC2, VC3, VC4

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|--|---|-------|-----|-----|----------|
| V_{IN} | Input voltage range | VC4 – VC3, VC3 – VC2, VC2 – VC1, VC1 – VSS | -0.20 | | 8 | V |
| | Conversion time | Single conversion | | 32 | | ms |
| | Resolution (no missing codes) | | 16 | | | bits |
| | Effective resolution | Single conversion, signed | 15 | | | bits |
| $R_{(BAL)}$ | $R_{DS(ON)}$ for internal FET at $V_{DS} > 2\text{ V}$ | $V_{DS} = \text{VC4} - \text{VC3}, \text{VC3} - \text{VC2}, \text{VC2} - \text{VC1}, \text{VC1} - \text{VSS}$ | 200 | 310 | 430 | Ω |
| | $R_{DS(ON)}$ for internal FET at $V_{DS} > 4\text{ V}$ | $V_{DS} = \text{VC4} - \text{VC3}, \text{VC3} - \text{VC2}, \text{VC2} - \text{VC1}, \text{VC1} - \text{VSS}$ | 60 | 125 | 230 | Ω |

ELECTRICAL CHARACTERISTICS: TS1, TS2

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|---|-----------------|------|------|------|-------------------------|
| R | Internal Pull Up Resistor | | 16.5 | 17.5 | 19.0 | $\text{K}\Omega$ |
| R_{DRIFT} | Internal Pull Up Resistor Drift from 25°C | | | | 200 | PPM/ $^{\circ}\text{C}$ |
| R_{PAD} | Internal Pin Pad resistance | | | 84 | | Ω |

ELECTRICAL CHARACTERISTICS: TS1, TS2 (continued)

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-------------------------------|----------------------|-------|-----|------------------------|------|
| V_{IN} | Input voltage range | TS1 – VSS, TS2 – VSS | –0.20 | | $0.8 \times V_{REG25}$ | V |
| | Conversion Time | | | 16 | | ms |
| | Resolution (no missing codes) | | 16 | | | Bits |
| | Effective resolution | | 11 | 12 | | Bits |

ELECTRICAL CHARACTERISTICS: Internal Temperature Sensor

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|-------------------------------|-----------------|------|------|------|------------------------|
| $V_{(TEMP)}$ | Temperature sensor voltage | | –1.9 | –2.0 | –2.1 | mV/ $^{\circ}\text{C}$ |
| | Conversion Time | | | 16 | | ms |
| | Resolution (no missing codes) | | 16 | | | Bits |
| | Effective resolution | | 11 | 12 | | Bits |

ELECTRICAL CHARACTERISTICS: Internal Thermal Shutdown

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|---------------------------------|-----------------|-----|-----|-----|--------------------|
| T_{MAX} | Maximum REG33 temperature | | 125 | | 175 | |
| $T_{RECOVER}$ | Recovery hysteresis temperature | | | 10 | | $^{\circ}\text{C}$ |
| $t_{PROTECT}$ | Protection time | | | 5 | | μs |

ELECTRICAL CHARACTERISTICS: High Frequency Oscillator

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|-----------------------------------|---|-----|--------------|-----|------|
| $f_{(OSC)}$ | Operating frequency of CPU Clock | | | 4.194 | | MHz |
| $f_{(EIO)}$ | Frequency error ⁽¹⁾⁽²⁾ | $T_A = -20^{\circ}\text{C}$ to 70°C | –2% | $\pm 0.25\%$ | 2% | |
| | | $T_A = -40^{\circ}\text{C}$ to 85°C | –3% | $\pm 0.25\%$ | 3% | |
| $t_{(SXO)}$ | Start-up time ⁽³⁾ | $T_A = -25^{\circ}\text{C}$ to 85°C | | 3 | 6 | ms |

(1) The frequency error is measured from 4.194 MHz.

(2) The frequency drift is included and measured from the trimmed frequency at $V_{REG25} = 2.5\text{ V}$, $T_A = 25^{\circ}\text{C}$.

(3) The startup time is defined as the time it takes for the oscillator output frequency to be $\pm 3\%$ when the device is already powered.

ELECTRICAL CHARACTERISTICS: Low Frequency Oscillator

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|-----------------------------------|---|-------|--------------|------|---------------|
| $f_{(LOSC)}$ | Operating frequency | | | 32.768 | | kHz |
| $f_{(LEIO)}$ | Frequency error ⁽¹⁾⁽²⁾ | $T_A = -20^{\circ}\text{C}$ to 70°C | –1.5% | $\pm 0.25\%$ | 1.5% | |
| | | $T_A = -40^{\circ}\text{C}$ to 85°C | –2.5% | $\pm 0.25\%$ | 2.5% | |
| $t_{(LSXO)}$ | Start-up time ⁽³⁾ | $T_A = -25^{\circ}\text{C}$ to 85°C | | | 100 | μs |

(1) The frequency drift is included and measured from the trimmed frequency at $V_{CC} = 2.5\text{ V}$, $T_A = 25^{\circ}\text{C}$.

(2) The frequency error is measured from 32.768 kHz.

(3) The startup time is defined as the time it takes for the oscillator output frequency to be $\pm 3\%$.

ELECTRICAL CHARACTERISTICS: Internal Voltage Reference

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|----------------------------------|---|-------|----------|-------------------------|
| V_{REF} | Internal Reference Voltage | 1.215 | 1.225 | 1.230 | V |
| V_{REF_DRIFT} | Internal Reference Voltage Drift | $T_A = -25^{\circ}\text{C}$ to 85°C | | ± 80 | PPM/ $^{\circ}\text{C}$ |
| | | $T_A = 0^{\circ}\text{C}$ to 60°C | | ± 50 | PPM/ $^{\circ}\text{C}$ |

ELECTRICAL CHARACTERISTICS: Flash

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|---------------------------------|--------------------------------|-----|-----|-----|--------|
| | Data retention | | 10 | | | Years |
| | Flash programming write-cycles | Data Flash | 20k | | | Cycles |
| | | Instruction Flash | 1k | | | Cycles |
| I _{CC} (PROG_DF) | Data Flash-write supply current | T _A = −40°C to 85°C | | 3 | 4 | mA |
| I _{CC} (ERASE_DF) | Data Flash-erase supply current | T _A = −40°C to 85°C | | 3 | 18 | mA |

(1) Assured by design. Not production tested.

ELECTRICAL CHARACTERISTICS: OCD Current Protection

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|---|--------------------------------|-----|-----|-----|------|
| V _(OCD) | OCD detection threshold voltage range, typical | RSNS = 0 | 50 | | 200 | mV |
| | | RSNS = 1 | 25 | | 100 | mV |
| ΔV _(OCDT) | OCD detection threshold voltage program step | RSNS = 0 | 10 | | | mV |
| | | RSNS = 1 | 5 | | | mV |
| V _(OFFSET) | OCD offset | | −10 | | 10 | mV |
| V _(Scale_Err) | OCD scale error | | −10 | | 10 | % |
| t _(OCDD) | Overcurrent in Discharge Delay | | 1 | | 31 | ms |
| t _(OCDD_STEP) | OCDD Step options | | 2 | | | ms |
| t _(DETECT) | Current fault detect time | VSRP – SRN = VTHRESH + 12.5 mV | 160 | | | μs |
| t _{ACC} | Overcurrent and Short Circuit delay time accuracy | Accuracy of typical delay time | −20 | | 20 | % |

ELECTRICAL CHARACTERISTICS: SCD1 Current Protection

Typical values stated where $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|----------------------------|-----|------|---------------|
| $V_{(SDC1)}$ | SCD1 detection threshold voltage range, typical | RSNS = 0 | 100 | 450 | mV |
| | | RSNS = 1 | 50 | 225 | mV |
| $\Delta V_{(SDC1T)}$ | SCD1 detection threshold voltage program step | RSNS = 0 | 50 | | mV |
| | | RSNS = 1 | 25 | | mV |
| $V_{(OFFSET)}$ | SCD1 offset | -10 | | 10 | mV |
| $V_{(Scale_Err)}$ | SCD1 scale error | -10 | | 10 | % |
| $t_{(SCD1D)}$ | Short Circuit in Discharge Delay | AFE.STATE_CNTL[SCDDx2] = 0 | 0 | 915 | μs |
| | | AFE.STATE_CNTL[SCDDx2] = 1 | 0 | 1830 | μs |
| $t_{(SCD1D_STEP)}$ | SCD1D Step options | AFE.STATE_CNTL[SCDDx2] = 0 | 61 | | μs |
| | | AFE.STATE_CNTL[SCDDx2] = 1 | 122 | | μs |

ELECTRICAL CHARACTERISTICS: SCD1 Current Protection (continued)

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|-----|-----|-----|---------------|
| t_{DETECT} | Current fault detect time VSRP-SRN = VTHRESH + 12.5 mV | | | 160 | μs |
| t_{ACC} | Overcurrent and Short Circuit delay time accuracy Accuracy of typical delay time | -20 | | 20 | % |

ELECTRICAL CHARACTERISTICS: SCD2 Current Protection

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|---|-----|------|-----|---------------|
| V_{SDC2} | SCD2 detection threshold voltage range, typical RSNS = 0 | 100 | | 450 | mV |
| | RSNS = 1 | 50 | | 225 | mV |
| ΔV_{SCD2T} | SCD2 detection threshold voltage program step RSNS = 0 | | 50 | | mV |
| | RSNS = 1 | | 25 | | mV |
| V_{OFFSET} | SCD2 offset | -10 | | 10 | mV |
| $V_{\text{Scale_Err}}$ | SCD2 scale error | -10 | | 10 | % |
| t_{SCD1D} | Short Circuit in Discharge Delay AFE.STATE_CNTL[SCDDx2] = 0 | 0 | | 458 | μs |
| | AFE.STATE_CNTL[SCDDx2] = 1 | 0 | | 915 | μs |
| $t_{\text{SCD2D_STEP}}$ | SCD2D Step options AFE.STATE_CNTL[SCDDx2] = 0 | | 30.5 | | μs |
| | AFE.STATE_CNTL[SCDDx2] = 1 | | 61 | | μs |
| t_{DETECT} | Current fault detect time VSRP – SRN = VTHRESH + 12.5 mV | | | 160 | μs |
| t_{ACC} | Overcurrent and Short Circuit delay time accuracy Accuracy of typical delay time | -20 | | 20 | % |

ELECTRICAL CHARACTERISTICS: SCC Current Protection

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|---|------|-----|------|---------------|
| V_{SCCT} | SCC detection threshold voltage range, typical RSNS = 0 | -100 | | -300 | mV |
| | RSNS = 1 | -50 | | -225 | mV |
| ΔV_{SCCDT} | SCC detection threshold voltage program step RSNS = 0 | | -50 | | mV |
| | RSNS = 1 | | -25 | | mV |
| V_{OFFSET} | SCC offset | -10 | | 10 | mV |
| $V_{\text{Scale_Err}}$ | SCC scale error | -10 | | 10 | % |
| t_{SCCD} | Short Circuit in Charge Delay | 0 | | 915 | ms |
| $t_{\text{SCCD_STEP}}$ | SCCD Step options | | 61 | | ms |
| t_{DETECT} | Current fault detect time VSRP – SRN = VTHRESH + 12.5 mV | | | 160 | μs |
| t_{ACC} | Overcurrent and Short Circuit delay time accuracy Accuracy of typical delay time | -20 | | 20 | % |

ELECTRICAL CHARACTERISTICS: SBS Timing Characteristics

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|-----|------|-----|------|
| f_{SMB} | SMBus operating frequency SLAVE mode, SMBC 50% duty cycle | 10 | | 100 | kHz |
| f_{MAS} | SMBus master clock frequency MASTER mode, no clock low slave extend | | 51.2 | | kHz |

ELECTRICAL CHARACTERISTICS: SBS Timing Characteristics (continued)

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|--------------------|-----|-----|----------|---------------|
| t_{BUF} | Bus free time between start and stop | | 4.7 | | | μs |
| $t_{\text{HD:STA}}$ | Hold time after (repeated) start | | 4.0 | | | μs |
| $t_{\text{SU:STA}}$ | Repeated start setup time | | 4.7 | | | μs |
| $t_{\text{SU:STO}}$ | Stop setup time | | 4.0 | | | μs |
| $t_{\text{HD:DAT}}$ | Data hold time | | 300 | | | ns |
| $t_{\text{SU:DAT}}$ | Data setup time | | 250 | | | ns |
| t_{TIMEOUT} | Error signal/detect | See ⁽¹⁾ | 25 | | 35 | ms |
| t_{LOW} | Clock low period | | 4.7 | | | μs |
| t_{HIGH} | Clock high period | See ⁽²⁾ | | | Disabled | |
| t_{HIGH} | Clock high period | See ⁽²⁾ | 4.0 | | 50 | μs |
| $t_{\text{LOW:SEXT}}$ | Cumulative clock low slave extend time | See ⁽³⁾ | | | 25 | ms |
| $t_{\text{LOW:MEXT}}$ | Cumulative clock low master extend time | See ⁽⁴⁾ | | | 10 | ms |
| t_{F} | Clock/data fall time | See ⁽⁵⁾ | | | 300 | ns |
| t_{R} | Clock/data rise time | See ⁽⁶⁾ | | | 1000 | ns |

(1) The bq30z554-R1 times out when any clock low exceeds t_{TIMEOUT} .

(2) t_{HIGH} , Max, is the minimum bus idle time. $\text{SMBC} = 1$ for $t > 50\text{ }\mu\text{s}$ causes reset of any transaction involving bq30z554-R1 in progress. This specification is valid when the $\text{THIGH_VAL} = 0$. If $\text{THIGH_VAL} = 1$ then the value of THIGH is set by THIGH_1,2 and the timeout is not SMBus standard.

(3) $t_{\text{LOW:SEXT}}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.

(4) $t_{\text{LOW:MEXT}}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.

(5) Rise time $t_{\text{R}} = V_{\text{ILMAX}} - 0.15$ to $(V_{\text{IHMIN}} + 0.15)$

(6) Fall time $t_{\text{F}} = 0.9 V_{\text{DD}}$ to $(V_{\text{ILMAX}} - 0.15)$

ELECTRICAL CHARACTERISTICS: SBS XL Timing Characteristics

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{ V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{ V}$ to 25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--------------------------------------|--------------------|-----|-----|-----|---------------|
| f_{SMBXL} | SMBus XL operating frequency | SLAVE mode | 40 | | 400 | kHz |
| t_{BUF} | Bus free time between start and stop | | 4.7 | | | μs |
| $t_{\text{HD:STA}}$ | Hold time after (repeated) start | | 4.0 | | | μs |
| $t_{\text{SU:STA}}$ | Repeated start setup time | | 4.7 | | | μs |
| $t_{\text{SU:STO}}$ | Stop setup time | | 4.0 | | | μs |
| t_{TIMEOUT} | Error signal/detect | See ⁽¹⁾ | 5 | | 20 | ms |
| t_{LOW} | Clock low period | | | | 20 | μs |
| t_{HIGH} | Clock high period | See ⁽²⁾ | | | 20 | μs |

(1) The bq30z554-R1 times out when any clock low exceeds t_{TIMEOUT} .

(2) t_{HIGH} , Max, is the minimum bus idle time.

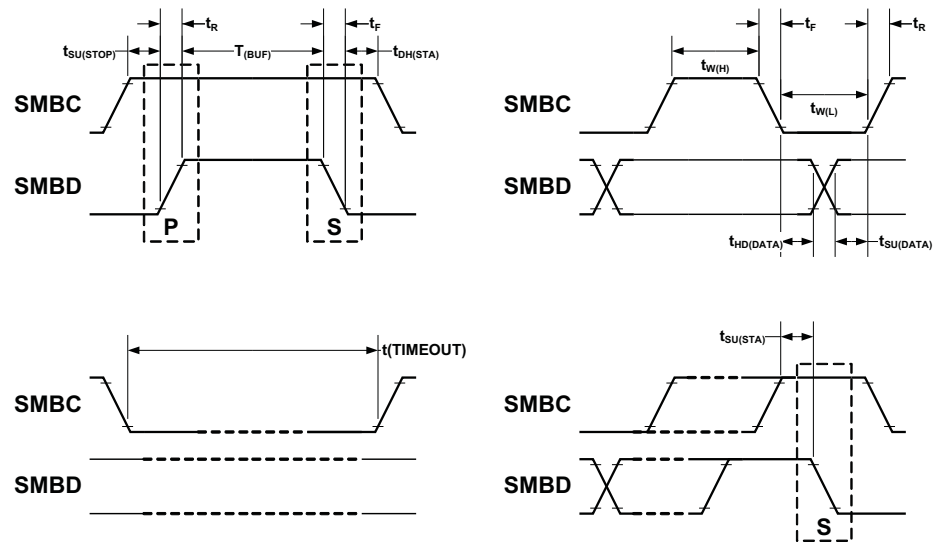


Figure 6. SMBus Timing Diagram

FEATURE SET

Protections Safety Features

The bq30z554-R1 supports a wide range of battery and system protection features that can easily be configured. The Protections safety features include:

- Cell Undervoltage Protection
- Cell Undervoltage I*R Compensated Protection
- Cell Overvoltage Protection
- Overcurrent in Charge Protection 1 and 2
- Overcurrent in Discharge Protection 1 and 2
- Overload in Discharge Protection
- Short Circuit in Charge Protection
- Short Circuit in Discharge Protection 1 and 2
- Overtemperature in Charge Protection
- Overtemperature in Discharge Protection
- Overtemperature FET protection
- SBS Host Watchdog Protection
- Precharge Timeout Protection
- Fast Charge Timeout Protection
- Overcharge Protection
- Overcharging Current Protection
- Overcharging Voltage Protection

Permanent Fail Safety Features

The FUSE pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. Upon a Permanent Fail event trigger, critical system information is written to non-volatile memory to simplify failure analysis. In addition, the black box stores the sequence of safety events also into non-volatile memory to simplify failure analysis. The Permanent Fail safety features include:

- Cell Undervoltage Protection
- Cell Overvoltage Protection
- Copper Deposition
- Overtemperature Cell
- Overtemperature FET
- QMAX Imbalance
- Cell Balancing
- Capacity Degradation
- Impedance
- Voltage Imbalance at Rest
- Voltage Imbalance Active
- Charge FET and Discharge FET
- Thermistor
- Chemical FUSE
- AFE Register
- AFE Communication
- 2nd-Level Protection
- PTC
- Instruction Flash
- Open Cell Tab Connection
- Data Flash

Charge Control Features

The bq30z554-R1 Charge Control features include:

- Supports JEITA temperature ranges T1, T2, T3, T4, T5, T6. Reports charging voltage and charging current, according to the active temperature range.
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges, and allows for varying the charging current according to the cell voltage.
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts.
- Determines the chemical state of charge of each battery cell using Impedance Track and can reduce the charge difference of the battery cells in a fully charged state of the battery pack, gradually using the cell balancing algorithm during rest and charging. This prevents fully charged cells from overcharging and causing excessive degradation, and also increases the usable pack energy by preventing premature charge termination.
- Supports precharging/zero-volt charging
- Supports charge inhibit and charge suspend if the battery pack temperature is out of temperature range.
- Reports charging fault and also indicates charge status via charge and discharge alarms.

Gas Gauging

The bq30z554-R1 uses the Impedance Track technology to measure and calculate the available charge in battery cells. The achievable accuracy is better than 1% error over the lifetime of the battery and there is no full charge or discharge learning cycle required. See the *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* application report ([SLUA364B](#)) for further details.

Lifetime Data Logging Features

The bq30z554-R1 offers extended lifetime data logging where important measurements are stored for warranty and analysis purposes. The data monitored includes *lifetime*:

- Maximum cell voltage cell0, cell1, cell2, cell3
- Minimum cell voltage cell0, cell1, cell2, cell3
- Maximum cell voltage delta
- Maximum charge and discharge current
- Maximum average discharge current
- Maximum average discharge power
- Maximum cell temperature
- Minimum cell temperature
- Maximum cell temperature delta
- Maximum device temperature
- Minimum device temperature
- Maximum FET temperature
- Total accumulated safety events and last safety event in term of charging cycle
- Total accumulated charging events and charging events
- Total accumulated gauging events and gauging events
- Total accumulated cell balancing time cell0, cell1, cell2, cell3
- Total device firmware runtime
- Accumulated runtime in JEITA undertemperature range
- Accumulated runtime in JEITA low temperature range
- Accumulated runtime in JEITA standard temperature range
- Accumulated runtime in JEITA recommended temperature range
- Accumulated runtime in JEITA high temperature range
- Accumulated runtime in JEITA overtemperature range

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Authentication

- The bq30z554-R1 supports authentication by the host using SHA-1.
- SHA-1 authentication by the gas gauge is required for unsealing and full access.

Power Modes

The bq30z554-R1 supports five power modes to reduce power consumption:

- In NORMAL mode, the bq30z554-R1 performs measurements, calculations, protection decisions, and data updates in 0.25-s intervals. Between these intervals, the bq30z554-R1 is in a reduced power stage. In addition, the device will provide information for peak TURBO mode power operation.
- The bq30z554-R1 supports a TURBO mode operation by providing information to the host MCU about the battery pack's ability to deliver peak power. The method of operation is based on the host MCU reading register 0x59 (TURBO_POWER) to determine if the selected power level for TURBO mode operation of the MCU is below the max power reported by the gas gauge. Additionally, the device reports current information during the power pulse by reading register 0x5E (TURBO_CURRENT). The information reported by these two registers allows the MCU to determine if the selected TURBO mode operation is safe and will not cause any system reset due to transient power pulses.
- In SLEEP mode, the bq30z554-R1 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq30z554-R1 is in a reduced power stage. The bq30z554-R1 has a wake function that enables exit from SLEEP mode when current flow or failure is detected.
- In SHUTDOWN mode, the bq30z554-R1 is completely disabled.
- In SHIP mode, the bq30z554-R1 enters a low-power mode with no voltage, current, and temperature measurements, the FETs are turned off, and the MCU is in a halt state. The device wakes up upon SMBus communication detection.

NOTE

For a detailed description of the SBS Commands and Data Flash (DF) Registers, refer to the *bq30z554-R1 Technical Reference Manual* ([SLUUA79](#)).

Configuration

System Present Operation

The bq30z554-R1 checks the $\overline{\text{PRES}}$ pin periodically (1 s). If $\overline{\text{PRES}}$ input is pulled to ground by the external system, the bq30z554-R1 detects this as system present.

Battery Power Interrupt Operation

The bq30z554-R1 can interrupt the battery power by using an external push-button switch and detecting a low-level threshold signal on the GPIO terminal (pin should be configured with an internal pull-up). Once the push button is pressed, there is a delay of 1 s (default) for debounce to detect the low-level threshold. There is also a data flash command for the battery power interrupt timeout. The default value is 30 minutes. If the push-button switch is selected before this timeout, the battery power is restored based on this action.

Timeout Configuration

The timeout feature allows the battery power to be restored once the timer expires. Alternatively, if the value is set to 0, this feature is disabled.

| Class | Subclass ID | Subclass | Offset | Name | Type | Min | Max | Default | Unit |
|-------|-------------|-----------|--------|---------|------|-----|-------|---------|------|
| Power | 248 | Power Off | 0 | Timeout | U2 | 0 | 65535 | 30 | min |

BATTERY PARAMETER MEASUREMENTS

Charge and Discharge Counting

The bq30z554-R1 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurements.

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SR1 and SR2 pins. The integrating ADC measures bipolar signals from -0.25 V to 0.25 V . The bq30z554-R1 detects charge activity when $V_{SR} = V_{(SRP)} - V_{(SRN)}$ is positive, and discharge activity when $V_{SR} = V_{(SRP)} - V_{(SRN)}$ is negative. The bq30z554-R1 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.65 nVh .

Voltage

The bq30z554-R1 updates the individual series cell voltages at 0.25-s intervals. The internal ADC of the bq30z554-R1 measures the voltage, and scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the Impedance Track gas gauging.

Current

The bq30z554-R1 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a $5\text{-m}\Omega$ to $20\text{-m}\Omega$ typ. sense resistor.

Auto Calibration

The bq30z554-R1 provides an auto-calibration feature to cancel the voltage offset error across SRN and SRP for maximum charge measurement accuracy. The bq30z554-R1 performs auto-calibration when the SMBus lines stay low continuously for a minimum of 5 s.

Temperature

The bq30z554-R1 has an internal temperature sensor and inputs for four external temperature sensors. All five temperature sensor options are enabled individually and configured for cell or FET temperature. Two configurable thermistor models are provided to allow the monitoring of cell temperature in addition to FET temperature, which may be of a higher temperature type.

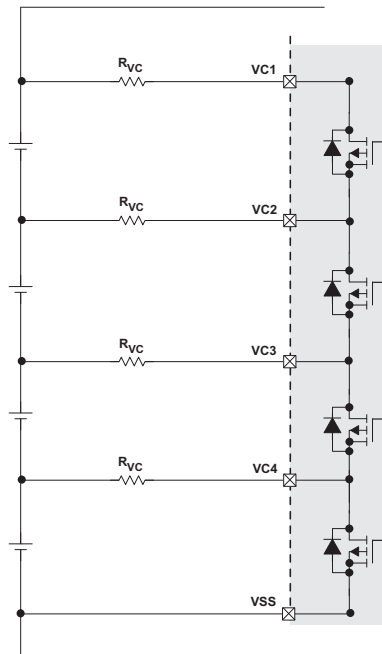
CELL BALANCING

The device supports cell balancing by bypassing the current of each cell during charging or at rest. If the device internal bypass is used, up to 10 mA can be bypassed and multiple cells can be bypassed at the same time. Higher cell balance current can be achieved by using an external cell balancing circuit. In EXTERNAL CELL BALANCING mode, only one cell at a time can be balanced.

The cell balancing algorithm determines the amount of charge needed to be bypassed to balance the capacity of all cells.

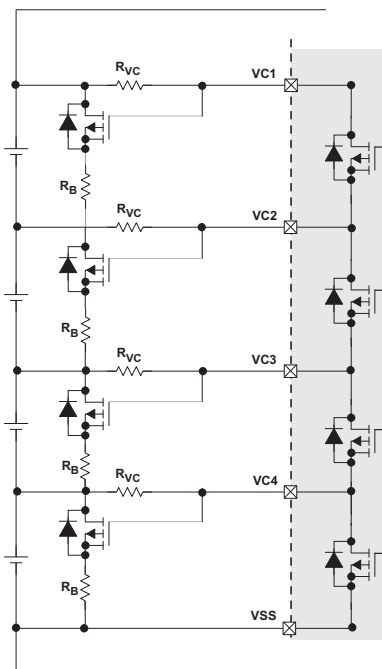
Internal Cell Balancing

When internal cell balancing is configured, the cell balance current is defined by the external resistor R_{VC} at the VCx input.



External Cell Balancing

When internal cell balancing is configured, the cell balance current is defined by R_B . Only one cell at a time can be balanced.



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PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| BQ30Z554DBT-R1 | Active | Production | TSSOP (DBT) 30 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ30Z554 |
| BQ30Z554DBT-R1.A | Active | Production | TSSOP (DBT) 30 | 60 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ30Z554 |
| BQ30Z554DBT-R1.B | Active | Production | TSSOP (DBT) 30 | 60 TUBE | - | Call TI | Call TI | -40 to 85 | |
| BQ30Z554DBTR-R1 | Active | Production | TSSOP (DBT) 30 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ30Z554 |
| BQ30Z554DBTR-R1.A | Active | Production | TSSOP (DBT) 30 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ30Z554 |
| BQ30Z554DBTR-R1.B | Active | Production | TSSOP (DBT) 30 | 2000 LARGE T&R | - | Call TI | Call TI | -40 to 85 | |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ30Z554DBTR-R1 | TSSOP | DBT | 30 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

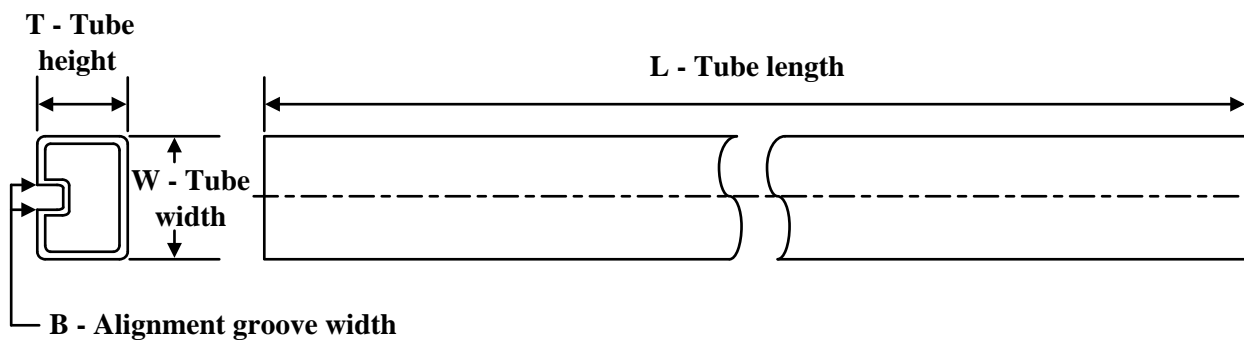
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

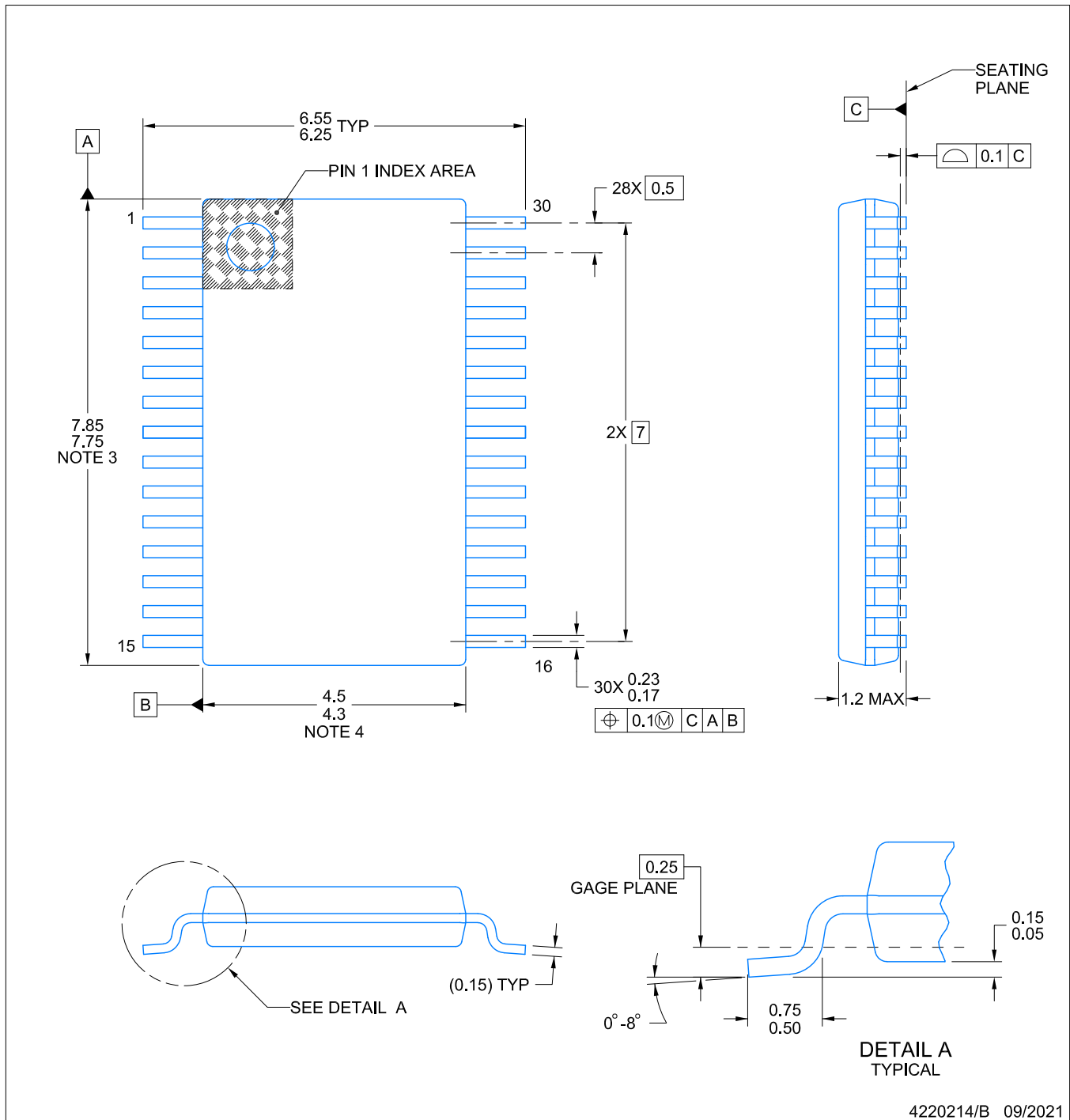
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ30Z554DBTR-R1 | TSSOP | DBT | 30 | 2000 | 350.0 | 350.0 | 43.0 |

TUBE



*All dimensions are nominal

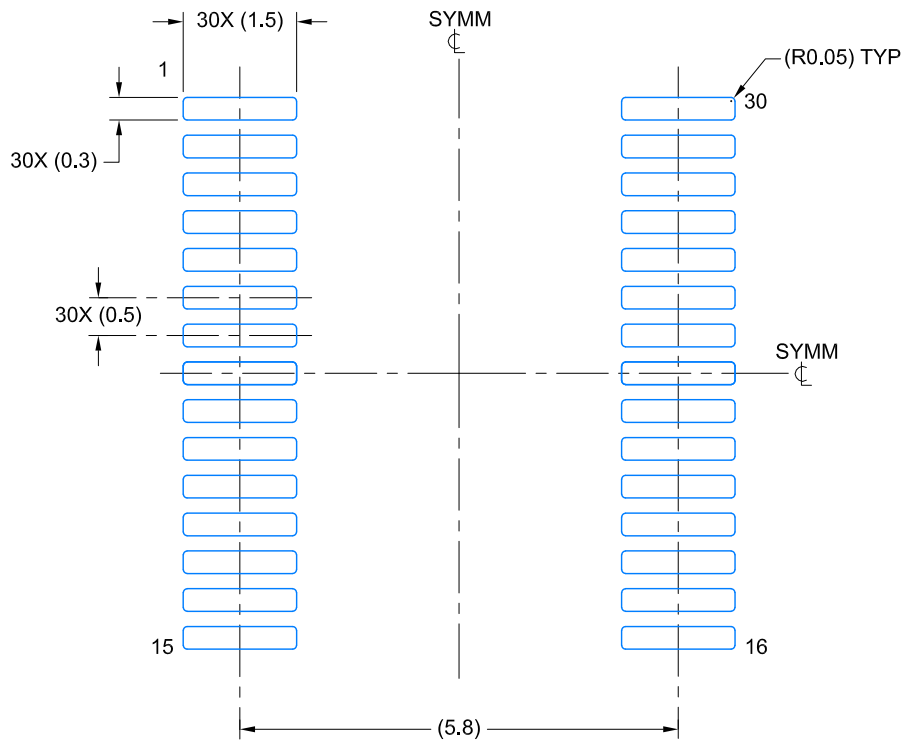
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| BQ30Z554DBT-R1 | DBT | TSSOP | 30 | 60 | 530 | 10.2 | 3600 | 3.5 |
| BQ30Z554DBT-R1.A | DBT | TSSOP | 30 | 60 | 530 | 10.2 | 3600 | 3.5 |



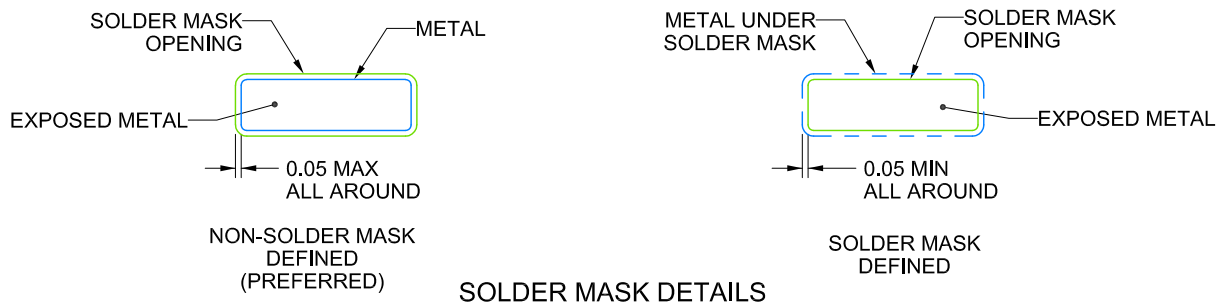
4220214/B 09/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



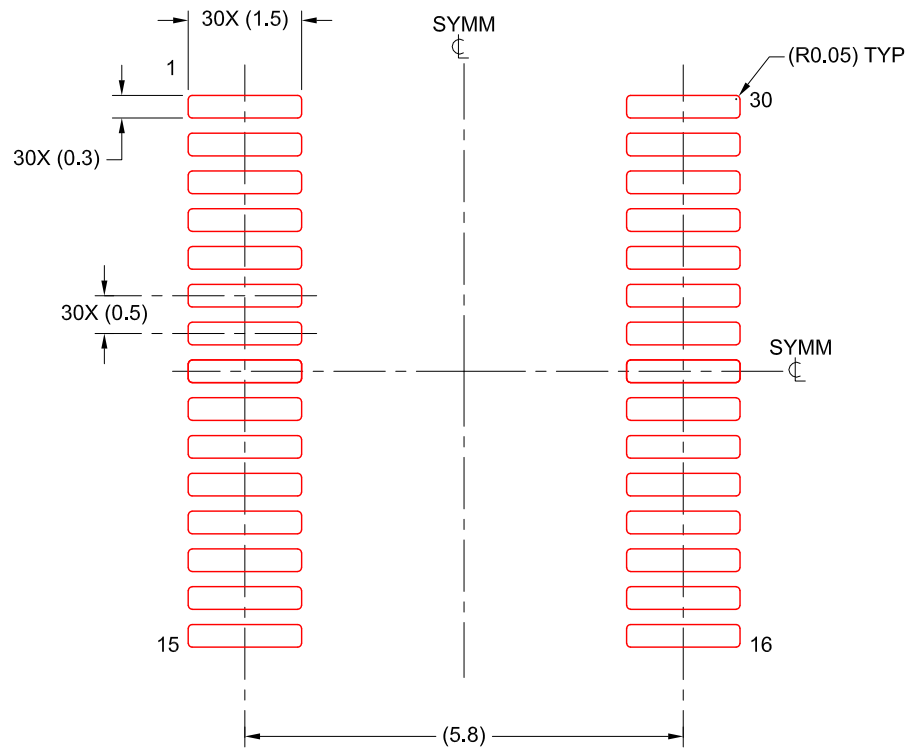
SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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