

3.3V ABT 16-Bit transparent D-type latches (3-State)

74LVT16373A

FEATURES

- 16-bit transparent latch
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset

- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

This device is a 16-bit transparent D-type latch with non-inverting 3-State bus compatible outputs. The device can be used as two 8-bit latches or one 16-bit latch. When enable (E) input is High, the Q outputs follow the data (D) inputs. When enable is taken Low, the Q outputs are latched at the levels of the D inputs one setup time prior to the High-to-Low transition.

DESCRIPTION

The LVT16373A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

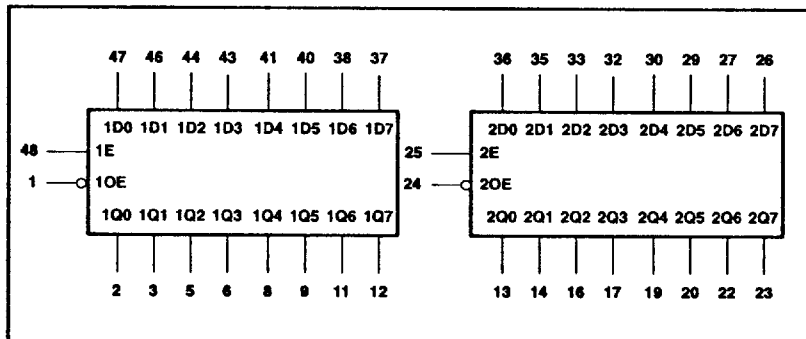
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; $GND = 0V$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	$C_L = 50\text{pF}$; $V_{CC} = 3.3V$		ns
C_{IN}	Input capacitance	$V_I = 0V$ or $3.0V$	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0V$ or $3.0V$	10	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 3.6V$	100	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	-40°C to $+85^{\circ}\text{C}$	74LVT16373ADL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	-40°C to $+85^{\circ}\text{C}$	74LVT16373ADGG	SOT362-1

LOGIC SYMBOL



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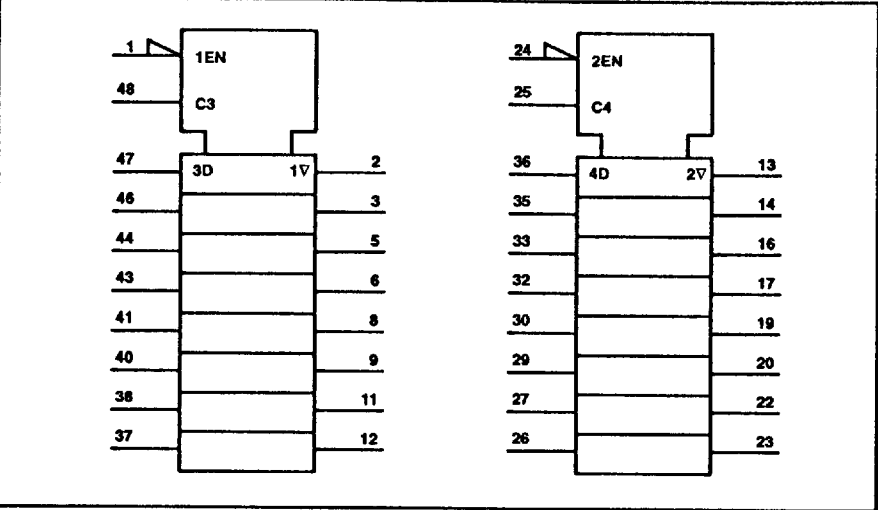
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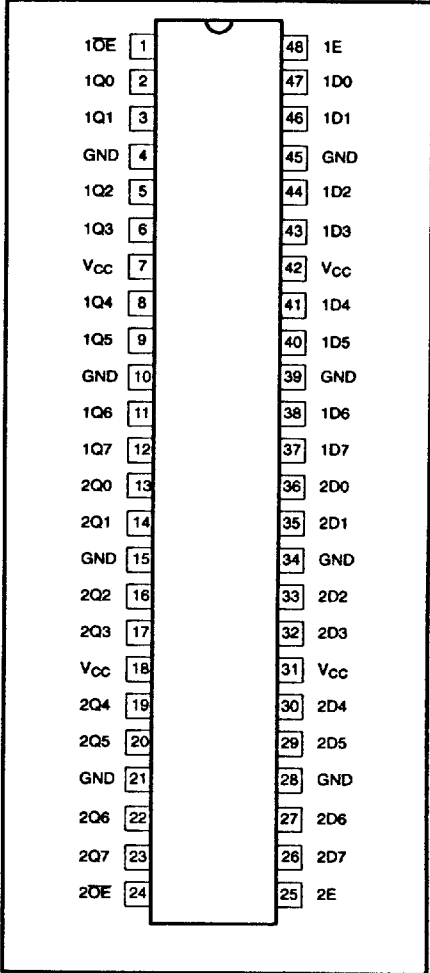
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LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



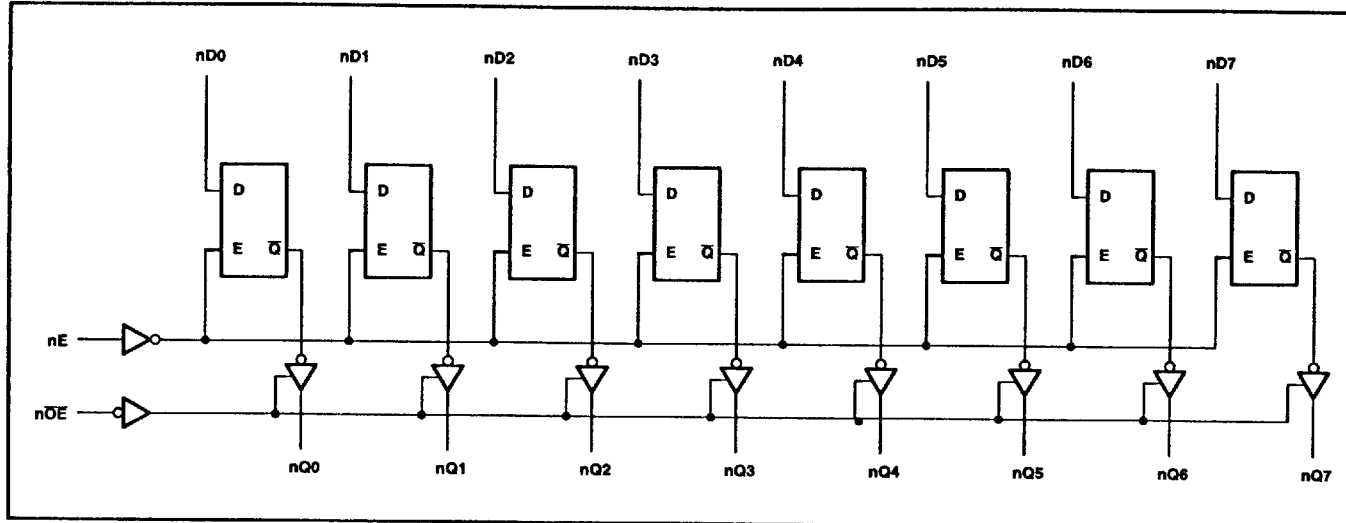
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	1OE, 2OE	Output enable inputs (active-Low)
48, 25	1E, 2E	Enable inputs (active-High)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive supply voltage

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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
nOE	nE	nDx		nQ0 – nQ7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	nDx	nDx	Z	

H = High voltage level

h = High voltage level one set-up time prior to the High-to-Low E transition

L = Low voltage level

l = Low voltage level one set-up time prior to the High-to-Low E transition

NC = No change

X = Don't care

Z = High impedance "off" state

↓ = High-to-Low E transition

ABSOLUTE MAXIMUM RATINGS^{1,2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		–0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	–50	mA
V _I	DC input voltage ³		–0.5 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	–50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	–0.5 to +7.0	V
I _{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T _{stg}	Storage temperature range		–65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1$ kHz		64	
$\Delta t/\Delta V$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			Temp = -40°C to +85°C				
			MIN	TYP ¹	MAX		
V _{IK}	Input clamp voltage	V _{CC} = 2.7V; I _{IK} = -18mA			-1.2	V	
V _{OH}	High-level output voltage	V _{CC} = 2.7 to 3.6V; I _{OH} = -100μA		V _{CC} -0.2		V	
		V _{CC} = 2.7V; I _{OH} = -8mA		2.4			
		V _{CC} = 3.0V; I _{OH} = -32mA		2.0			
V _{OL}	Low-level output voltage	V _{CC} = 2.7V; I _{OL} = 100μA			0.2	V	
		V _{CC} = 2.7V; I _{OL} = 24mA			0.5		
		V _{CC} = 3.0V; I _{OL} = 16mA			0.4		
		V _{CC} = 3.0V; I _{OL} = 32mA			0.5		
		V _{CC} = 3.0V; I _{OL} = 64mA			0.55		
V _{RST}	Power-up output Low voltage ⁵	V _{CC} = 3.6V; I _O = 1mA; V _I = GND or V _{CC}			0.55	V	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND		Control pins		±1	μA
		V _{CC} = 0 or 3.6V; V _I = 5.5V				10	
		V _{CC} = 3.6V; V _I = V _{CC}		Data pins ⁴		1	
		V _{CC} = 3.6V; V _I = 0				-5	
I _{OFF}	Output off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V			±100	μA	
I _{HOLD}	Bus Hold current D inputs	V _{CC} = 3V; V _I = 0.8V			75	μA	
		V _{CC} = 3V; V _I = 2.0V			-75	μA	
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V			125	μA	
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care			±100	μA	
I _{OZH}	3-State output High current	V _{CC} = 3.6V; V _O = 3.0V; V _I = V _{IH} or V _{IL}			5	μA	
I _{OZL}	3-State output Low current	V _{CC} = 3.6V; V _O = 0.5V; V _I = V _{IH} or V _{IL}			-5		
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0			0.12	mA	
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0			5		
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0			0.12		
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND			0.2	mA	

NOTES:

- All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From $V_{CC} = 1.2V$ to $V_{CC} = 3.3V \pm 0.3V$ a transition time of 100 μ sec is permitted. This parameter is valid for $T_{amb} = 25^\circ C$ only.
- Unused pins at V_{CC} or GND.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

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AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP ¹	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2					ns
t_{PLH} t_{PHL}	Propagation delay nE to nQx	1					ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5					ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	4 5					ns

NOTE:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.

AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP	MAX	MIN	
$t_{S(H)}$ $t_{S(L)}$	Setup time nDx to nE	3					ns
$t_{H(H)}$ $t_{H(L)}$	Hold time nDx to nE	3					ns
$t_W(H)$	nE pulse width High	1					ns

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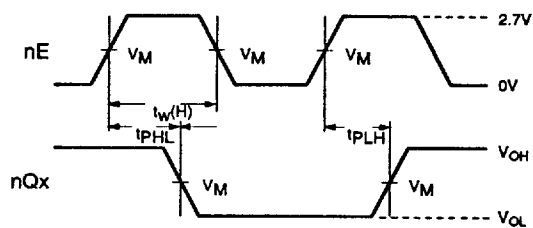
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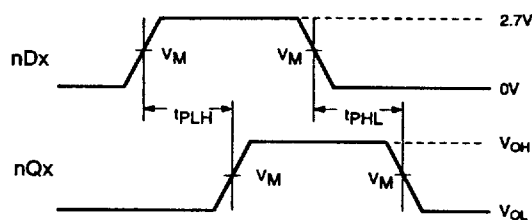
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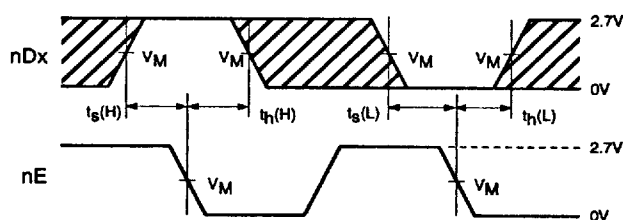
AC WAVEFORMS



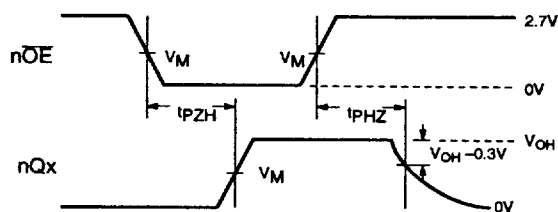
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



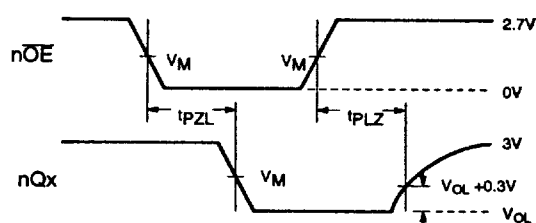
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

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TEST CIRCUIT AND WAVEFORMS

