

54ACT11253, 74ACT11253
DUAL 1-OF-4 DATA SELECTORS/MUXES
WITH 3-STATE OUTPUTS

SCAS040A – D3110, MARCH 1988 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- 3-State Version of 'ACT11153
- Permits Multiplexing From N Lines to One Line
- Performs Parallel-to-Serial Conversion
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe (\bar{G}). The outputs are disabled when \bar{G} is high.

The 54ACT11253 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT11253 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

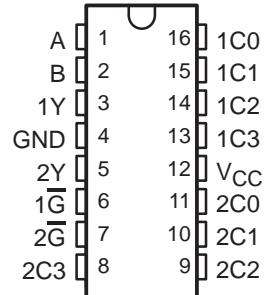
SELECT INPUTS	DATA INPUTS				OUTPUT CONTROL G	OUTPUT Y
	B	A	C0	C1	C2	C3
X X	X	X	X	X	X	Z
L L	L	X	X	X	L	L
L L	H	X	X	X	L	H
L H	X	L	X	X	L	L
L H	X	H	X	X	L	H
H L	X	X	L	X	L	L
H L	X	X	H	X	L	H
H H	X	X	X	L	L	L
H H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

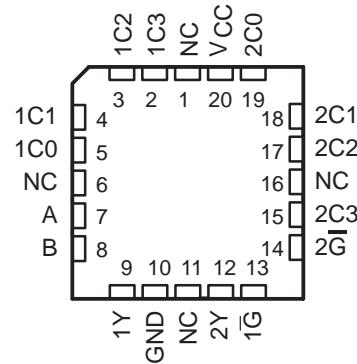
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54ACT11253 . . . J PACKAGE
74ACT11253 . . . D OR N PACKAGE
(TOP VIEW)

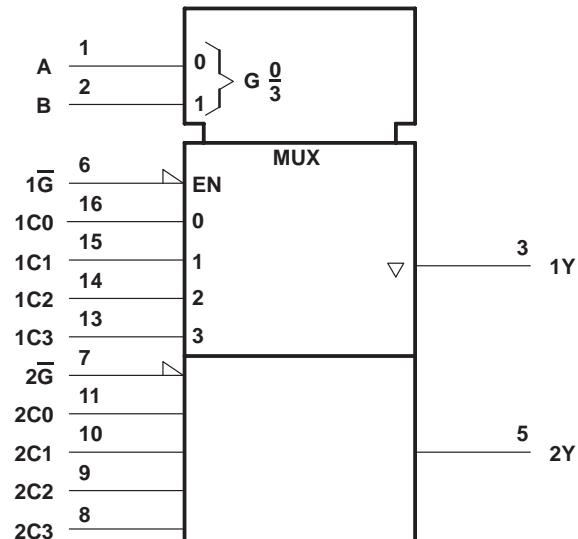


54ACT11253 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

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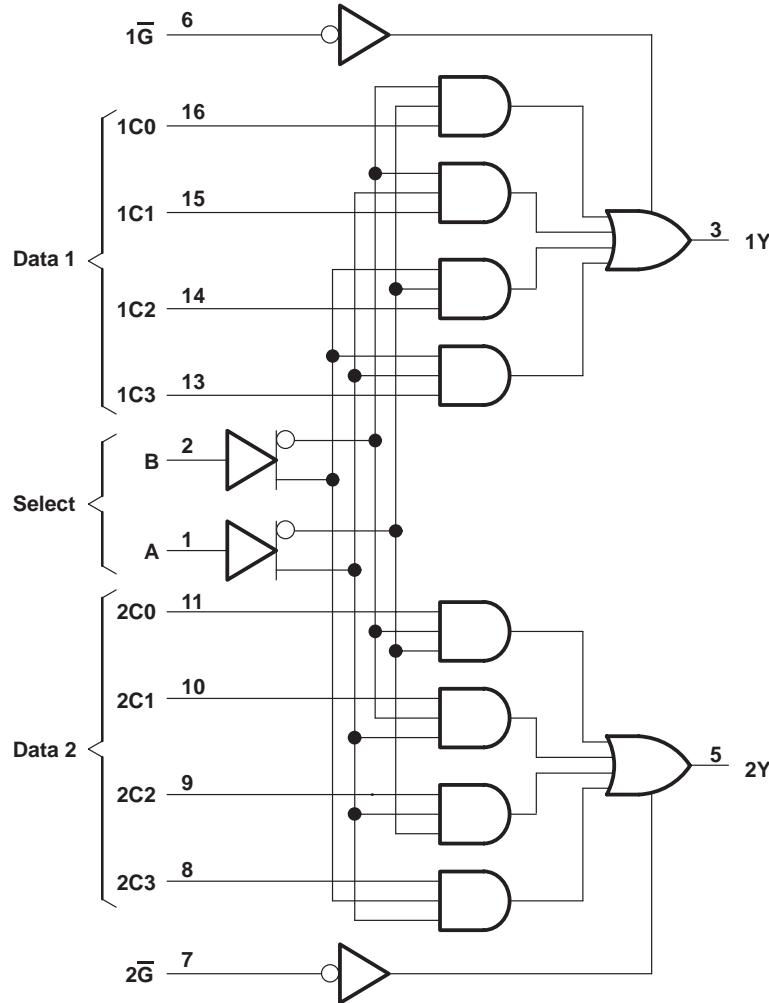
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logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

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recommended operating conditions

		54ACT11253		74ACT11253		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		-24		-24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ C$			54ACT11253	74ACT11253	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50 \mu A$	4.5 V	4.4			4.4	4.4	V
		5.5 V	5.4			5.4	5.4	
	$I_{OH} = -24 mA$	4.5 V	3.94			3.7	3.8	
		5.5 V	4.94			4.7	4.8	
	$I_{OH} = -50 mA^\dagger$	5.5 V				3.85		
V_{OL}	$I_{OL} = 50 \mu A$	4.5 V		0.1		0.1	0.1	V
		5.5 V		0.1		0.1	0.1	
	$I_{OL} = 24 mA$	4.5 V		0.36		0.5	0.44	
		5.5 V		0.36		0.5	0.44	
	$I_{OL} = 50 mA^\dagger$	5.5 V				1.65		
I_{OZ}	$V_O = V_{CC}$ or GND	4.5 V						μA
		5.5 V						
	I_I	4.5 V		± 0.5		± 10	± 5	
		5.5 V		± 0.1		± 1	± 1	
	I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		8	160	80	μA
ΔI_{CC}^\ddagger	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.9		1	1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5				pF
C_o	$V_O = V_{CC}$ or GND	5 V		8				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

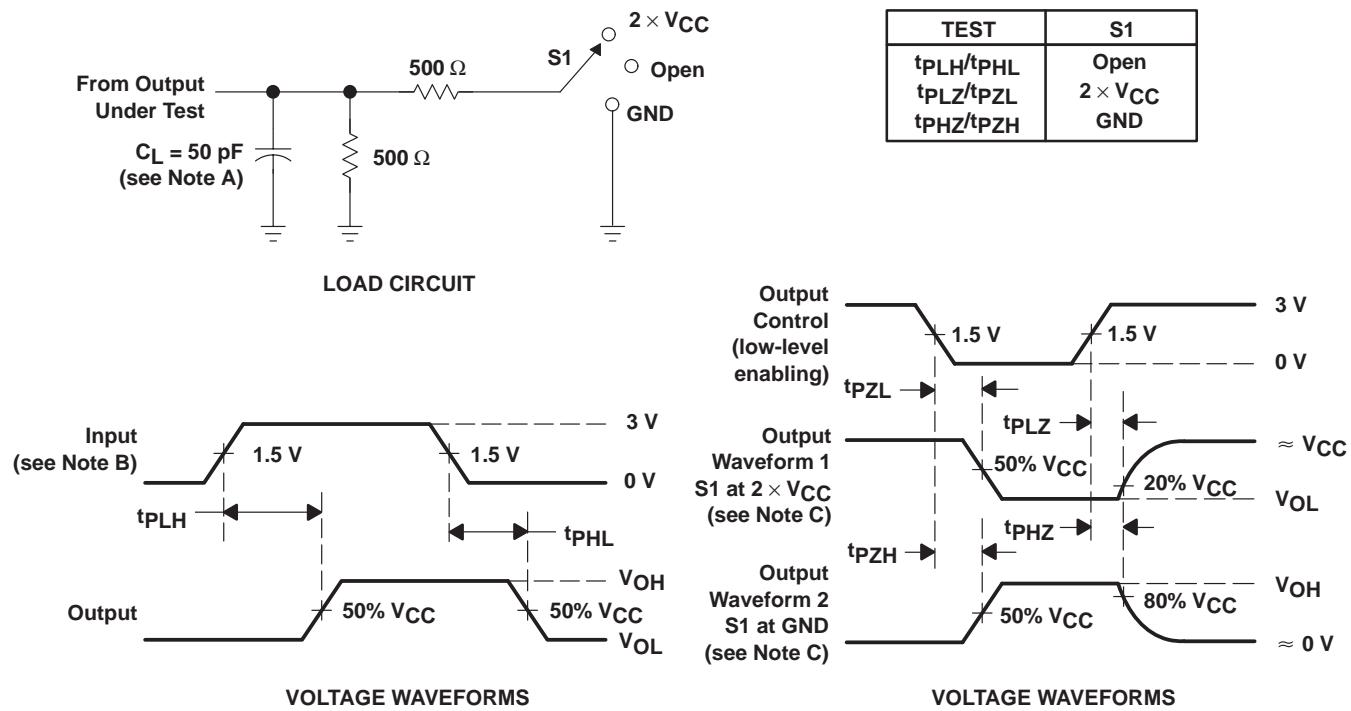
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TA = 25°C			54ACT11253	74ACT11253	UNIT	
			MIN	TYP	MAX	MIN	MAX		
tPLH	A or B	Any Y	1.5	6.8	9.8	1.5	11.8	1.5	11
tPHL			1.5	9.1	12.6	1.5	15.5	1.5	14.3
tPLH	Data (Any C)	Y	1.5	5.7	7.4	1.5	8.9	1.5	8.3
tPHL			1.5	7.2	10.5	1.5	12.5	1.5	11.7
tPZH	G	Y	1.5	5	7.6	1.5	9	1.5	8.5
tPZL			1.5	4.8	7.3	1.5	8.6	1.5	8.1
tPHZ	G	Y	1.5	6.4	8.6	1.5	9.5	1.5	9.2
tPLZ			1.5	5.9	7.4	1.5	8.1	1.5	7.8

operating characteristics, V_{CC} = 5 V, TA = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
	Outputs enabled	Outputs disabled		
C _{pd} Power dissipation capacitance per multiplexer	C _L = 50 pF, f = 1 MHz		42	pF
			18	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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