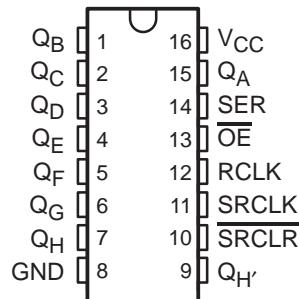


- 8-Bit Serial-In, Parallel-Out Shift
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Shift Register Has Direct Clear

DW, E, M, NS, OR SM PACKAGE  
(TOP VIEW)



### description/ordering information

The CD74HC595 device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial output for cascading. When the output-enable (OE) input is high, the outputs are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	PDIP – E	Tube of 25	CD74HC595E	CD74HC595E
	SOIC – DW	Tube of 40	CD74HC595DW	HC595M
		Reel of 2000	CD74HC595DWR	
	SOIC – M	Tube of 40	CD74HC595M	HC595M
		Reel of 2500	CD74HC595M96	
		Reel of 250	CD74HC595MT	
	SOP – NS	Reel of 2000	CD74HC595NSR	HC595M
	SSOP – SM	Tube of 80	CD74HC595SM	HJ595
		Reel of 2000	CD74HC595SM96	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

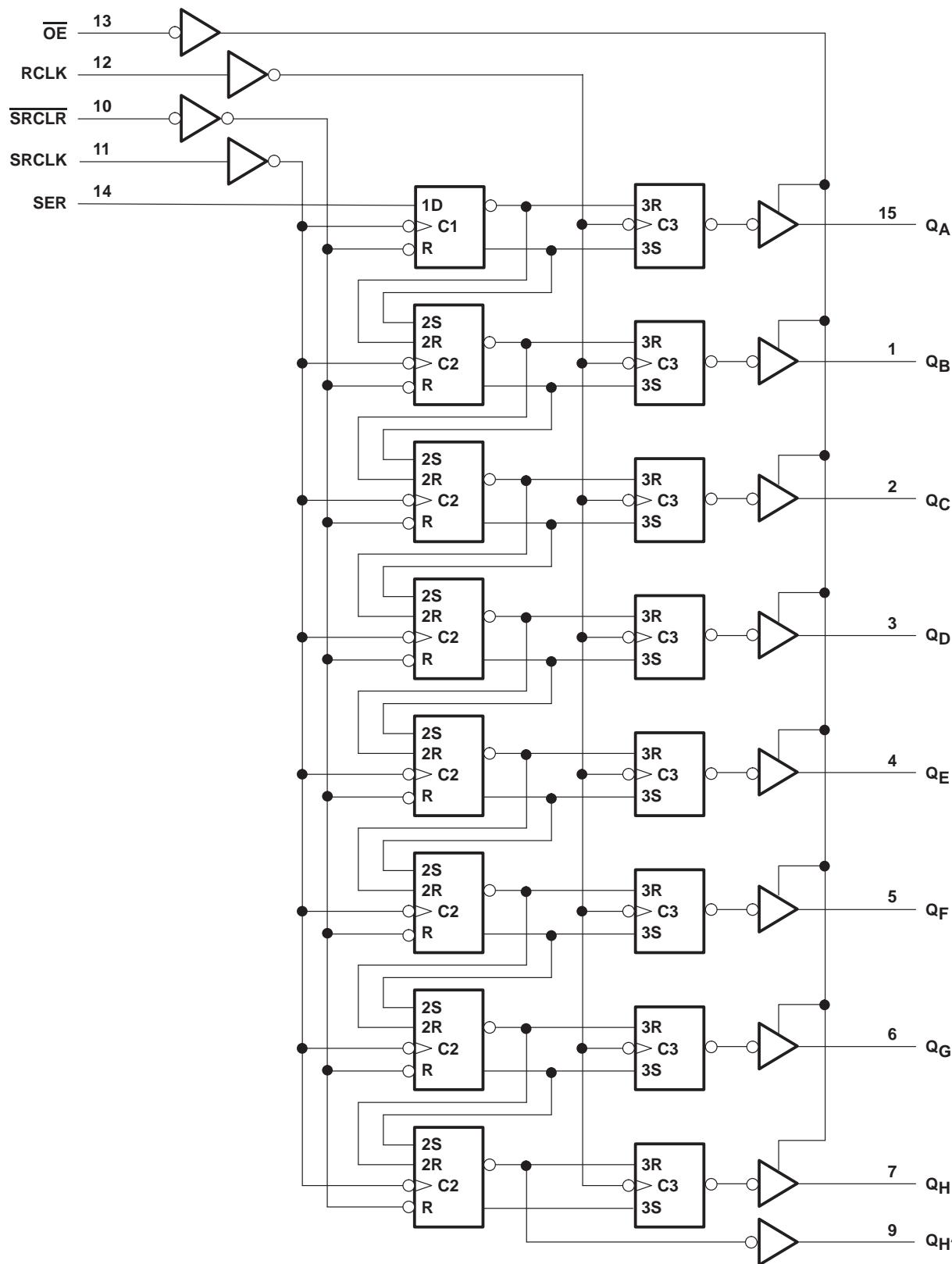
**CD74HC595**  
**8-BIT SHIFT REGISTERS**  
**WITH 3-STATE OUTPUT REGISTERS**

SCHS353 – JANUARY 2004

FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	OE	
X	X	X	X	H	Outputs Q <sub>A</sub> –Q <sub>H</sub> are disabled.
X	X	X	X	L	Outputs Q <sub>A</sub> –Q <sub>H</sub> are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.

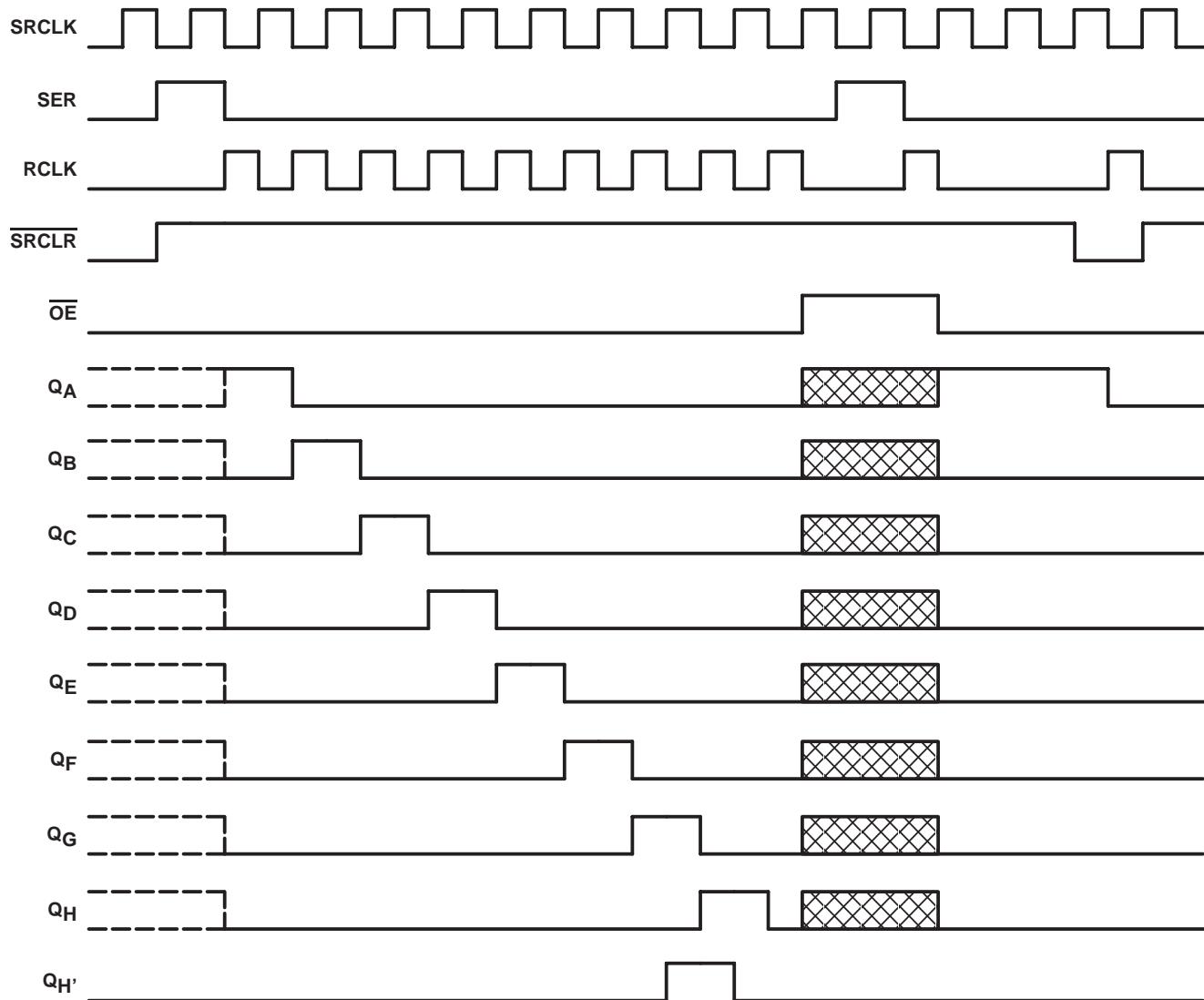
logic diagram (positive logic)



**CD74HC595**  
**8-BIT SHIFT REGISTERS**  
**WITH 3-STATE OUTPUT REGISTERS**

SCHS353 – JANUARY 2004

**timing diagram**



NOTE: implies that the output is in 3-State mode.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### **recommended operating conditions (see Note 3)**

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5			V
		V <sub>CC</sub> = 4.5 V	3.15			
		V <sub>CC</sub> = 6 V	4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V			0.5	V
		V <sub>CC</sub> = 4.5 V			1.35	
		V <sub>CC</sub> = 6 V			1.8	
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>		V
Δt/Δv <sup>†</sup>	Input transition rise/fall time	V <sub>CC</sub> = 2 V			1000	ns
		V <sub>CC</sub> = 4.5 V			500	
		V <sub>CC</sub> = 6 V			400	
T <sub>A</sub>	Operating free-air temperature		-55		125	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

‡ If this device is used in the threshold region (from  $V_{IL\max} = 0.5\text{ V}$  to  $V_{IL\min} = 1.5\text{ V}$ ), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_t = 1000\text{ ns}$  and  $V_{CC} = 2\text{ V}$  does not damage the device; however, functionally, the  $\text{Cl}$   $\text{K}$  inputs are not ensured while in the shift, count, or toggle operating modes.

**CD74HC595**  
**8-BIT SHIFT REGISTERS**  
**WITH 3-STATE OUTPUT REGISTERS**

SCHS353 – JANUARY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 µA	2 V	1.9	1.998	1.9		1.9		V
			4.5 V	4.4	4.499	4.4		4.4		
			6 V	5.9	5.999	5.9		5.9		
		Q <sub>H'</sub> , I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3	3.7		3.84		
				3.98	4.3	3.7		3.84		
		Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OH</sub> = -6 mA	6 V	5.48	5.8	5.2		5.34		
				5.48	5.8	5.2		5.34		
		Q <sub>H'</sub> , I <sub>OH</sub> = -5.2 mA	6 V	0.002	0.1	0.1		0.1		
				0.001	0.1	0.1		0.1		
				0.001	0.1	0.1		0.1		
				0.17	0.26	0.4		0.33		
				0.17	0.26	0.4		0.33		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA	4.5 V	0.15	0.26	0.4		0.33		V
				0.15	0.26	0.4		0.33		
				0.15	0.26	0.4		0.33		
		Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OL</sub> = 6 mA	6 V	0.17	0.26	0.4		0.33		
				0.17	0.26	0.4		0.33		
				0.17	0.26	0.4		0.33		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V		±0.1	±100	±1000		±1000		nA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0, Q <sub>A</sub> -Q <sub>H</sub>	6 V		±0.01	±0.5	±10		±5		µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8	160		80		µA
C <sub>i</sub>		2 V to 6 V		3	10	10		10		pF

CD74HC595  
8-BIT SHIFT REGISTERS  
WITH 3-STATE OUTPUT REGISTERS  
SCHS353 – JANUARY 2004

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		$V_{CC}$	$T_A = 25^\circ C$		$T_A = -55^\circ C$ TO $125^\circ C$		$T_A = -40^\circ C$ TO $85^\circ C$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency	2 V	6		4.2		5		MHz
		4.5 V		31		21		25	
		6 V		36		25		29	
$t_W$	Pulse duration	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	<u>SRCLR</u> low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
$t_{SU}$	SER before $SRCLK^\uparrow$	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
	$SRCLK^\uparrow$ before $RCLK^{\uparrow\uparrow}$	2 V	75		113		94		
		4.5 V	15		23		19		
		6 V	13		19		16		
	<u>SRCLR</u> low before $RCLK^\uparrow$	2 V	50		75		65		
		4.5 V	10		15		13		
		6 V	9		13		11		
	<u>SRCLR</u> high (inactive) before $SRCLK^\uparrow$	2 V	50		75		60		
		4.5 V	10		15		12		
		6 V	9		13		11		
$t_H$	Hold time, SER after $SRCLK^\uparrow$	2 V	0		0		0		ns
		4.5 V	0		0		0		
		6 V	0		0		0		

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

**CD74HC595**  
**8-BIT SHIFT REGISTERS**  
**WITH 3-STATE OUTPUT REGISTERS**

SCHS353 – JANUARY 2004

switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C} \text{ TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C} \text{ TO } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$				2 V	6	26	4.2		5		MHz
				4.5 V	31	38	21		25		
				6 V	36	42	25		29		
$t_{pd}$	SRCLK	$Q_{H'}$		2 V	50	160	240		200		ns
				4.5 V	17	32	48		40		
				6 V	14	27	41		34		
	RCLK	$Q_A-Q_H$		2 V	50	150	225		187		
				4.5 V	17	30	45		37		
				6 V	14	26	38		32		
$t_{PHL}$	SRCLR	$Q_{H'}$		2 V	51	175	261		219		ns
				4.5 V	18	35	52		44		
				6 V	15	30	44		37		
$t_{en}$	$\overline{OE}$	$Q_A-Q_H$		2 V	40	150	225		187		ns
				4.5 V	15	30	45		37		
				6 V	13	26	38		32		
$t_{dis}$	$\overline{OE}$	$Q_A-Q_H$		2 V	42	200	300		250		ns
				4.5 V	23	40	60		50		
				6 V	20	34	51		43		
$t_t$		$Q_A-Q_H$		2 V	28	60	90		75		ns
				4.5 V	8	12	18		15		
				6 V	6	10	15		13		
		$Q_{H'}$		2 V	28	75	110		95		
				4.5 V	8	15	22		19		
				6 V	6	13	19		16		

switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C} \text{ TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C} \text{ TO } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	RCLK	$Q_A-Q_H$		2 V	60	200	300		250		ns
				4.5 V	22	40	60		50		
				6 V	19	34	51		43		
$t_{en}$	$\overline{OE}$	$Q_A-Q_H$		2 V	70	200	298		250		ns
				4.5 V	23	40	60		50		
				6 V	19	34	51		43		
$t_t$		$Q_A-Q_H$		2 V	45	210	315		265		ns
				4.5 V	17	42	63		53		
				6 V	13	36	53		45		

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load	400	pF

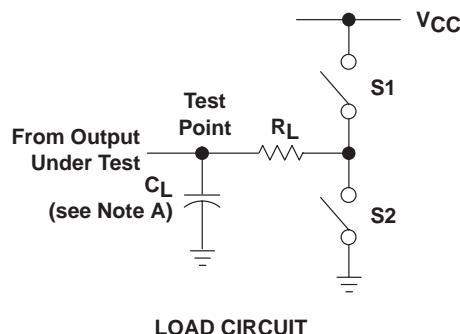
# CD74HC595

## 8-BIT SHIFT REGISTERS

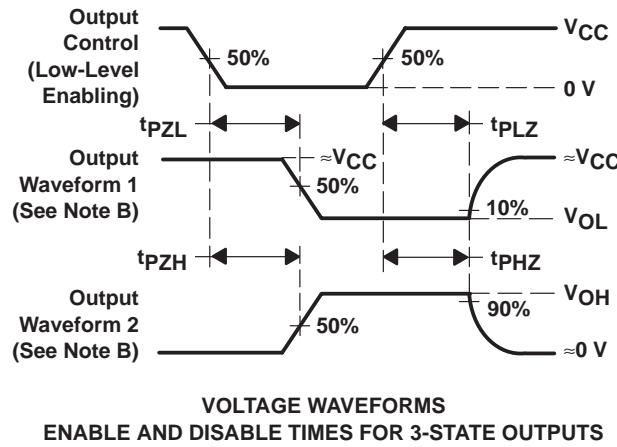
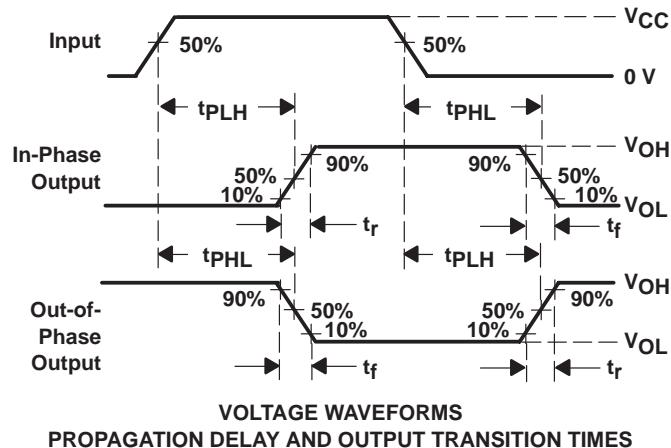
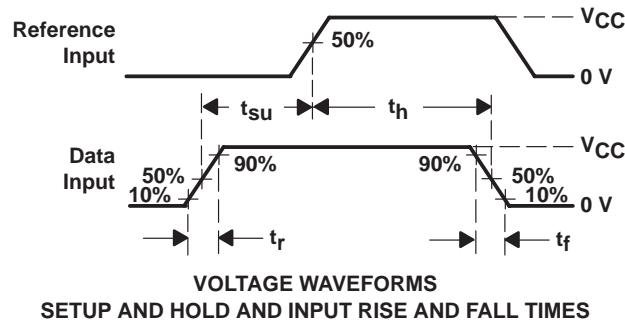
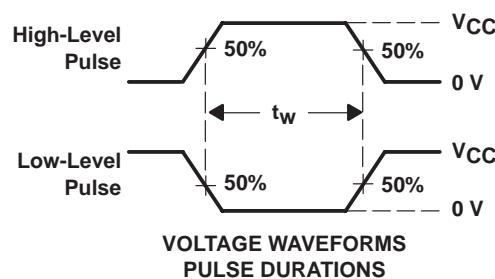
### WITH 3-STATE OUTPUT REGISTERS

SCHS353 – JANUARY 2004

#### PARAMETER MEASUREMENT INFORMATION



PARAMETER	$R_L$	$C_L$	S1	S2
$t_{en}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
			Closed	Open
$t_{dis}$	1 k $\Omega$	50 pF	Open	Closed
			Closed	Open
$t_{pd}$ or $t_t$	--	50 pF or 150 pF	Open	Open



NOTES:

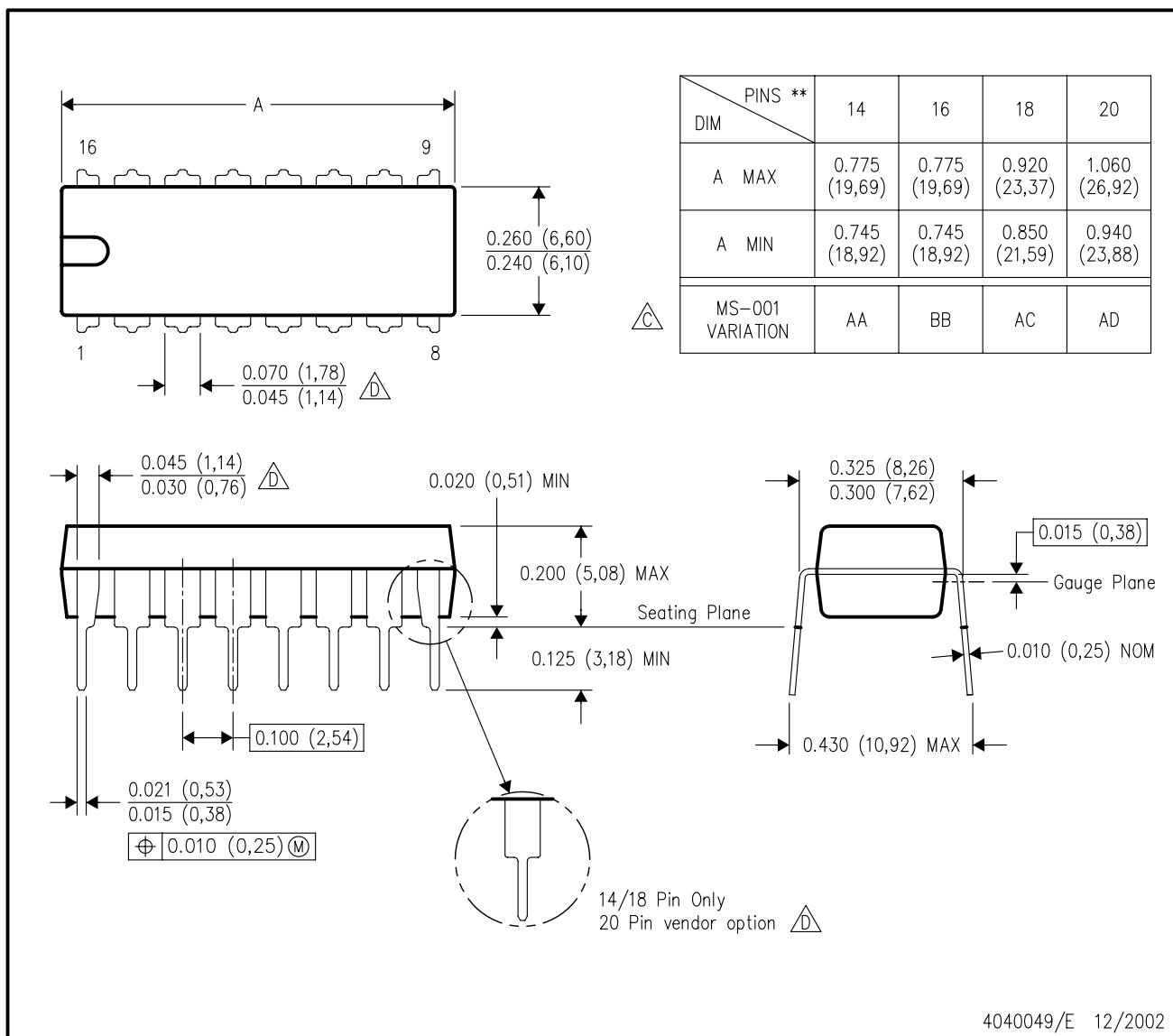
- $C_L$  includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
- For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
- The outputs are measured one at a time, with one input transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

## N (R-PDIP-T\*\*)

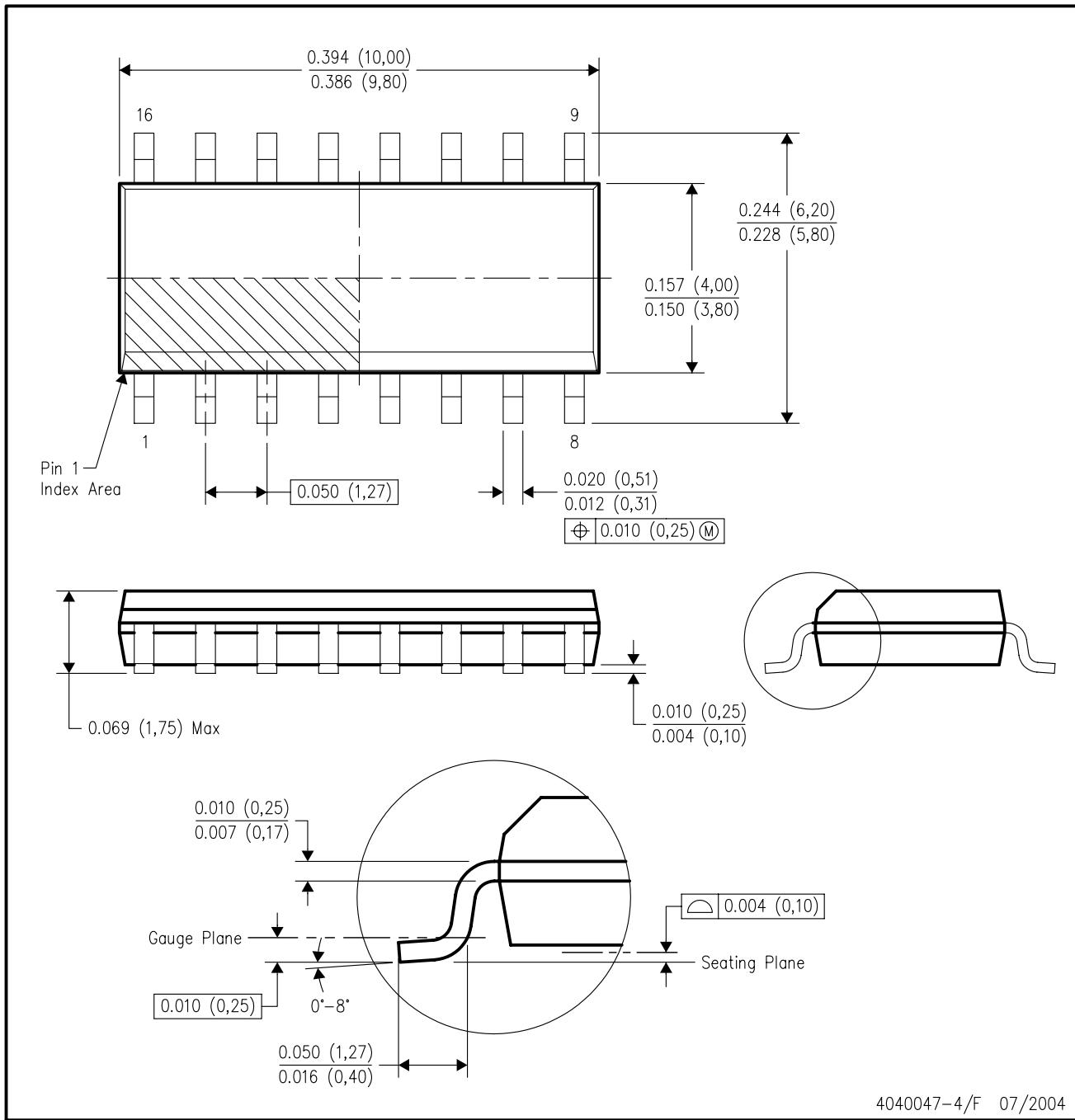
16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE

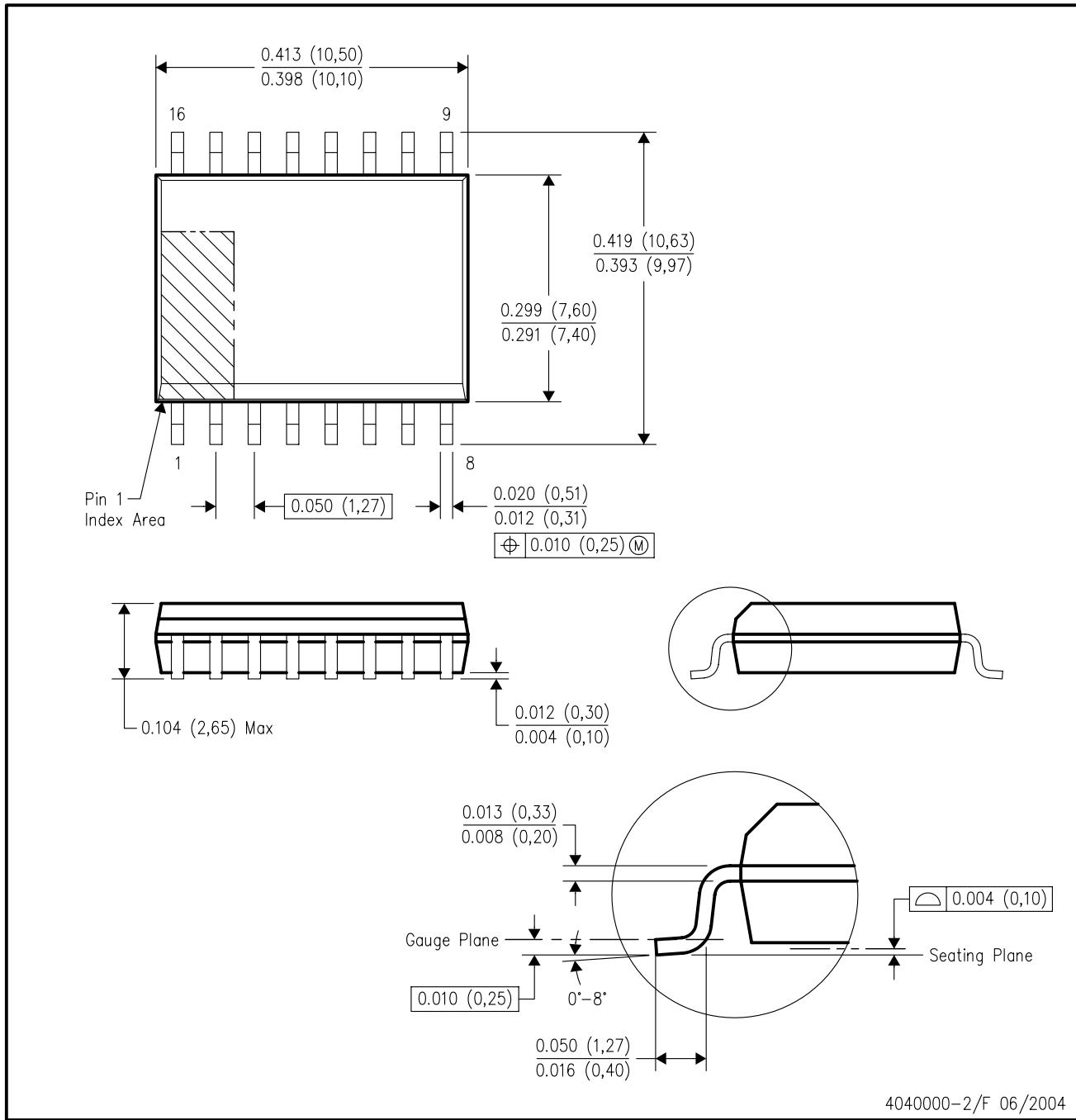


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AC.

## DW (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

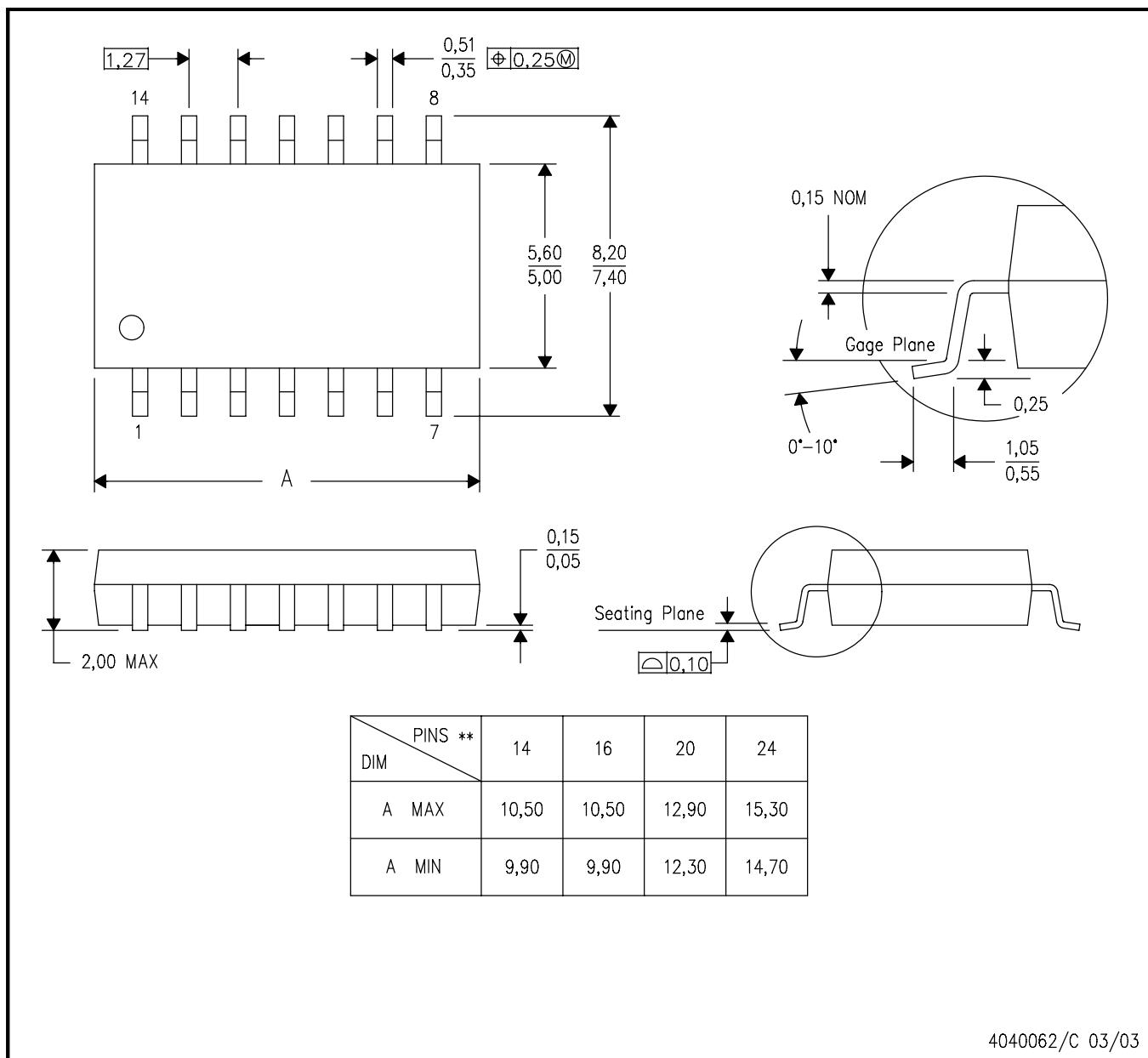
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-013 variation AA.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



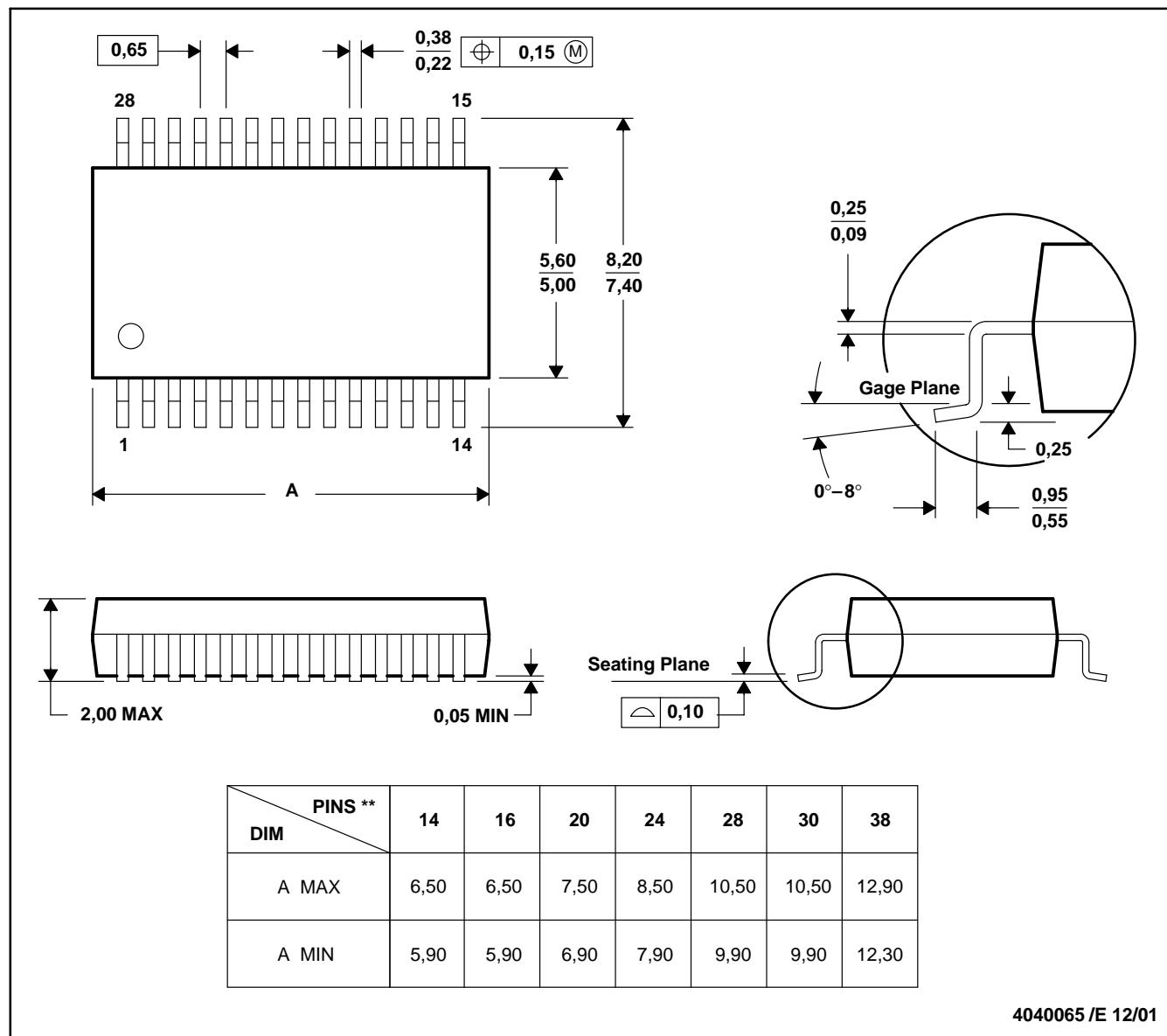
NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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