ISL9123, ISL9123A, ISL9123B

Ultra-Low IQ Buck Regulator with Bypass

The ISL9123, ISL9123A, and ISL9123B are highly integrated buck switching regulators capable of supplying output voltage down to 0.4V. The device features an extremely low quiescent current consumption of 950nA in Regulation mode, 140nA in Forced Bypass mode (ISL9123/A), and 7nA in Shutdown mode. It supports input voltages from 1.8V to 5.5V.

The ISL9123/A device has automatic bypass functionality for situations in which the input voltage is close to or below the output voltage. In addition to the automatic bypass functionality, the Forced Bypass power saving mode can be chosen if voltage regulation is not required. Forced Bypass power saving mode is accessible using the I^2C interface bus.

The device is capable of delivering up to 600mA of output current (V_{IN} > 2.5V) and provides excellent efficiency because of its adaptive frequency hysteretic control architecture.

The device is designed for stand-alone applications and supports a default output voltage at Power-On Reset (POR). After POR, the output voltage can be adjusted in the range of 0.4V to 5.375V for (ISL9123/A) and to 1.180V (for ISL9123B) by using the I^2C interface bus. Specific default output voltages are available upon request.

The device requires only a single EIA 0603 size inductor and a minimum of two external capacitors. Power supply solution size is minimized by a 1.8mm×1.0mm 8 Bump WLCSP.

Features

- 950nA quiescent current
- 86% efficiency at 10µA load (V_{IN} = 3.6V, V_{OUT} = 3.3V) (ISL9123/A)
- 97% peak efficiency (V_{IN} = 3.6V, V_{OUT} = 3.3V) (ISL9123/A)
- Input voltage range: 1.8V to 5.5V
- Output voltage range: 0.4V to 5.375V (ISL9123/A)
- Output voltage range: 0.4V to 1.180V (ISL9123B)
- Output current: up to 600mA (V_{IN} > 2.5V)
- Selectable Forced and Auto Bypass power saving modes (ISL9123/A only)
- PFM and PWM modes with seamless transition
- I^2C control and voltage adjustability
- Hysteretic controller
- Auxiliary switched output (ISL9123/A only)
- Small 1.8mm×1.0mm 8 Bump WLCSP

Applications

- Smart watches and wristband devices
- Wireless earphones
- Internet of Things (IoT) devices
- Water, gas, and oil meters
- Portable medical devices
- Hearing aid devices

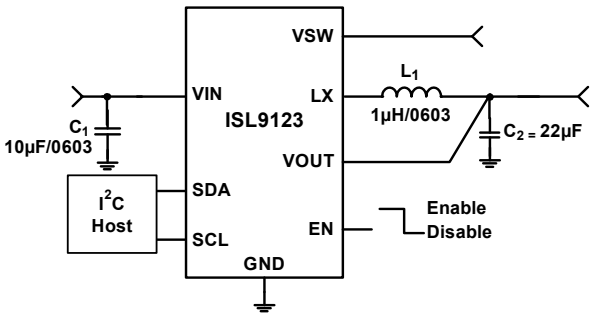

Figure 1. Typical Application (Minimum derated C_2 = 6µF)

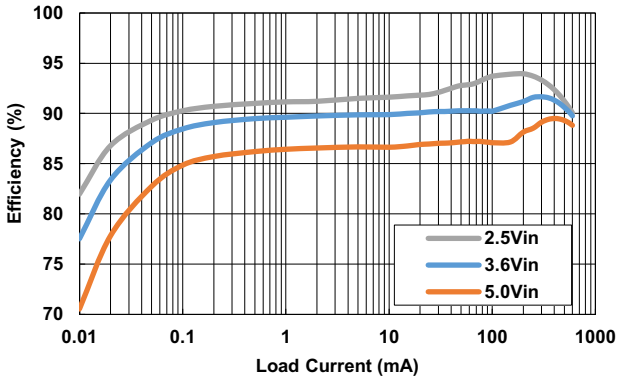

Figure 2. Efficiency vs Load Current: V_{OUT} = 1.8V, T_A = +25°C (ISL9123/A)

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1.1 Block Diagrams

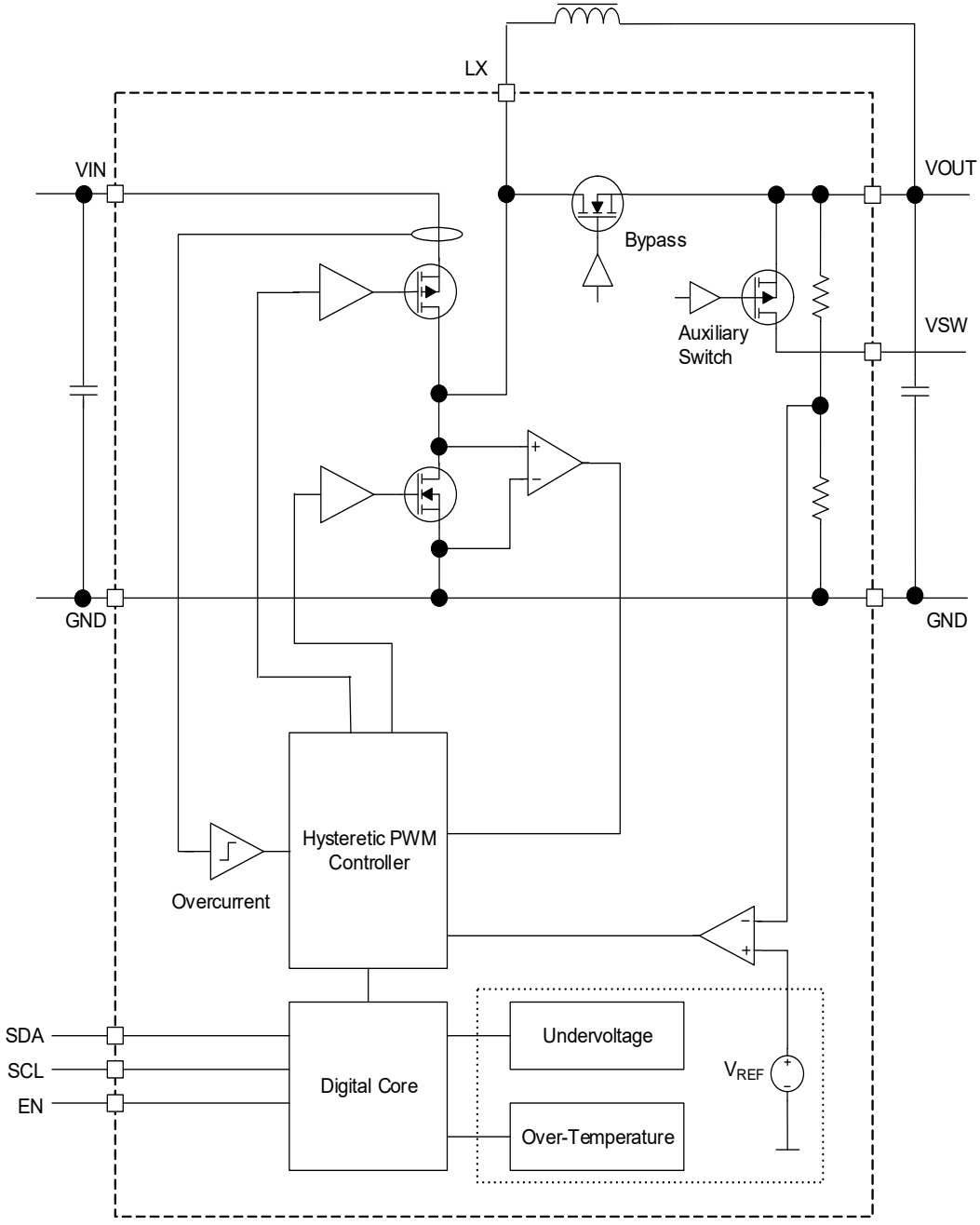


Figure 3. ISL9123/A Block Diagram

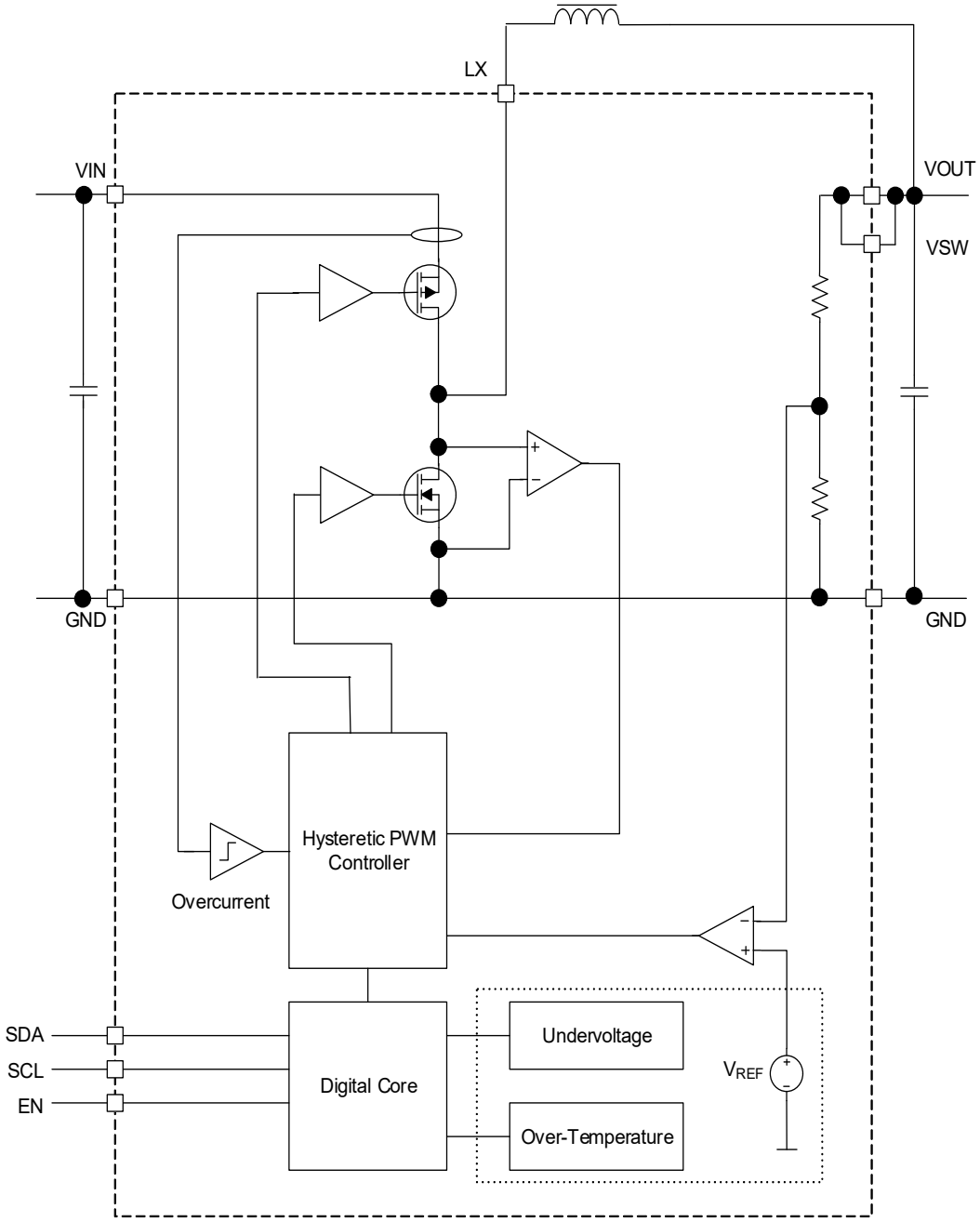
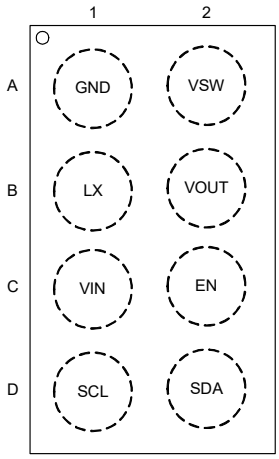


Figure 4. ISL9123B Block Diagram

2. Pin Information

2.1 Pin Assignments



8 Bump WLCSP
Top View

2.2 Pin Descriptions

WLCSP Ball Number	Pin Names	Description
A1	GND	Ground connection
A2 (ISL9123/A)	VSW	Auxiliary output. Leave floating if unused, see Auxiliary Output (ISL9123/A only).
A2 (ISL9123B)	VSW	Internally shorted to VOUT. Leave floating, or connect to VOUT on PCB. Do not use this pin in lieu of VOUT.
B1	LX	Inductor connection
B2	VOUT	Buck output
C1	VIN	Power supply input
C2	EN	Logic input, drive HIGH to enable device. Do not leave floating
D1	SCL	I^2C clock input. Pull down to GND if not being used. Do not leave floating
D2	SDA	I^2C data input. Pull down to GND if not being used. Do not leave floating

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN, VOUT	-0.3	6.5	V
LX	-0.3	6.5	V
LX (less than 10ns)	-2.0	8.0	V
All Other Pins	-0.3	6.5	V
Maximum Junction Temperature	-	+125	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2017)	-	2	kV
Charged Device Model (Tested per JS-002-2014)	-	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Bump WLCSP Package	θ_{JA}[1]	Junction to ambient	110	°C/W
		θ_{JB}[2]	Junction to base	28	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JB}, the board temperature is taken on the board near the edge of the package, on a copper trace at the center of one side. See TB379.

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature (T_A) Range	-40	+85	°C
Supply Voltage (V_{IN}) Range	1.8	5.5	V
Output Voltage (V_{OUT}) Range (ISL9123/A)	0.4	5.375	V
Output Voltage (V_{OUT}) Range (ISL9123B)	0.4	1.180	V
Load Current (I_{OUT}) Range (DC)	0	600	mA
Effective Output Capacitance (C_{OUT})[1]	6	-	µF
Effective Input Capacitance (C_{IN})[1]	5	-	µF

1. Refer to *ISL9123 Evaluation Board Manual* for the reference design and recommended components.

3.4 Analog Specifications

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 1.8V (ISL9123/A), V_{OUT} = 0.7V (ISL9123B), I^2C pull-up voltage = 3.6V, L_1 = 1µH, C_1 = 10µF, C_2 = C_{OUT}(effective) = 6µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range (-40°C to +85°C) and input voltage range (1.8V to 5.5V), unless specified otherwise.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Power Supply						
Input Voltage Range	V_{IN}	-	**1.8**	-	**5.5**	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} rising	-	-	**1.791**	V
V_{UVLO} Hysteresis	$HYST_{UVLO}$	-	-	100	-	mV
V_{IN} Quiescent Current	I_Q	V_{IN} = 3.6V, I_{OUT} = 0A[2]	-	950	**1800**	nA
V_{IN} Supply Current, Shutdown (ISL9123/A)	I_{SD}	V_{IN} = 3.6V, V_{EN} pulled to GND	-	7	**450**	nA
V_{IN} Supply Current, Shutdown (ISL9123B)		V_{IN} = 3.6V, V_{EN} pulled to GND		7.5	**125**	nA
V_{IN} Supply Current, Soft Shutdown	I_{SSD}	V_{IN} = 3.6V, Shutdown using I^2C register. EN_AND = CONV_CFG[7] = 0	-	30	**450**	nA
V_{IN} Supply Current, Forced Bypass Mode (ISL9123/A only)	I_{BYP}	V_{IN} = 3.6V, I_{OUT} = 0A. Forced Bypass using I^2C register. FMODE = CONV_CFG[3:2] = 0x3	-	140	**850**	nA
Output Voltage Regulation						
Output Voltage Range, Buck Mode[3] (ISL9123/A)	V_{OUT}	V_{IN} > V_{SET}, I_{OUT} = 1mA	**0.4**	-	**5.375**	V
Output Voltage Range, Buck Mode[3] (ISL9123B)	V_{OUT}	V_{IN} > V_{SET}, I_{OUT} = 1mA	**0.4**	-	**1.180**	V
Output Voltage Accuracy						
ISL9123IICZ, ISL9123AIICZ	V_{OUT_ACC}	V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 0A, forced PWM	-2.5	-	+2.5	%
		V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 1mA, PFM	-3.6	-	+3.6	%
ISL9123IINZ		V_{IN} = 3.6V, V_{OUT} = 3.0V, I_{OUT} = 0A, forced PWM	-2.0	-	+2.0	%
		V_{IN} = 3.6V, V_{OUT} = 3.0V, I_{OUT} = 1mA, PFM	-3.6	-	+3.6	%
ISL9123II4Z		V_{IN} = 3.6V, V_{OUT} = 1.0V, I_{OUT} = 0A, forced PWM	-65	-	+65	mV
		V_{IN} = 3.6V, V_{OUT} = 1.0V, I_{OUT} = 1mA, PFM	-80	-	+80	mV
ISL9123II2Z	-	V_{IN} = 3.6V, V_{OUT} = 2.1V, I_{OUT} = 0A, forced PWM	-2.5	-	+2.5	%
		V_{IN} = 3.6V, V_{OUT} = 2.1V, I_{OUT} = 1mA, PFM	-3.6	-	+3.6	%
ISL9123IITZ	-	V_{IN} = 3.6V, V_{OUT} = 1.9V, I_{OUT} = 0A, forced PWM	-2.5	-	+2.5	%
		V_{IN} = 3.6V, V_{OUT} = 1.9V, I_{OUT} = 1mA, PFM	-3.6	-	+3.6	%

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 1.8V (ISL9123/A), V_{OUT} = 0.7V (ISL9123B), I^2C pull-up voltage = 3.6V, L_1 = 1µH, C_1 = 10µF, C_2 = C_{OUT}(effective) = 6µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range (-40°C to +85°C) and input voltage range (1.8V to 5.5V), unless specified otherwise.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
ISL9123BII7Z		V_{IN} = 3.6V, V_{OUT} = 0.7V, I_{OUT} = 0A, forced PWM	-14	-	14	mV
		V_{IN} = 3.6V, V_{OUT} = 0.7V, I_{OUT} = 1mA, PFM	-20	-	20	mV
ISL9123BII9Z		V_{IN} = 3.6V, V_{OUT} = 0.88V, I_{OUT} = 0A, forced PWM	-17.6	-	17.6	mV
		V_{IN} = 3.6V, V_{OUT} = 0.88V, I_{OUT} = 1mA, PFM	-17.6	-	17.6	mV
Soft-Start and Soft Discharge						
Time to Read OTP	t_{OTP}	Time from when V_{IN} > V_{UVLO} and EN signal asserts until switching starts	-	125	-	µs
V_{OUT} Ramp Rate for Soft-Start and During Dynamic Voltage Scaling (applicable only for V_{OUT} ramp-up, not ramp-down) (ISL9123/A)	DVSRATE	Default at POR	-	3.125	-	mV/µs
		Programmable using I^2C after POR	-	6.25 0.78125 1.5625	-	mV/µs
V_{OUT} Ramp Rate for Soft-Start and During Dynamic Voltage Scaling (applicable only for V_{OUT} ramp-up, not ramp-down) (ISL9123B)		Default at POR	-	1.25	-	mV/µs
		Programmable using I^2C after POR	-	0.625 0.15625 0.3125	-	mV/µs
V_{OUT} Soft Discharge ON-Resistance (ISL9123 only)	r_{DISCHG}	V_{EN} pulled to GND	-	125	-	Ω
V_{OUT} Soft Discharge ON-Resistance (ISL9123B only)		V_{EN} pulled to GND	-	1.15	-	MΩ
Power MOSFET						
P-Channel MOSFET ON-Resistance	r_{DSON_P}	V_{IN} = 3.6V, V_{OUT} = 3.6V (ISL9123/A only) V_{IN} = 3.6V, V_{OUT} = 0.8V (ISL9123B only)	**50**	95	**140**	mΩ
N-Channel MOSFET ON-Resistance	r_{DSON_N}		**50**	100	**140**	mΩ
Auxiliary Switched Output MOSFET ON-Resistance	r_{DSON_VAUX}	V_{IN} = 3.6V, V_{OUT} = 3.6V (ISL9123/A only)	-	55	**70**	mΩ
Bypass Mode						
Auto Bypass Thresholds (ISL9123/A only)	V_{IN_BYP}	Auto bypass exit threshold - V_{IN} offset above regulated output voltage V_{OUT}. I_{OUT} = 10mA	-	30	-	mV
		Auto bypass entry threshold - V_{IN} offset above regulated output voltage V_{OUT}. I_{OUT} = 10mA	-	20	-	mV
Inductor Peak Current Limit						
Peak Current Limit	I_{LIM}	2.5V < V_{IN} < 5.5V	-	1.4	-	A
		1.8V < V_{IN} < 2.5V	-	1.4*(V_{IN}/2.5)	-	A

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 1.8V (ISL9123/A), V_{OUT} = 0.7V (ISL9123B), I^2C pull-up voltage = 3.6V, L_1 = 1µH, C_1 = 10µF, C_2 = C_{OUT}(effective) = 6µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range (-40°C to +85°C) and input voltage range (1.8V to 5.5V), unless specified otherwise.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Efficiency						
Efficiency (ISL9123/A)	η	I_{OUT} = 50mA, V_{IN} = 3.7V, V_{OUT} = 3.3V	-	96	-	%
		I_{OUT} = 10µA, V_{IN} = 3.7V, V_{OUT} = 3.3V	-	86	-	
		I_{OUT} = 50mA, V_{IN} = 3.6V, V_{OUT} = 1.8V	-	91	-	
		I_{OUT} = 10µA, V_{IN} = 3.6V, V_{OUT} = 1.8V	-	78	-	
Efficiency (ISL9123B)		I_{OUT} = 50mA, V_{IN} = 3.6V, V_{OUT} = 0.7V	-	80	-	%
		I_{OUT} = 10µA, V_{IN} = 3.6V, V_{OUT} = 0.7V	-	50	-	
Switching Frequency						
Switching Frequency (ISL9123/A)	f_{SW}	I_{OUT} = 1mA, Forced PWM	-	2.5	-	MHz
Switching Frequency (ISL9123B)	-	I_{OUT} = 1mA, Forced PWM, V_{OUT} = 0.8V	-	1.75	-	MHz
Hiccup Mode						
Hiccup Time	t_{FLT_WAIT}	Time from OCP shutdown to restart	-	100	-	ms
Thermal Protection						
Thermal Shutdown Threshold	T_{SD}	Rising temperature	-	140	-	°C
Thermal Shutdown Hysteresis	T_{SD_HYS}	-	-	25	-	°C
Logic Levels						
Input Leakage	I_{LEAK}	EN pin	-	9	**300**	nA
		SCL pin	-	8	**300**	nA
		SDA pin	-	8	**300**	nA
EN Input HIGH Voltage	EN_{IH}	V_{IN} = 3.6V	**1.6**	-	-	V
EN Input LOW Voltage	EN_{IL}		-	-	**0.36**	V
SCL/SDA Input HIGH Voltage	SCL/SDA_{IH}		**1.45**	-	-	V
SCL/SDA Input LOW Voltage	SCL/SDA_{IL}		-	-	**0.36**	V

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits are established by characterization and are not production tested.
2. Quiescent current measurements are taken when the device is not switching.
3. Minimum load of 300nA is needed to maintain V_{OUT}, for VSET less than 1.1V.

3.5 I²C Interface Timing Specifications

Applicable to SCL and SDA in the Fast mode I²C operation, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
I²C Frequency Capability	f_{I2C}	-	0	-	400	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{SP}	Any pulse narrower than the maximum specification is suppressed	-	-	50	ns
Data Valid Time	$t_{VD:DAT}$	Time from SCL falling edge crossing SCL_{IL} to SDA exiting the SDA_{IL} to SDA_{IH} window	-	-	900	ns
Data Valid Acknowledge Time	$t_{VD:ACK}$	Time from SCL falling edge crossing SCL_{IL} to SDA exiting the SDA_{IL} to SDA_{IH} window, during acknowledgment	-	-	900	ns
Bus Free Time Between a STOP and START Condition	t_{BUF}	Time from SDA crossing SDA_{IH} at STOP to SDA crossing SDA_{IH} at the following START	1300	-	-	ns
SCL Low Time	t_{LOW}	Measured at the SCL_{IL} crossing	1300	-	-	ns
SCL High Time	t_{HIGH}	Measured at the SCL_{IH} crossing	600	-	-	ns
START Condition Setup Time	$t_{SU:STA}$	Time from SCL rising edge crossing SCL_{IH} to SDA falling edge crossing SDA_{IH}	600	-	-	ns
START Condition Hold Time	$t_{HD:STA}$	Time from SDA falling edge crossing SDA_{IL} to SCL falling edge crossing SCL_{IH}	600	-	-	ns
Data Set-Up Time	$t_{SU:DAT}$	Time from SDA exiting the SDA_{IL} to SDA_{IH} window to SCL rising edge crossing SCL_{IL}	100	-	-	ns
Data Hold Time	$t_{HD:DAT}$	Time from SCL falling edge crossing SCL_{IL} to SDA entering the SDA_{IL} to SDA_{IH} window	50	-	-	ns
STOP Condition Set-Up Time	$t_{SU:STO}$	Time from SCL rising edge crossing SCL_{IH} to SDA rising edge crossing SDA_{IL}	600	-	-	ns
SCL/SDA Capacitive Loading	C_b	Capacitive load for each bus line	-	-	400	pF

1. Limits established by design and are not production tested.

4. Typical Performance Curves

4.1 ISL9123/A

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 1.8V, I^2C pull-up voltage = 3.6V, L_1 = 1µH, C_1 = C_{OUT} = 10µF/0603, C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated.

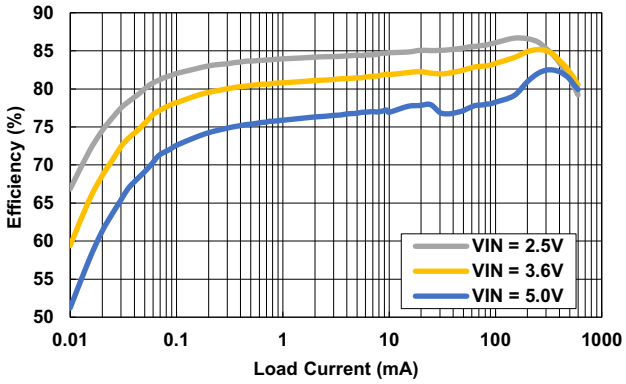


Figure 5. Efficiency vs Load Current: V_{OUT} = 0.8V

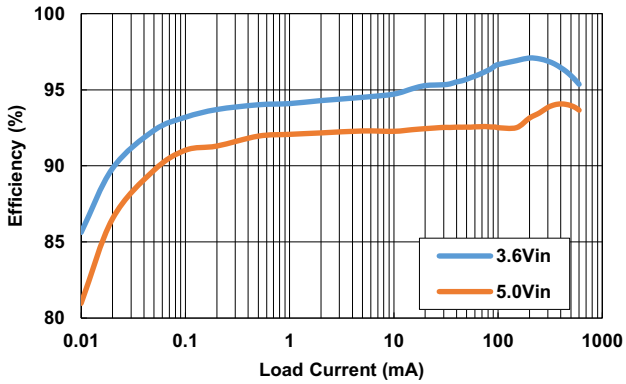


Figure 6. Efficiency vs Load Current: V_{OUT} = 3.3V

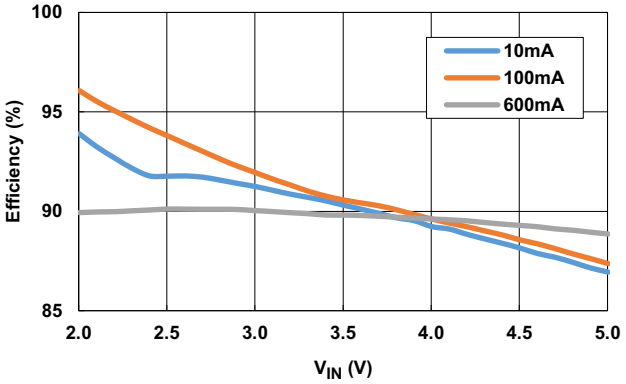


Figure 7. Efficiency vs Input Voltage: V_{OUT} = 1.8V

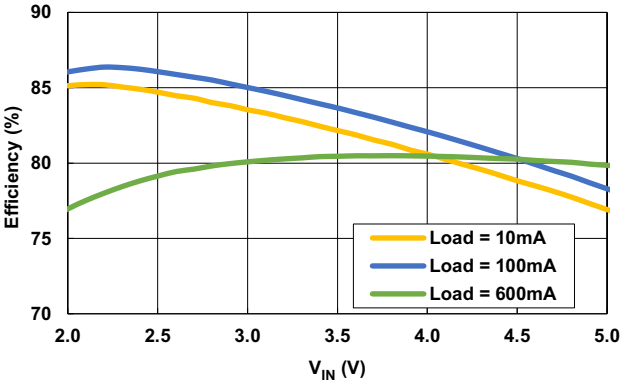


Figure 8. Efficiency vs Input Voltage: V_{OUT} = 0.8V

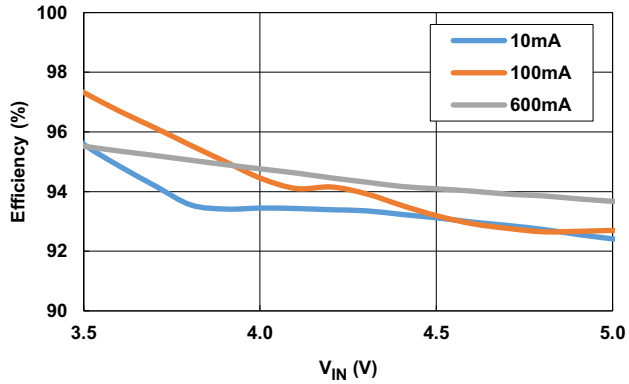


Figure 9. Efficiency vs Input Voltage: V_{OUT} = 3.3V

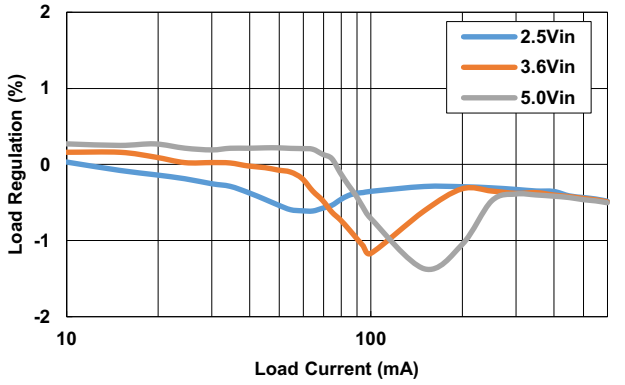


Figure 10. Output Voltage Accuracy vs Load Current: V_{OUT} = 1.8V

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 1.8V, I^2C pull-up voltage = 3.6V, L_1 = 1µH, C_1 = C_{OUT} = 10µF/0603, C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated. (Cont.)

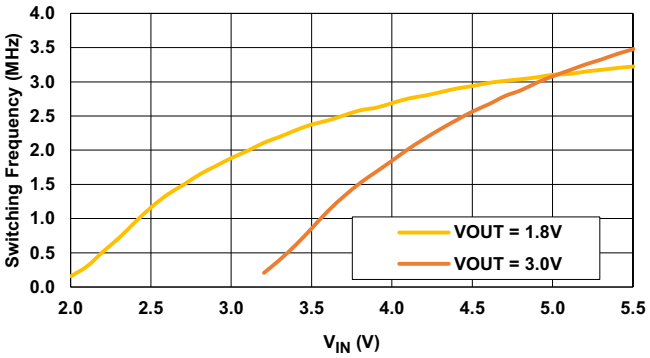


Figure 11. Switching Frequency vs Input Voltage: I_{OUT} = 600mA

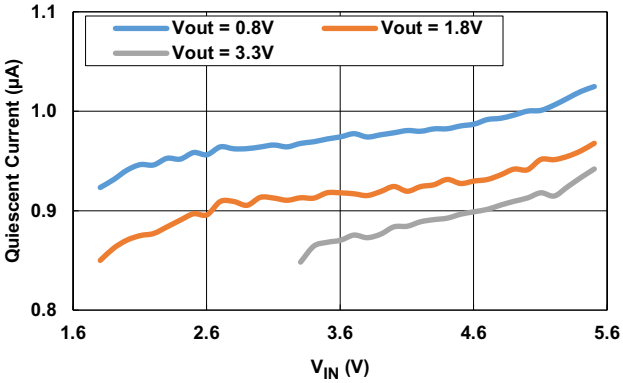


Figure 12. Quiescent Current vs Input Voltage

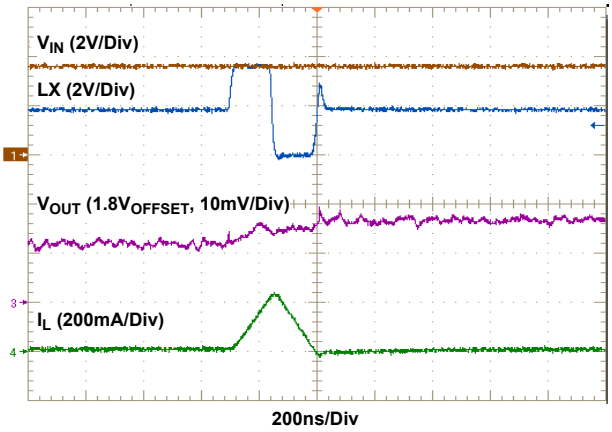


Figure 13. Steady-State Operation in PFM: V_{IN} = 3.6V, V_{OUT} = 1.8V, No Load

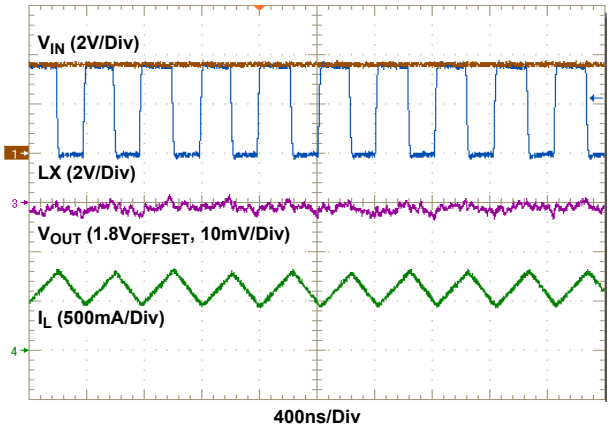


Figure 14. Steady-State Operation in PWM: V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 600mA

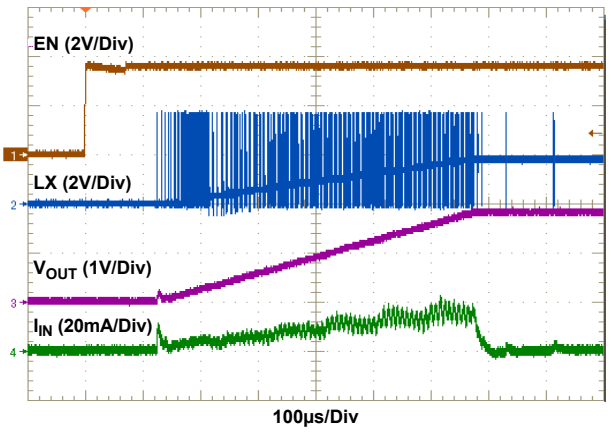


Figure 15. Soft-Start: V_{IN} = 3.6V, V_{SET} = 1.8V, No Load

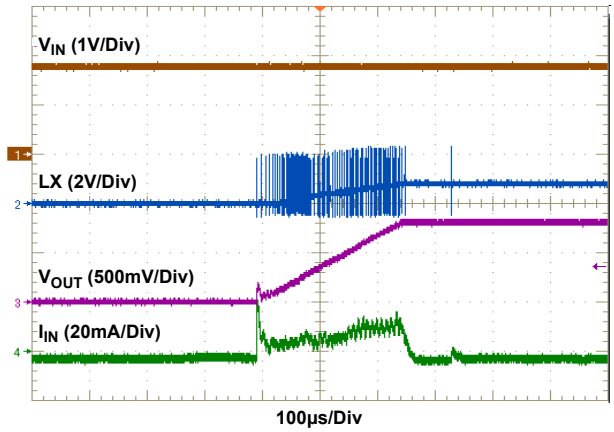


Figure 16. Soft-Start: V_{IN} = 1.8V, V_{SET} = 0.8V, No Load

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 1.8V, I^2C pull-up voltage = 3.6V, L_1 = 1µH, C_1 = C_{OUT} = 10µF/0603, C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated. (Cont.)

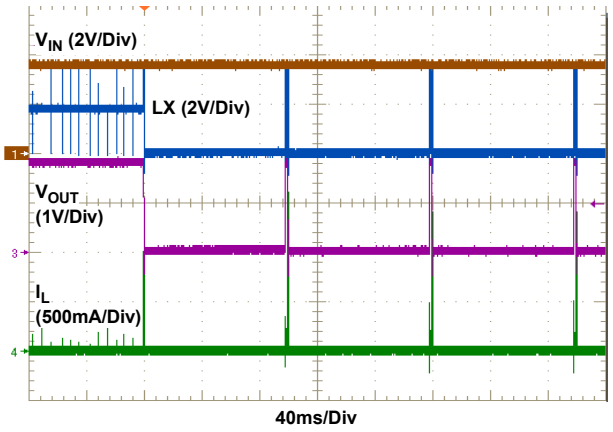


Figure 17. Output Short-Circuit Behavior (Hiccup Mode)

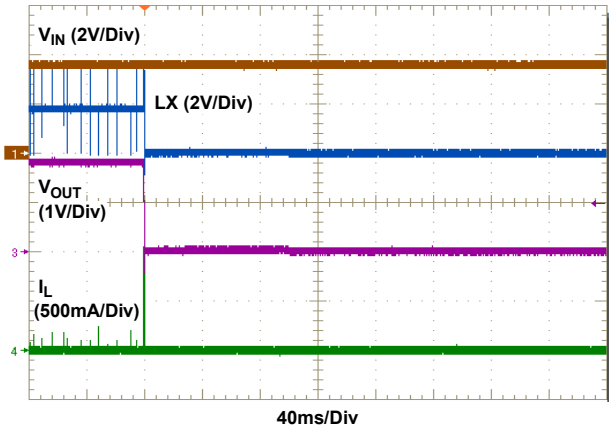


Figure 18. Output Short-Circuit Behavior (Shutdown Mode)

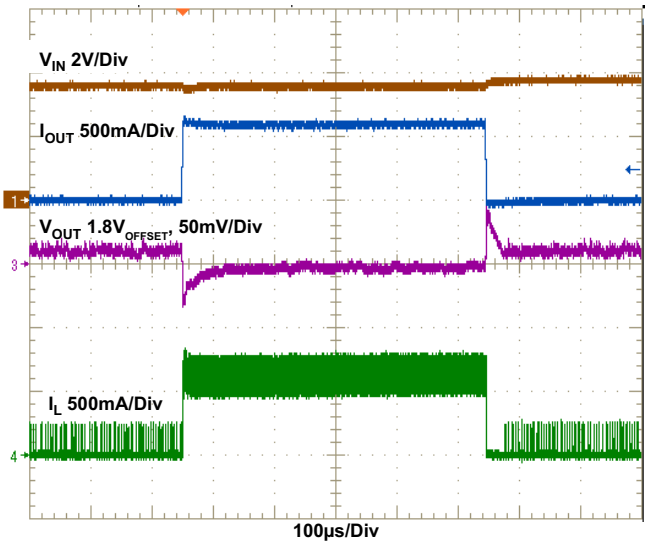


Figure 19. Load Transient: V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 0.01A to 0.60A, Slew Rate = 1A/µs, Type II Error Amplifier

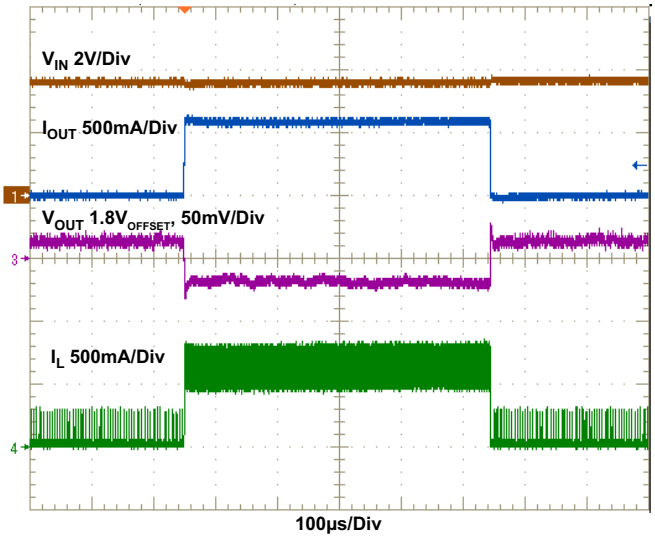


Figure 20. Load Transient: V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 0.01A to 0.60A, Slew Rate = 1A/µs, Type I Error Amplifier

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 1.8V, I^2C pull-up voltage = 3.6V, L_1 = 1µH, C_1 = C_{OUT} = 10µF/0603, C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated. (Cont.)

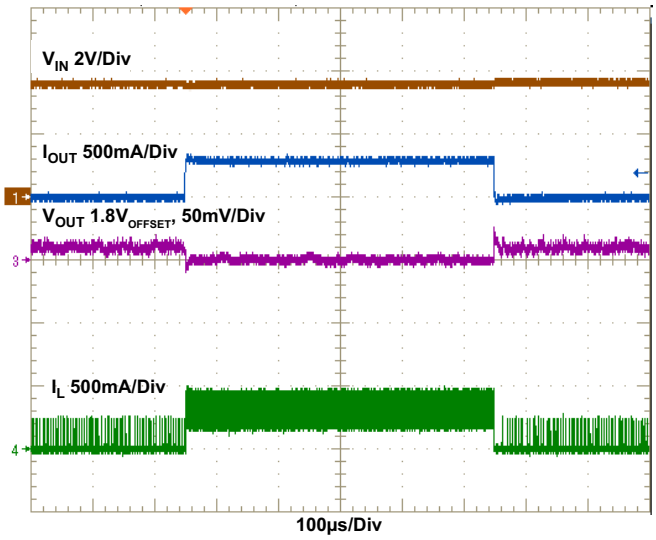


Figure 21. Load Transient: V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 0.01A to 0.30A, Slew Rate = 1A/µs, Type II Error Amplifier

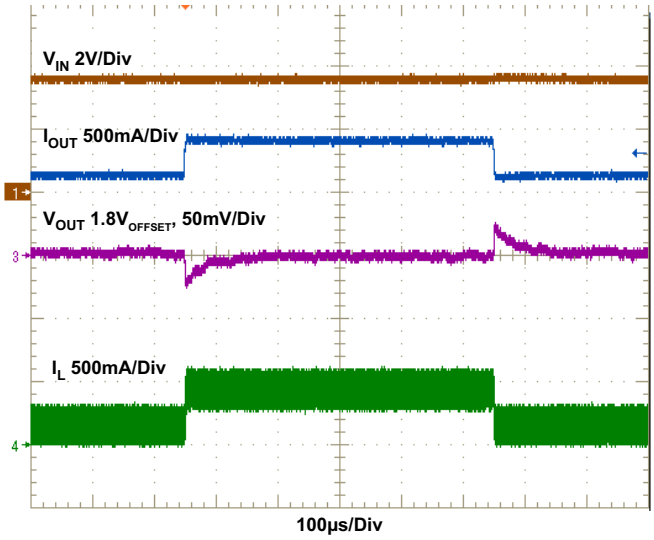


Figure 22. Load Transient: V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 0.15A to 0.45A, Slew Rate = 1A/µs, Type II Error Amplifier

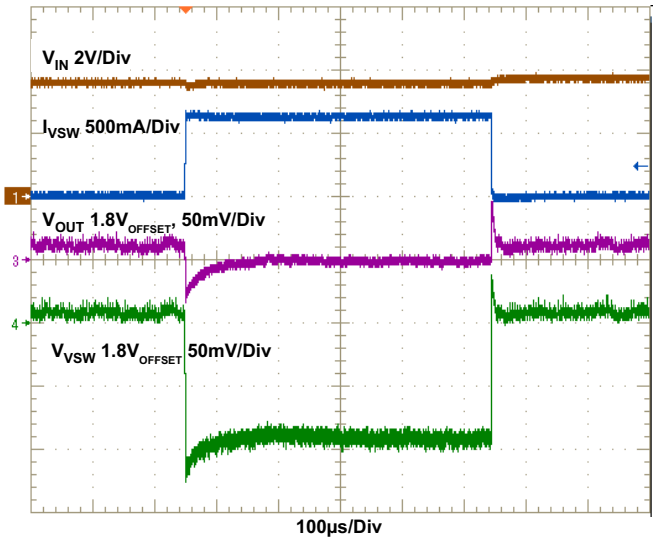


Figure 23. Load Transient: V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} at VSW = 0.01A to 0.60A, Slew Rate = 1A/µs, Type II Error Amplifier

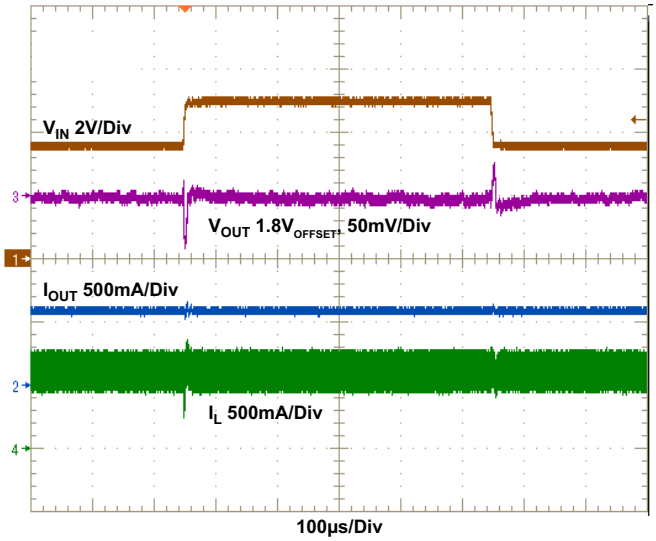


Figure 24. Line Transient: V_{IN} = 3.6V to 5.0V, Slew Rate = 0.5V/µs, V_{OUT} = 1.8V, I_{OUT} = 600mA, Type II Error Amplifier

4.2 ISL9123B

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 0.88V, I^2C pull-up voltage = 3.6V, L_1 = 1µH, C_1 = C_{IN} = 10µF/0603, C_2 = C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated.

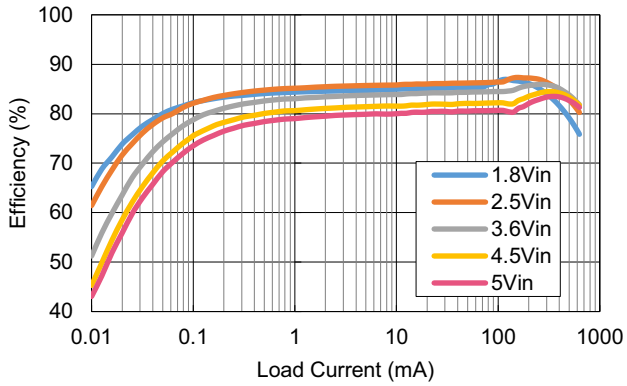


Figure 25. Efficiency vs Load Current

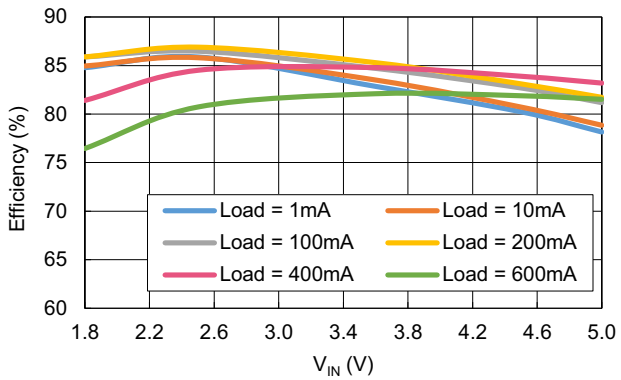


Figure 26. Efficiency vs Input Voltage

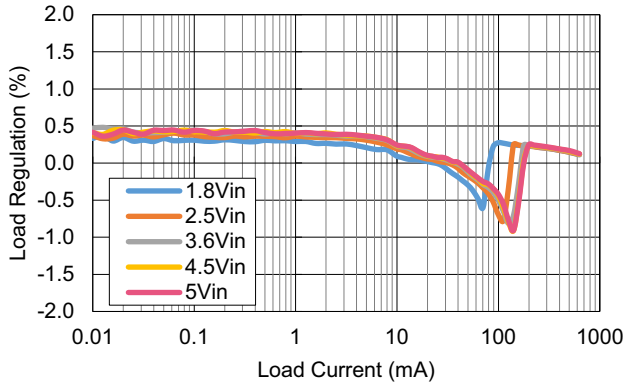


Figure 27. Output Voltage Accuracy vs Load Current

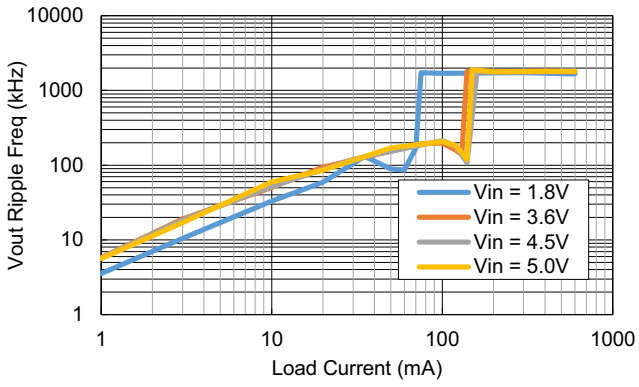


Figure 28. V_{OUT} Ripple Frequency vs. Load Current Auto PFM/PWM Mode

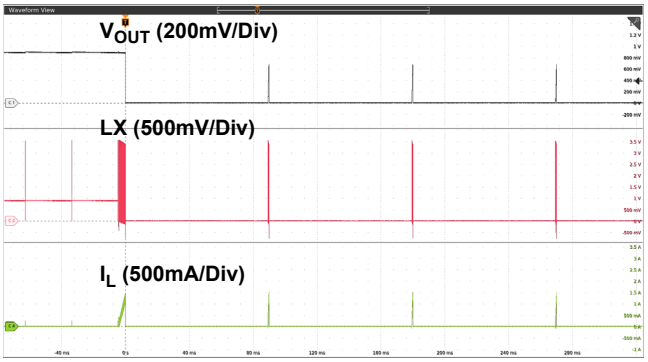


Figure 29. Output Short-Circuit Behavior (Hiccup Mode)

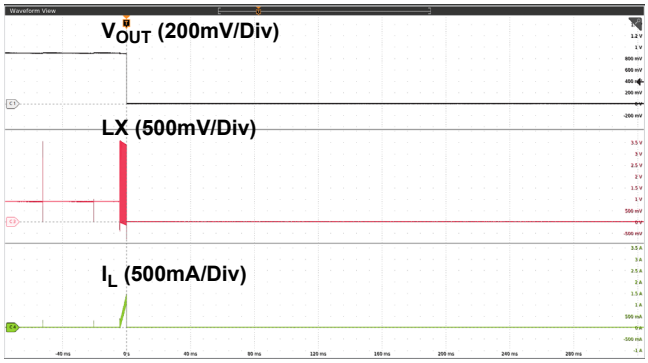


Figure 30. Output Short-Circuit Behavior (Shutdown Mode)

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 0.88V, I^2C pull-up voltage = 3.6V, L_1 = 1µH, C_1 = C_{IN} = 10µF/0603, C_2 = C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated. (Cont.)

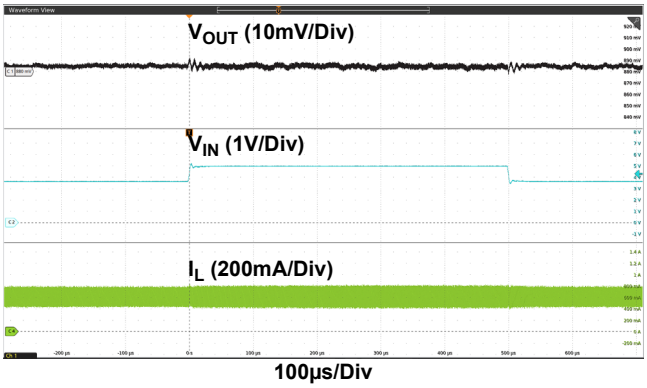


Figure 31. Line Transient: V_{IN} = 3.6V to 5.0V, Slew Rate = 0.5V/µs, Load = 600mA, Type-II Error Amplifier

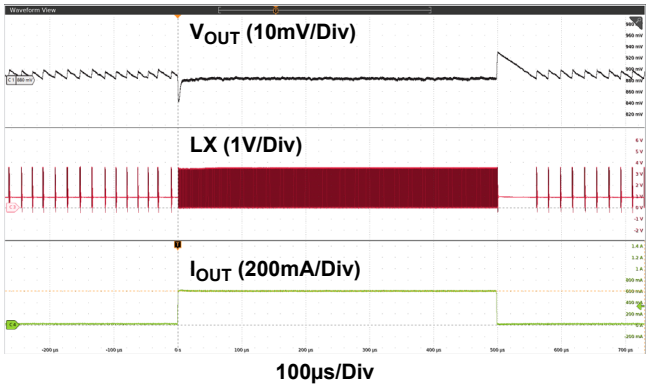


Figure 32. Load Transient: Load = 0.01A to 0.60A, Slew Rate = 1A/µs, Type-II Error Amplifier

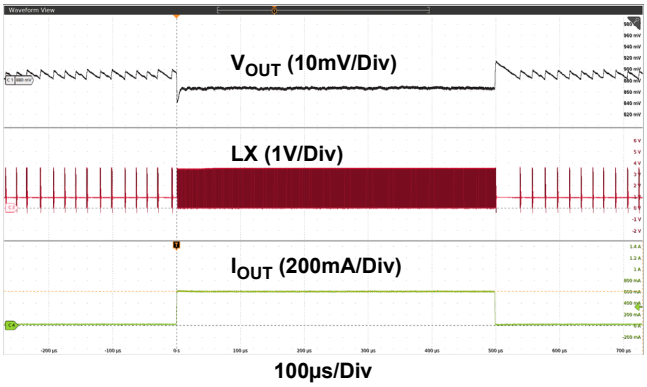


Figure 33. Load Transient Load = 0.01A to 0.60A, Slew Rate = 1A/µs, Type-I Error Amplifier

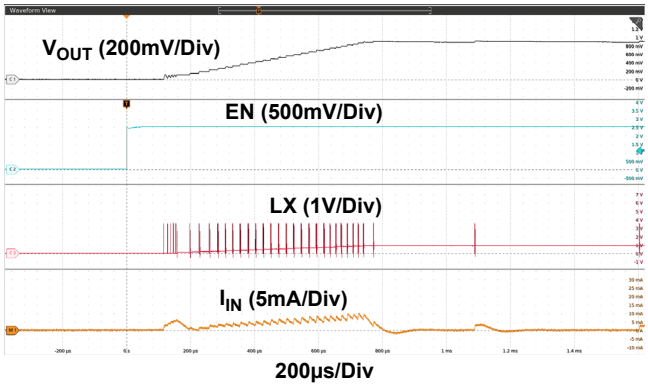


Figure 34. Soft-Start, No Load

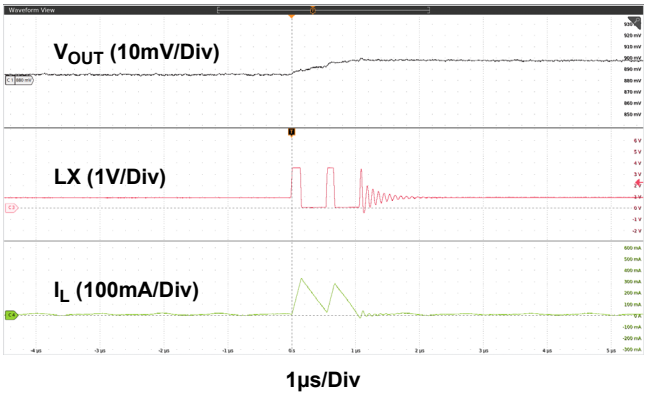


Figure 35. Steady-State Operation, No Load

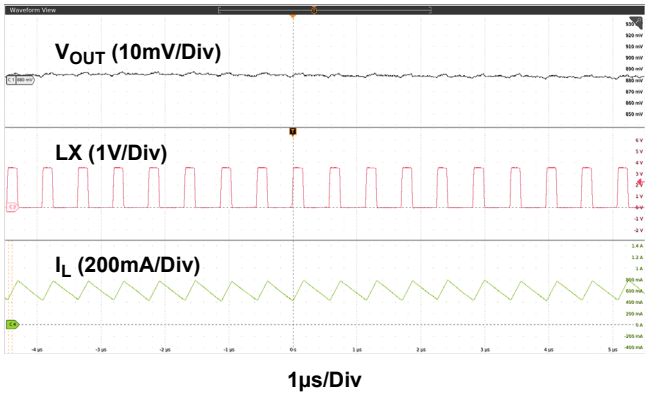


Figure 36. Steady-State Operation, Load = 600mA

5. Functional Description

The ISL9123/A and ISL9123B implement a complete buck switching regulator, with PWM controller, internal switches, references, protection circuitry, and control inputs. For more information see the Block Diagrams.

5.1 Enable Input

The device is enabled by asserting EN pin HIGH. Driving EN LOW invokes Power-Down mode, in which most internal device functions are disabled. EN must remain LOW for at least 50µs for the device to be disabled. When the device is disabled by driving EN low, while V_{IN} is valid, the output discharges differently in ISL9123 than in ISL9123A or ISL9123B, due to the ISL9123 internal Soft Discharge (ISL9123/B only) resistor.

5.2 Soft Discharge (ISL9123/B only)

Whenever the converter is disabled over I^2C, an internal discharge resistor between VOUT and GND can be activated to slowly discharge the output capacitor. This internal discharge resistor has a typical resistance of 125Ω for ISL9123, and 1.15MΩ for ISL9123B. The soft discharge function is accessed using I^2C while keeping the EN pin HIGH. Using the CONV_CFG register, set DISCH bit to 1 and disable the IC by setting EN_AND bit to 0 (see Table 5 for details).

5.3 Startup

When the input voltage rises above the undervoltage lockout threshold and EN is asserted HIGH, the power-on sequence starts. First, the IC is initialized and its One-Time Programmable (OTP) memory is read. After the OTP has been read and the controller knows the target output voltage and ramp rate, soft-start begins and the output voltage rises at the programmed dynamic voltage scaling (DVS) ramp rate until it reaches the target output voltage.

5.4 Overcurrent/Short-Circuit Protection

The ISL9123/A and ISL9123B provide overcurrent protection by monitoring the inductor current. When the peak inductor current hits its current limit, the IC enters Hiccup mode, Shutdown mode, or Current Limit mode according to the setting of the OC_FAULT_MODE bits in the INT_FLAG_MASK register.

During Hiccup mode, the IC shuts down for 100ms and then tries to restart. If it encounters the overcurrent condition again, it shuts down and tries to restart after another 100ms. This cycle keeps repeating until there is no overcurrent and VOUT can then come back up.

In Shutdown mode, the IC shuts down whenever overcurrent is encountered and the only way to bring the output voltage up is to restart the part by either cycling VIN, or EN, or by resetting and then setting the EN_AND bit in the CONV_CFG register, to mimic EN cycling behavior.

In Current Limit mode, the IC provides the maximum current it can, while respecting the peak current limit. If the load demand is even more, the IC starts dropping the output voltage while supplying the same maximum current.

5.5 Thermal Shutdown

The ISL9123/A feature thermal shutdown that protects the device from damage due to overheating. An integrated temperature sensor circuit monitors the internal IC temperature. When the temperature exceeds T_{SD}, the device stops switching and waits for the temperature to fall. When the temperature falls by T_{SDHYS}, the controller first goes through the soft-start phase and then starts regulating at the target output voltage as defined by the I^2C register value.

5.6 Buck Conversion Topology

The ISL9123/A operate in either Bypass or Buck mode. ISL9123B does not support Bypass mode. When operating in conditions in which V_{IN} is close to V_{OUT}, the device automatically switches from Buck mode to Bypass mode. For other conditions, the device performs Buck regulation.

Figure 37 shows a simplified diagram of the internal switches and external inductor. In ISL9123/A only, Switch D provides an auxiliary switched output connection, see Auxiliary Output (ISL9123/A only). In ISL9123B, Switch D is deleted and VSW is internally shorted to VOUT.

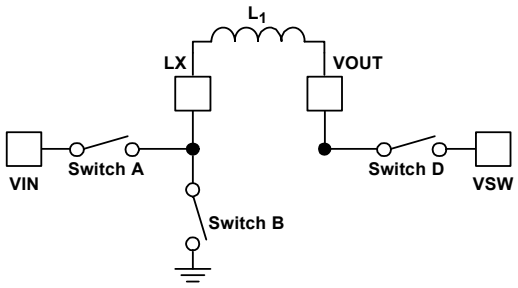


Figure 37. Buck Topology

5.7 Pulse Width Modulation (PWM) Operation

In Buck PWM mode, Switches A and B operate as in a synchronous buck converter. Initially Switch A is turned ON and this ramps up the inductor current with a slope of $(V_{IN} - V_{OUT})/L$ (in buck mode, $V_{IN} > V_{OUT}$). Once inductor current hits the upper threshold, as dictated by the hysteretic controller, Switch A is turned OFF. This is followed by a small dead-time where both the switches are OFF. During this interval, the inductor current keeps flowing, finding its path through the body diode of Switch B. When the dead-time is over, Switch B is turned ON and the inductor current ramps down with a slope of $-(V_{OUT})/L$. When it hits the lower hysteretic threshold, Switch B is turned OFF, followed by another dead-time interval. After this, Switch A is turned ON again and the entire sequence repeats.

The converter operates in PWM mode under two conditions: load is sufficiently high in the Normal Mode (Auto PFM/PWM mode) OR Forced PWM mode is enabled by setting the FMODE bits in CONV_CFG register to 0x2.

The optimal switching frequency is determined by the hysteretic controller and is centered around 2.5MHz (for ISL9123/A) for V_{IN} = 3.6V and V_{OUT} = 1.8V, and 1.75MHz (for ISL9123B) for V_{IN} = 3.6V and V_{OUT} = 0.8V.

5.8 Pulse Frequency Modulation (PFM) Operation

During PFM operation in Buck mode, Switches A and B operate in Discontinuous Conduction Mode (DCM). Just like the Buck PWM operation, Switch A is turned ON followed by a dead-time and then Switch B is turned ON. The inductor current ramps up and down respectively, and the energy contained in this current pulse charges up V_{OUT}. After this, unlike the PWM operation, both switches remain OFF until V_{OUT} discharges down to the lower threshold of the hysteretic controller. The switching cycle repeats after that.

In some operating conditions, multiple switching pulses are needed to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the upper threshold of the PFM hysteretic controller. Switching then stops and remains stopped until V_{OUT} decays to the lower threshold. As load increases, the frequency of PFM pulses increases as V_{OUT} gets discharged faster and needs to be recharged more often. This continues until the PFM pulses start bunching together and the part then enters sustained PWM operation. The converter operates in PFM mode under only one condition: load is light enough in the Normal Mode (Auto PFM/PWM mode).

The PFM-PWM transition, going from light to heavy load and then back to light load, has a hysteretic band. This allows for a seamless PFM to PWM and PWM to PFM transition.

5.9 Operation with V_{IN} Close to V_{OUT} (ISL9123/A only)

When the output voltage is close to the input voltage, the ISL9123/A rapidly and smoothly switches between Buck mode and Bypass mode as needed to maintain the regulated output voltage. This behavior provides excellent efficiency and very low output voltage ripple.

5.10 Forced Operating Modes (ISL9123/A only)

Forced operating modes include Forced PWM mode and Forced Bypass mode. Forced operating modes are selected using the FMODE bits in the CONV_CFG register (see Table 5 for details). The power-up default mode is Normal operation with automatic mode transitions to optimize efficiency. If V_{IN} approaches V_{OUT}, switching instances reduce and smoothly transition from Switching to Bypass mode.

Forced PWM mode can be selected to minimize the switching frequency variation and to obtain a tight V_{OUT} accuracy, although this comes at the expense of increased input current. Forced Bypass mode can be selected to minimize power losses when output voltage regulation is not required. When the device enters Bypass mode, Switch A is turned ON, providing a direct path from the input to output through the inductor. In Bypass mode, all other blocks, except POR and I^2C, are turned off to minimize quiescent current consumption. If the part has to repeatedly bounce between the Forced Bypass and Regulation modes, there should be at least 1ms delay between the successive mode setting I^2C commands. *Note:* There is no overcurrent protection in Bypass mode.

5.11 Auxiliary Output (ISL9123/A only)

The ISL9123/A offer an auxiliary output (VSW). VSW can be connected to VOUT by the internal Switch D (Figure 37), which is enabled/disabled by the AUX_SW register bit. VSW is actively controlled when $V_{IN} > V_{UVLO}$, and below V_{UVLO} VSW is disconnected and floating. VSW supports the specified load capability of the buck regulator. Local decoupling at VSW is not required, and should not be used.

It is acceptable to enable/disable the auxiliary output on-the-fly. However, when enabling into a load, inrush and transient effects can be managed by using the buck soft-start mechanism. Use the following steps to enable VSW:

1. Disable the buck converter through I^2C: using EN_AND bit
2. Allow the output (V_{OUT}) to discharge
3. Enable VSW pin connection through I^2C: using AUX_SW bit
4. Enable the buck converter through I^2C: using EN_AND bit

If VSW is unused in the application, it should be floated irrespective of the AUX_SW bit setting.

5.12 I^2C Serial Interface

The ISL9123 family supports a bidirectional bus-oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the device operates as a slave device in all applications.

The IC supports the following data transfer rates and modes as defined in the I^2C specification:

- Up to 100kbit/s in Standard mode
- Up to 400kbit/s in Fast mode

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

The I^2C pull-up voltage may be from 1.8V to 5.5V. However, input quiescent current increases by up to 1µA (typ), 3µA (max), if the I^2C pull-up voltage is less than V_{IN}. There is no increase in the quiescent current if the I^2C pins are pulled down to ground.

5.12.1 Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 38). At power-up the SDA pin is in input mode.

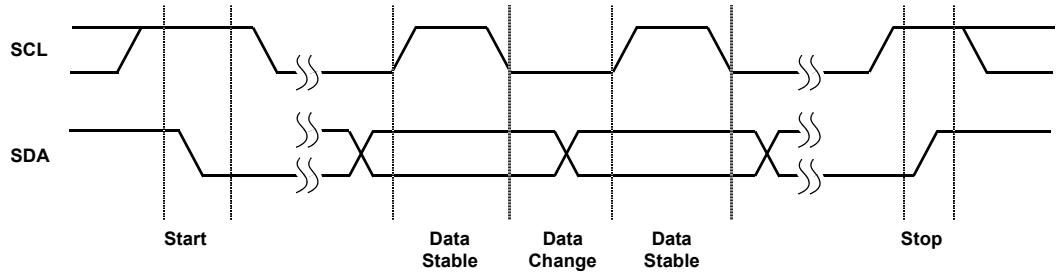


Figure 38. Valid Data Changes, Start, and Stop Conditions

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 38). A START condition is ignored during the power-up sequence and when the EN input is low.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 38).

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 39), and the data is latched in and responded to by the device.

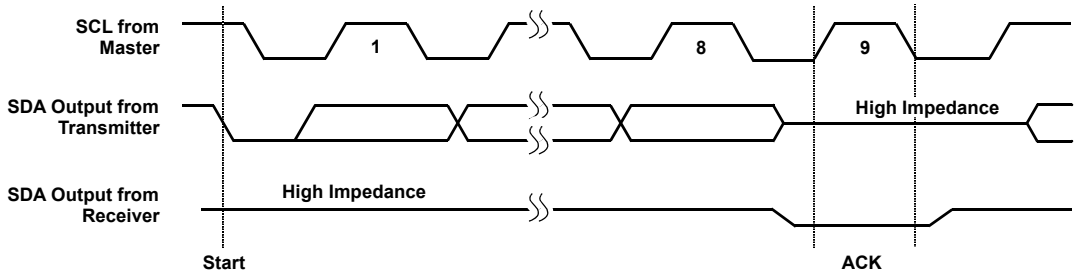


Figure 39. Acknowledge Response from Receiver

The device responds with an ACK after recognizing a START condition followed by a valid 7-bit slave address, and once again after successful receipt of a register address byte. The device again responds with an ACK after receiving a data byte of a write operation. The master must respond with an ACK after receiving a data byte of a read operation.

For the base version of ISL9123, the 7-bit slave address is set in trim to 0x1C. For the base version of ISL9123A, the 7-bit slave address is set in trim to 0x1D. For the base version of ISL9123B, the 7-bit slave address is set in trim to 0x1E. The 7-bit address is followed by a Read/$\overline{\text{Write}}$ bit whose value is 1 for a Read operation, and 0 for a Write operation (see Table 1).

Table 1. 7-Bit Address Format

ISL9123	0	0	1	1	1	0	0	R/$\overline{\text{W}}$
ISL9123A	0	0	1	1	1	0	1	R/$\overline{\text{W}}$
ISL9123B	0	0	1	1	1	1	0	R/$\overline{\text{W}}$
	(MSB)							(LSB)

5.12.2 Write Operation

Write operations are shown in Figure 40. A write operation requires a START condition, followed by a valid 7-bit slave address with the R/$\overline{W}$ bit set to 0, a valid register address byte, one or more data bytes, and a STOP condition. After each of the bytes, the device responds with an ACK. After each data byte is acknowledged, the device increments its register address to support block writes. The master sends a STOP to complete the command.

STOP conditions that terminate write operations must be sent by the master after sending at least one full data byte and its associated ACK signal. If a STOP condition is issued in the middle of a data byte, or before one full data byte + ACK is sent, the device ignores the command, and does not change the output voltage or other settings.

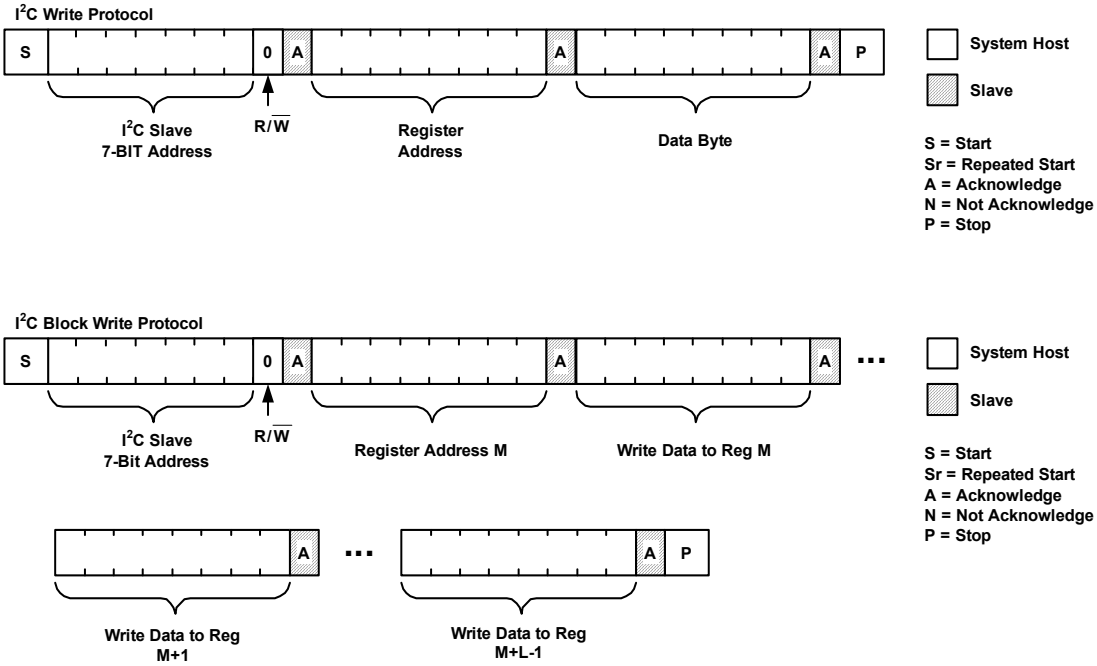


Figure 40. I²C Register Write Protocols

5.12.3 Read Operation

Read operations are shown in Figure 41. They consist of four or more bytes. The host generates a START condition, then transmits the 7-bit slave address with the R/$\overline{W}$ bit set to 0. The device responds with an ACK. The host then transmits the register address byte, and the device responds with another ACK.

The host then generates a repeat START condition and transmits the 7-bit slave address with the R/$\overline{W}$ bit set to 1. The device responds with an ACK, indicating it is ready to provide the requested data.

The device then transmits the data byte by asserting control of the SDA pin while the host generates clock pulses on the SCL pin. After each data byte is complete, the host generates an ACK condition. After every successfully transmitted data byte, the device automatically increments its internal register address to support block reads. The host terminates the Read operation by issuing a NACK and sending a STOP condition.

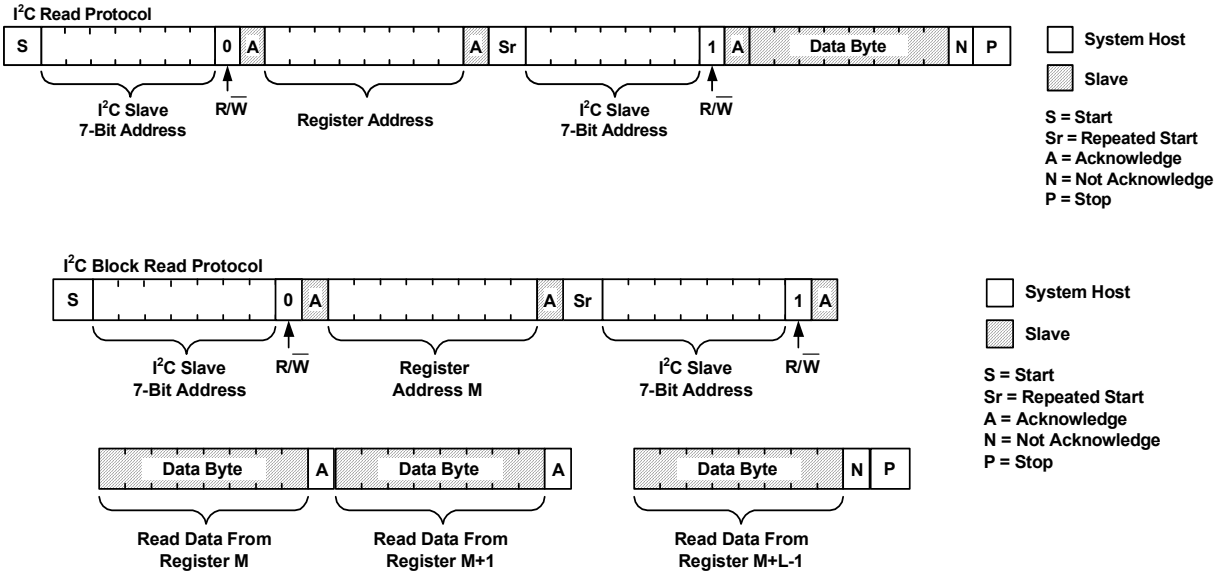


Figure 41. I²C Register Read Protocols

6. Register Descriptions

The ISL9123 family devices have five I²C accessible control registers whose functions are described in Table 2 through Table 6. These registers can be accessed any time the device is enabled. When the device is disabled (EN = LOW), or loading OTP, attempts to communicate through its I²C interface are not supported.

6.1 RO_REG1

The RO_REG1 register contains the hardware identification bits as described in Table 2.

Table 2. Register Address 0x02: RO_REG1

Bit	Name	Type	Reset	Description
7:6	FAMILY_ID[1:0]	R	0x0	Chip family identifier 0x0 = ISL9122 stand-alone converter family
5:3	HW_REV[2:0]	R	0x3	(ISL9123 only): Chip revision level 0x3 = Hardware revision D
			0x4	(ISL9123A only): Chip revision level 0x4 = Hardware revision E
			0x6	(ISL9123B only): Chip revision level 0x6 = Hardware revision G
2:0	RAIL_VAR[2:0]	R	0x4	Converter variant identifier 0x4 = Buck

6.2 INTFLG_REG

The INTFLG_REG register contains fault flags. Each bit represents a different type of fault as described in Table 3. A 0 indicates no fault, and a 1 indicates a fault. Each bit is set by a fault event and is cleared when read. When a fault flag is read back and asserted (1), it indicates a fault occurred in the past. Read the flag again to examine the current IC status – occurring in the time between the first and second I^2C read. Continuing to poll the flags provides period updates of the IC status relative to the previous read-back.

Table 3. Register Address 0x03: INTFLG_REG

Bit	Name	Type	Reset	Description
3	INT3	R	0x0	Voltage setting under range. Sets to '1' when VSET changes from within the 0x04-0xD7 range to below 0x4.
2	INT2	R	0x0	Voltage setting over range. Sets to '1' when VSET changes from within the 0x04-0xD7 range to above 0xD7.
1	INT1	R	0x0	Over-temperature
0	INT0	R	0x0	Overcurrent

6.3 VSET

The ISL9123/A VSET register contains the output voltage setting in 25mV steps as shown in Equation 1.

(EQ. 1) $V_{OUT} = VSET \times 0.025V$

The ISL9123B VSET register contains the output voltage setting in 5mV steps as shown in Equation 2.

(EQ. 2) $V_{OUT} = VSET \times 0.005V$

VSET can be changed after the IC is enabled and operating. When the output voltage is changed, it ramps at the rate set in the DVSRATE bits of CONV_CFG register.

The output voltage range is digitally limited to be between the minimum and maximum values shown in Table 4. Setting values above or below the limits results in the output voltage ramping to the limit and the appropriate overvoltage or undervoltage interrupt flag in INTFLG_REG being set. The limits prescribed in Recommended Operating Conditions should be followed while setting the output voltage.

Table 4. Register Address 0x11: VSET

Bit	Name	Type	Reset[1]	Description
7:0	VSET[7:0]	R/W	-	(ISL9123/A only): Output voltage setting (25mV steps): Minimum limit = 0.1V (0x04). *Note:* the specified operating minimum is 0.4V (0x10). Maximum limit = 5.375V (0xD7)
				(ISL9123B only): Output voltage setting (5mV steps): Minimum limit = 0.02V (0x04). *Note*: the specified operating minimum is 0.4V (0x50). Maximum limit = 1.180V (0xEC)

1. For part specific default output voltage, see the Ordering Information table.

6.4 CONV_CFG

The CONV_CFG register settings are described in Table 5.

Table 5. Register Address 0x12: CONV_CFG

Bit	Name	Type	Reset	Description
7	EN_AND	R/W	0x1	Enable bit. ANDed with the enable input 0x0 = EN pin going high wakes up the I^2C, but does not start the converter. The converter is started by writing 1 to this bit using I^2C while the EN pin is high 0x1 = EN pin going high wakes up the I^2C and starts the converter *Note:* EN pin low always disables the converter and I^2C
6	DISCH	R/W	0x0	(ISL9123/B only): 0x0 = No discharge resistor present when converter is disabled over I^2C 0x1 = Discharge resistor present when converter is disabled over I^2C
	Reserved			(ISL9123A only): Reserved
5:4	DVSRATE[1:0]	R/W	0x0	(ISL9123/A only): Dynamic Voltage Scaling slew rate applied when the output voltage setting is changed 0x0 = 3.125mV/µs 0x1 = 6.25mV/µs 0x2 = 0.78125mV/µs 0x3 = 1.5625mV/µs
			0x1	(ISL9123B only): Dynamic Voltage Scaling slew rate applied when the output voltage setting is changed 0x0 = 0.625mV/µs 0x1 = 1.25mV/µs 0x2 = 0.15625mV/µs 0x3 = 0.3125mV/µs
3:2	FMODE[1:0]	R/W	0x0	Forced operating modes 0x0 = Normal operation with automatic mode transitions 0x1 = RESERVED. Do Not Use this combination 0x2 = Forced PWM mode with no PFM operation (ISL9123/A only): 0x3 = Forced bypass. Disables switching. If the Forced Bypass mode is selected and the part is disabled over I^2C (CONV_CFG[7] = EN_AND = 0x0), the converter remains in Forced Bypass (ISL9123B only): 0x3 = RESERVED. **DO NOT USE** this combination.
1	CONV_RSVD	R/W	0x0	Reserved
0	TYPE1	R/W	0x1	0x0 = Type I error amplifier for best transient response with voltage positioning 0x1 = Type II error amplifier for best steady state voltage accuracy. **DO NOT USE** Type II error amplifier if overcurrent fault handling is disabled (INTFLG_MASK[7] = OC_FAULT_MODE = 0x2 or 0x3)

6.5 INTFLG_MASK

The INTFLG_MASK register settings are described in Table 6.

Table 6. Register Address 0x13: INTFLG_MASK

Bit	Name	Type	Reset	Description
7:6	OC_FAULT_MODE	R/W	0x0	Overcurrent fault handling modes 0x0 = Hiccup mode with 100ms wait 0x1 = Shutdown mode. Requires restart over I^2C or EN pin 0x2 = Current limit with no fault action taken. USE ONLY with Type I error amplifier (CONV_CFG[0] = TYPE1 = 0x0) 0x3 = Reserved. USE ONLY with Type I error amplifier (CONV_CFG[0] = TYPE1 = 0x0)
5[1]	AUX_SW	R/W	0x0	(ISL9123/A only): Auxiliary switched output control 0x0 = VSW pin disconnected 0x1 = VSW pin connected to the VOUT pin by power switch
	Reserved			(ISL9123B only): Reserved
4	EN_OR	R/W	0x0	Enable override bit for I^2C control of the converter. Implements push-button ON operation; the button pulls EN high and the part starts. If EN_OR is set from OTP or over I^2C, the part remains enabled when the button is released. 0x0 = Controlled by the EN pin 0x1 = Held in enable state - EN pin is ignored

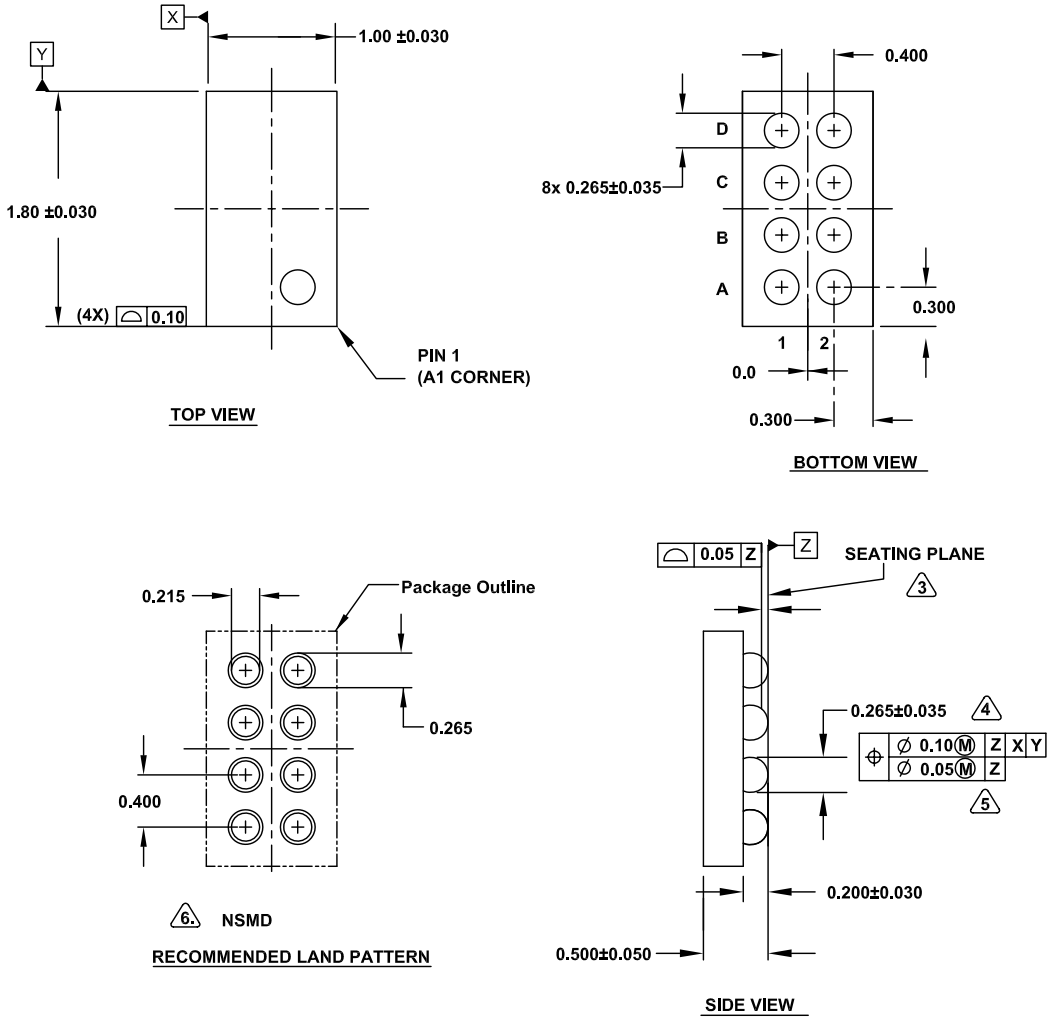
1. For part specific default differences, see Part Number Differences section.

7. Package Outline Drawings

For the most recent package outline drawing, see W2x4.8.

W2x4.8

8 Ball Wafer Level Chip Scale Package (WLCSP) 0.4mm Pitch
Rev 0, 6/17



NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASMEY 14.5-1994
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
5. Bump position designation per JESD 95-1, SPP-010.
6. NSMD refers to non-solder mask defined pad design per Intersil Techbrief. http://www.intersil.com/data/tb/tb451.pdf

8. Ordering Information

Part Number[1]	Part Marking	Default V_{OUT} (V)	I^2C Address	Package Description[2] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp Range
ISL9123IINZ-T[4]	9123	3.0V	0x1C	8 Bump WLCSP	W2x4.8	Reel, 3k	-40 to +85°C
ISL9123IICZ-T[4]	C123	1.8V					
ISL9123II4Z-T[4]	1234	1.0V					
ISL9123II2Z-T[4]	1233	2.1V	0x1C	8 Bump WLCSP	W2x4.8	Reel, 3k	-40 to +85
ISL9123IITZ-T[4]	2319	1.9V	0x1C	8 Bump WLCSP	W2x4.8	Reel, 3k	-40 to +85
ISL9123AIICZ-T[4]	23AC	1.8V	0x1D	8 Bump WLCSP	W2x4.8	Reel, 3k	-40 to +85°C
ISL9123BII7Z-T[4]	123B	0.7V	0x1E	8 Bump WLCSP	W2x4.8	Reel, 3k	-40 to +85°C
ISL9123BII9Z-T[4]	1239	0.88V					
ISL9123IIC-EVZ	Evaluation Board for the ISL9123IICZ						
ISL9123IIN-EVZ	Evaluation Board for the ISL9123IINZ						
ISL9123AIIC-EVZ	Evaluation Board for the ISL9123AIICZ						
ISL9123BII9-EVZ	Evaluation Board for the ISL9123BII9Z						

1. For Moisture Sensitivity Level (MSL), see the ISL9123, ISL9123A, and ISL9123B device pages. For more information about MSL, see TB363.
2. For the Pb-Free Reflow Profile, see TB493.
3. See TB347 for details about reel specifications.
4. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.

Table 7. Key Differences Between Family of Parts

Part	Topology	V_{OUT} Setting Range (V) / Step Size (mV)	Base I^2C Address	Forced/Auto Bypass	r_{DISCHG} present on V_{OUT} when EN = LOW and V_{IN} = HIGH
ISL9123	Buck	0.4 to 5.375 / 25mV	0x1C	Yes	Yes
ISL9123A	Buck	0.4 to 5.375 / 25mV	0x1D	Yes	No
ISL9123B	Buck	0.4 to 1.180 / 5mV	0x1E	No	Yes (weak)

9. Part Number Differences

This datasheet describes the common ISL9123/A/B devices and settings. Specific part numbers with further default or implementation differences relative to this are outlined in the following sections.

9.1 ISL9123II2Z and ISL9123IITZ

9.1.1 Register Map Detail

Summary of differences:

- Auxiliary switch: VSW pin connected to VOUT

Table 8. Register Address 0x13: INTFLG_MASK

Bit	Name	Type	Reset	Description
5	AUX_SW	R/W	0x1	Auxiliary switched output control 0x0 = VSW pin disconnected 0x1 = VSW pin connected to the VOUT pin by power switch

10. Revision History

Rev.	Date	Description
3.03	Nov 15, 2023	Added ISL9123II2Z and ISL9123IITZ information. Added Part Number Differences section.
3.02	Aug 17, 2023	Updated the Protocol Conventions and Read Operation sections.
3.01	Jul 26, 2023	Added ISL9123B information throughout. Corrected notes on thermal information table. Moved ESD and Maximum thermals to the Abs Max section. Added clarification in ISL9123/A pin description table for VSW. Updated the Recommended Operating Conditions section. Updated I2C Serial Interface section. Updated INTFLG_REG section.
3.00	Jan 19, 2023	Applied new template. Added ISL9123A information throughout datasheet. Updated features for efficiency, peak efficiency, and output current. Removed ultrasonic mode. Updated Figure 1. Updated pin descriptions for D1 and D2, WLCSP. Updated Absolute Maximum Ratings, added LX (less than 10ns). Updated Recommended Operating Conditions section. Updated Analog Specification by updating the following: Test Conditions: VIN Supply Current, Shutdown, VIN Supply Current, Forced Bypass Mode, VOUT Soft Discharge ON-Resistance, Switching frequency, Hiccup Time Changed Typical value: Peak Current Limit (2nd line) Removed Output Current specifications. UpdatedI2C Frequency Capability specification by removing typical and added min and max value. Updated parameters for 3 Typical Performance Curves. Updated Figure 10 and Figure 18 through Figure 24. Updated Enable Input, Overcurrent/Short-Circuit Protection, Pulse Width Modulation (PWM) Operation, Pulse Frequency Modulation (PFM) Operation, Forced Operating Modes, and Protocol Conventions sections. Updated Table 3 and 6. Clarified Cout = 6uF minimum effective capacitance required (throughout file). Added “Auxiliary Output” information section, and updated Pg1 Features Update/clarify register descriptions in sections 5.x as needed for ISL9123 and ISL9123A Added hyperlink to “Recommended Operating Conditions” section in VSET section 5.3 Updated Block Diagram to show Bypass Updated wording in I2C section Updated Ordering information table Removed DFN package option information throughout. Removed ISL9123II7Z-T from the ordering information table.

Rev.	Date	Description
2.00	Jan 20, 2021	Added DFN package option information throughout. Added ISL9123II7Z-T to the ordering information table.
1.00	Sep 11, 2019	Changed the minimum values to typical values for the Maximum Load Current and Maximum Load Current at Low Vin specifications. Removed the bolding on the Output Voltage Accuracy specifications minimum and maximum values.
0.00	Aug 26, 2019	Initial release

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