HA13159

37 W × 4-Channel BTL Power IC

HITACHI

ADE-207-264 (Z)
1st Edition
Sept. 1, 1998

Description

The HA13159 is four-channel BTL amplifier IC designed for car audio, featuring high output and low distortion, and applicable to digital audio equipment. It provides 37 W output per channel, with a 13.7 V power supply and at Max distortion.

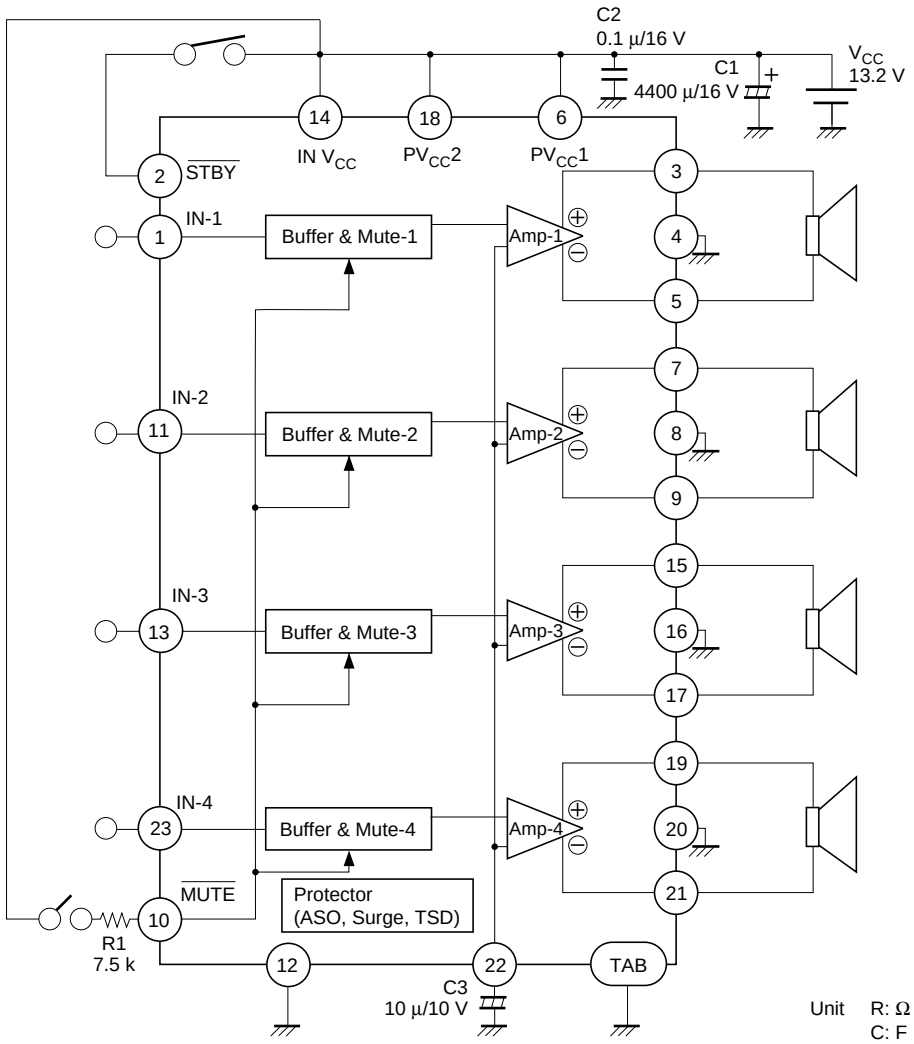
Functions

- 4 ch BTL power amplifiers
- Built-in standby circuit
- Built-in muting circuit
- Built-in protection circuit (surge, T.S.D and ASO)

Features

- Low power dissipation
- Soft thermal limiter
- Requires few external parts (C:3, R:1)
- Popping noise minimized
- Low output noise
- Built-in high reliability protection circuit
- Pin to pin with HA13153A/HA13154A/HA13155/HA13157/HA13158/HA13158A

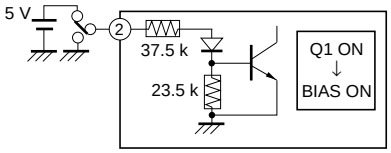
Block Diagram

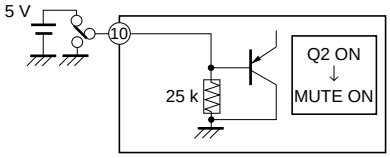


Notes: 1. Standby
Power is turned on when a signal of 3.5 V or 0.05 mA is impressed at pin 2. When pin 2 is open or connected to GND, standby is turned on (output off).

2. Muting
Muting is turned off (output on) when a signal of 3.5 V or 0.2 mA is impressed at pin 10.
When pin 10 is open or connected to GND, muting is turned on (output off).

3. TAB (header of IC) connected to GND.

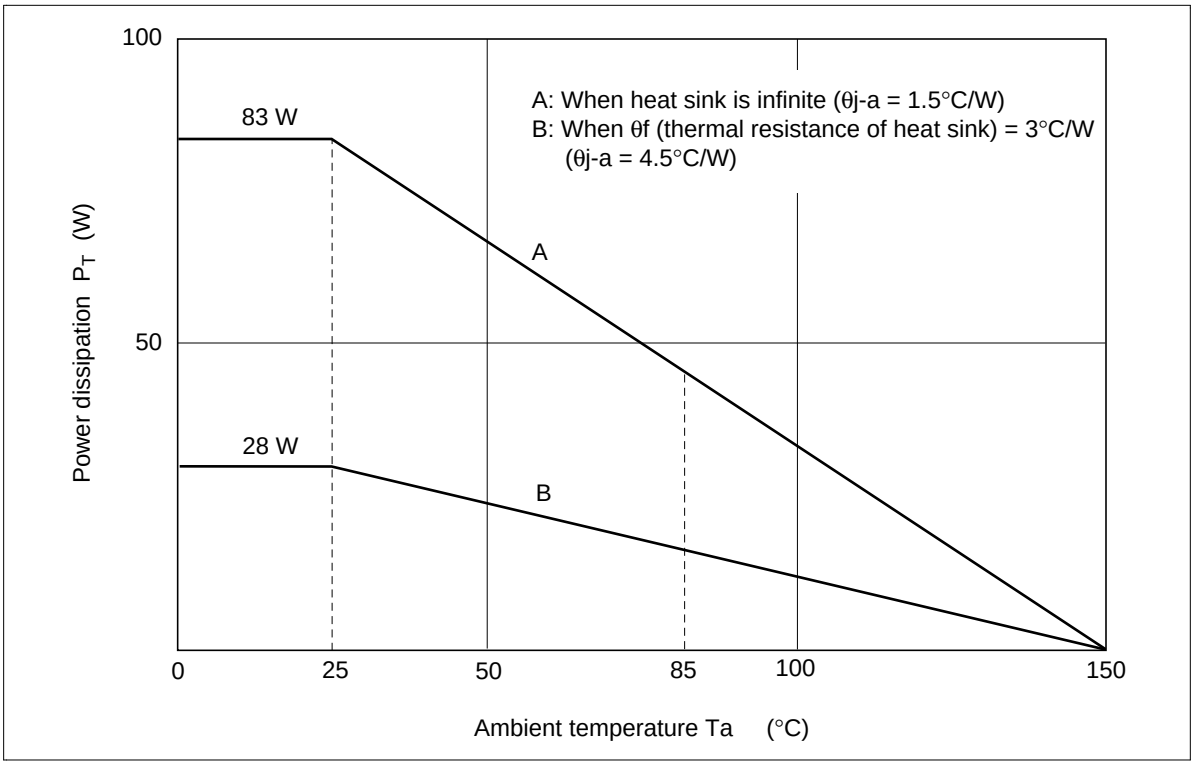




Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Operating supply voltage	V_{CC}	18	V
Supply voltage when no signal*[1]	V_{CC} (DC)	26	V
Peak supply voltage*[2]	V_{CC} (PEAK)	50	V
Output current*[3]	I_O (PEAK)	4	A
Power dissipation*[4]	P_T	83	W
Junction temperature	Tj	150	°C
Operating temperature	Topr	–30 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

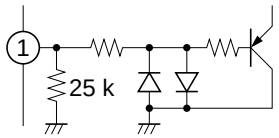
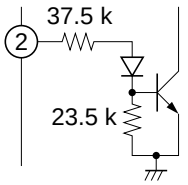
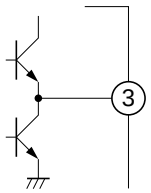
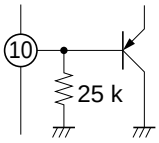
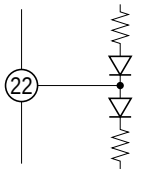
Note: 1. Tolerance within 30 seconds.
2. Tolerance in surge pulse waveform.
3. Value per 1 channel.
4. Value when attached on the infinite heat sink plate at Ta = 25 °C.
The derating carve is as shown in the graph below.



Electrical Characteristics (V_{CC} = 13.2 V, f = 1 kHz, R_L = 4 Ω, Rg = 600 Ω, Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Quiescent current	I_{Q1}	—	220	—	mA	Vin = 0
Output offset voltage	ΔV_Q	–180	0	180	mV	
Gain	G_V	30.5	32	33.5	dB	
Gain difference between channels	ΔG_V	–1.5	0	1.5	dB	
Rated output power	P_O	—	22	—	W	V_{CC} = 13.2 V, THD = 10%, R_L = 4 Ω
Max output power	P_{OMAX}	—	37	—	W	V_{CC} = 13.7 V, R_L = 4 Ω
Total harmonic distortion	T.H.D.	—	0.03	—	%	Po = 3 W
Output noise voltage	WBN	—	0.15	—	mVrms	Rg = 0 Ω, BW = 20 to 20 kHz
Ripple rejection	SVR	—	55	—	dB	f = 120 Hz
Channel cross talk	C.T.	—	70	—	dB	Vout = 0 dBm
Input impedance	Rin	—	25	—	kΩ	
Standby current	I_{Q2}	—	—	10	μA	
Standby control voltage (high)	V_{STH}	3.5	—	V_{CC}	V	
Standby control voltage (low)	V_{STL}	0	—	1.5	V	
Muting control voltage (high)	V_{MH}	3.5	—	V_{CC}	V	
Muting control voltage (low)	V_{ML}	0	—	1.5	V	
Muting attenuation	ATTM	—	70	—	dB	Vout = 0 dBm

Pin Explanation

Pin No.	Symbol	Functions	Input Impedance	DC Voltage	Equivalence Circuit
1	IN1	CH1 INPUT	25 kΩ (Typ)	0 V	
11	IN2	CH2 INPUT			
13	IN3	CH3 INPUT			
23	IN4	CH4 INPUT			
2	$\overline{\text{STBY}}$	Standby control	90 kΩ (at Trs. cutoff)	—	
3	OUT1 (+)	CH1 OUTPUT	—	$V_{CC}/2$	
5	OUT1 (–)				
7	OUT2 (+)	CH2 OUTPUT			
9	OUT2 (–)				
15	OUT3 (+)	CH3 OUTPUT			
17	OUT3 (–)				
19	OUT4 (+)	CH4 OUTPUT			
21	OUT4 (–)				
10	$\overline{\text{MUTE}}$	Muting control	25 kΩ (Typ)	—	
22	RIPPLE	Bias stability	—	$V_{CC}/2$	

Pin Explanation (cont)

Pin No.	Symbol	Functions	Input Impedance	DC Voltage	Equivalence Circuit
6	$PV_{CC}1$	Power of output stage	—	V_{CC}	—
18	$PV_{CC}2$				
14	INV_{CC}	Power of input stage	—	V_{CC}	—
4	CH1 GND	CH1 power GND	—	—	—
8	CH2 GND	CH2 power GND			
16	CH3 GND	CH3 power GND			
20	CH4 GND	CH4 power GND			
12	IN GND	Input signal GND	—	—	—

Point of Application Board Design

1. Notes on Application Board's Pattern Design

- For increasing stability, the connected line of V_{CC} and OUTGND is better to be made wider and lower impedance.
- For increasing stability, it is better to place the capacitor between V_{CC} and GND (0.1 µF) close to IC.
- It is better to place the grounding of resistor (Rg), between input line and ground, close to INGND (Pin 12) because if OUTGND is connected to the line between Rg and INGND, THD will become worse due to current from OUTGND.

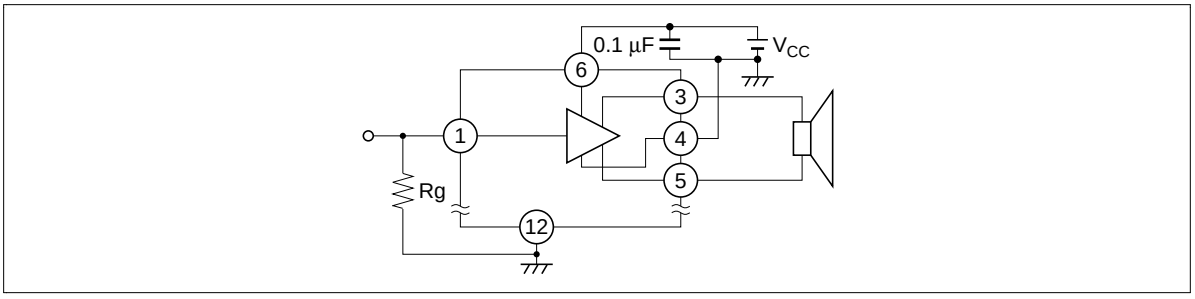


Figure 1 Notes on Application Board's Pattern Design

2. How to Reduce the Popping Noise by Muting Circuit

   At normal operating circuit, Muting circuit operates at high speed under 1 µs.

   In case popping noise becomes a problem, it is possible to reduce the popping noise by connecting capacitor, which determines the switching time constant, between pin 10 and GND. (Following figure 2)

   We recommend value of capacitor greater then 1 µF.

   Also transitional popping noise can be reduced sharply by muting before V_{CC} and Standby are ON/OFF.

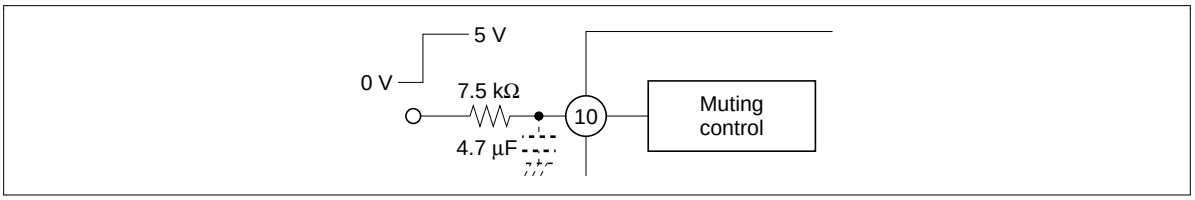


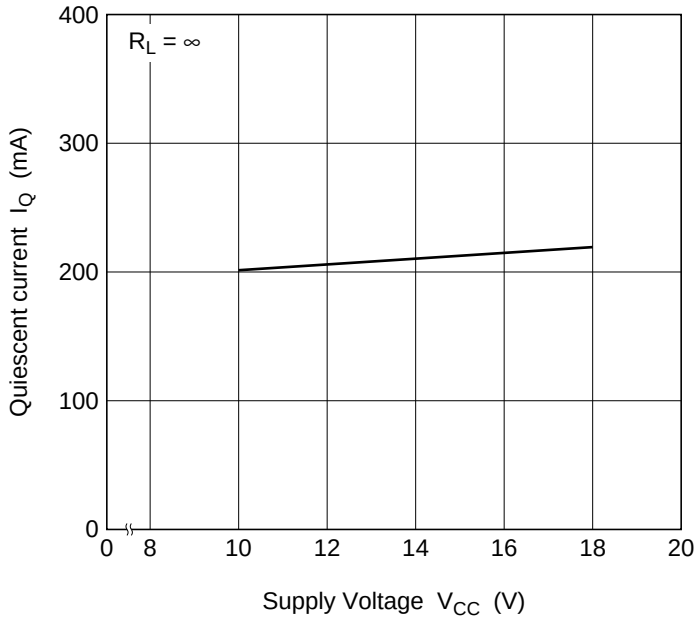
Figure 2 How to use Muting Circuit

Table 1 Muting ON/OFF Time

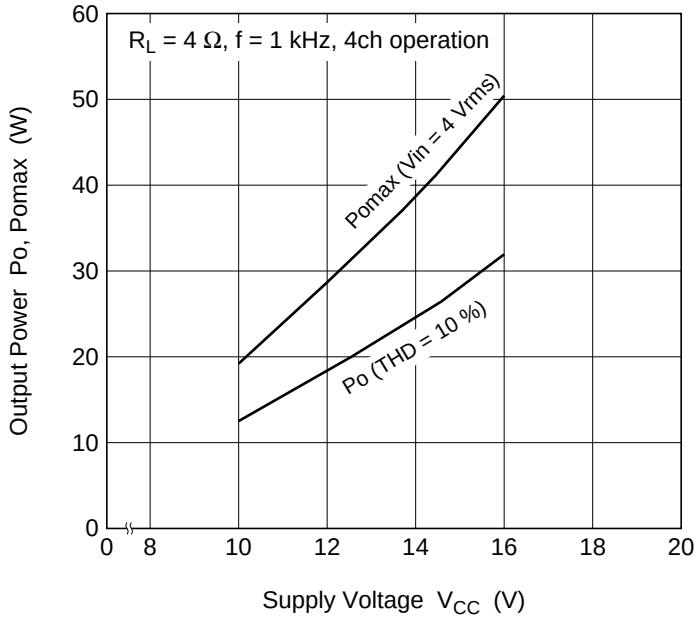
C (µF)	ON Time	OFF Time
nothing	under 1 µs	under 1 µs
0.47	2 ms	2 ms
4.7	19 ms	19 ms

Characteristic Curves

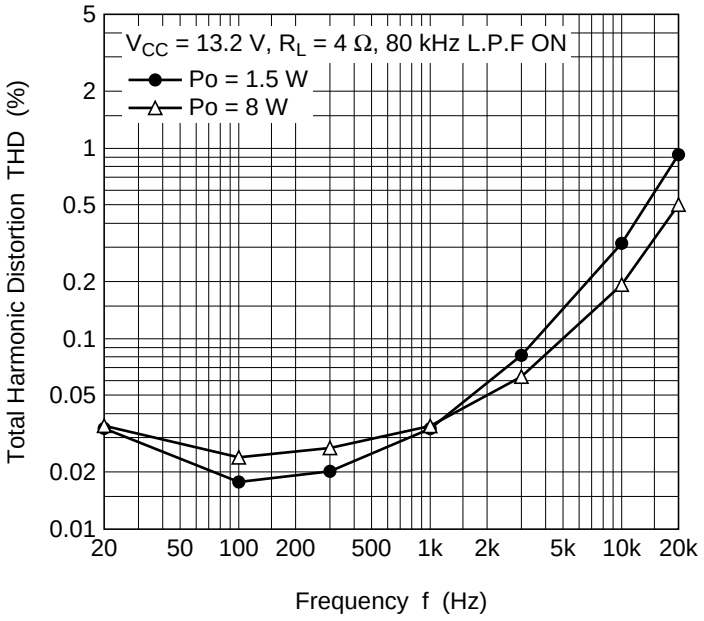
Quiescent current vs. Supply Voltage



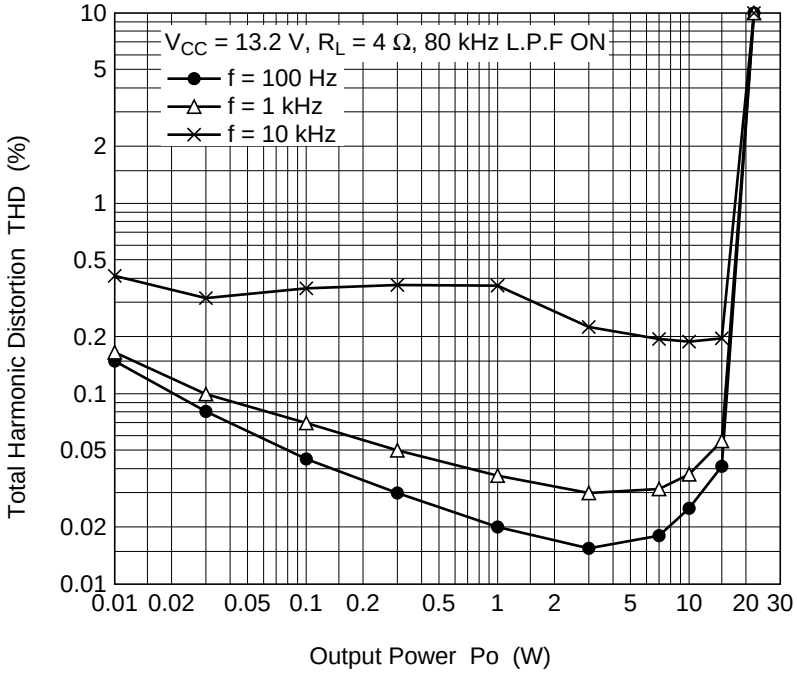
Output Power vs. Supply Voltage



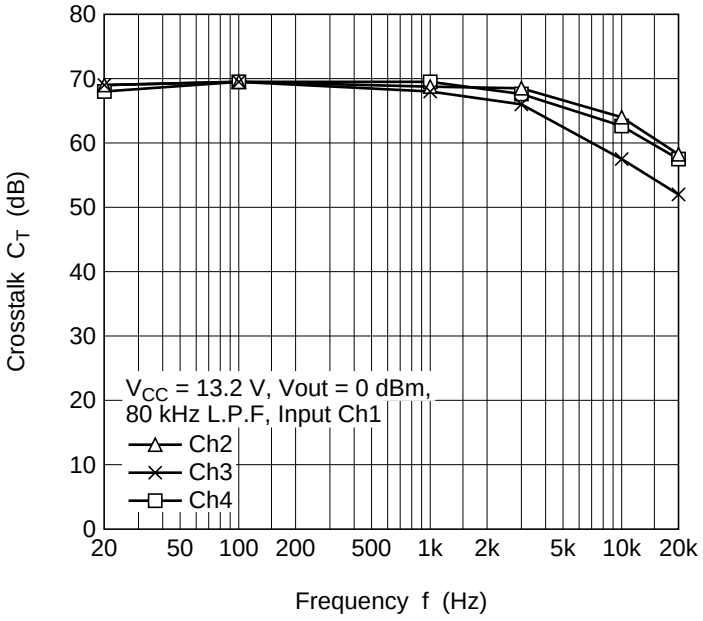
Total Harmonic Distortion vs. Frequency



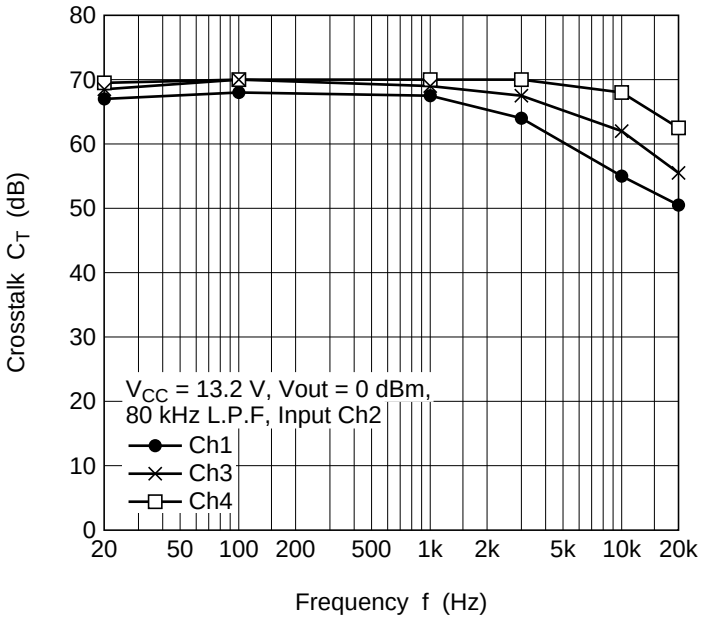
Total Harmonic Distortion vs. Output Power



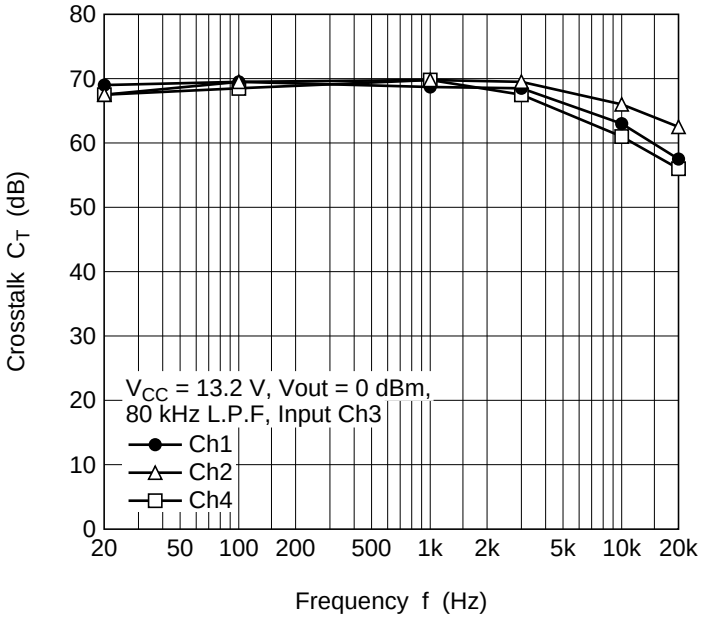
Crosstalk vs. Frequency (1)



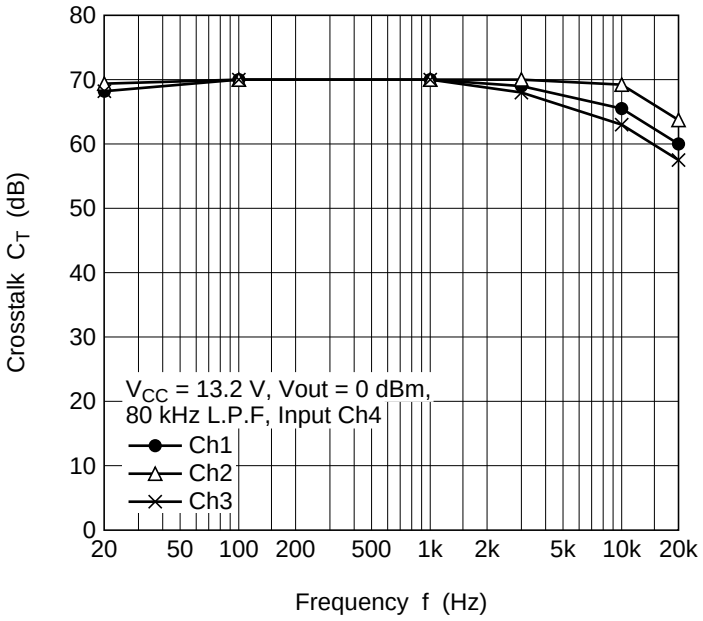
Crosstalk vs. Frequency (2)



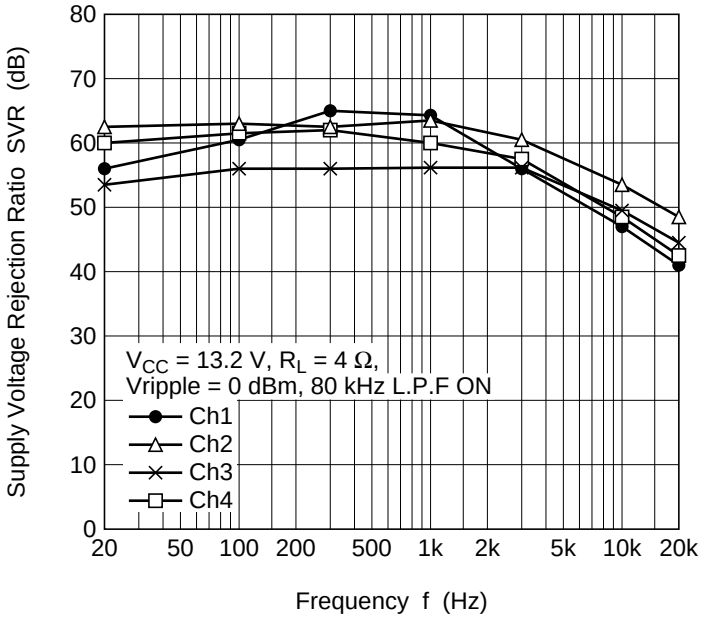
Crosstalk vs. Frequency (3)



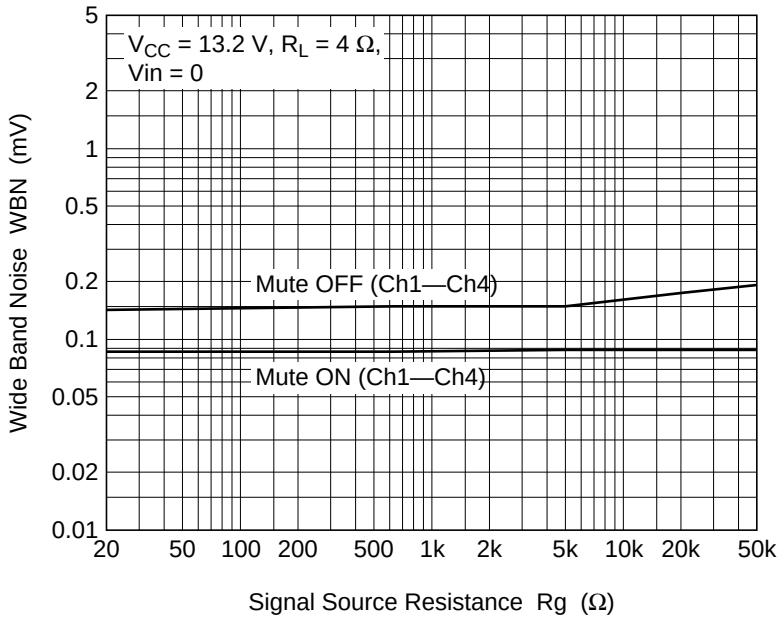
Crosstalk vs. Frequency (4)



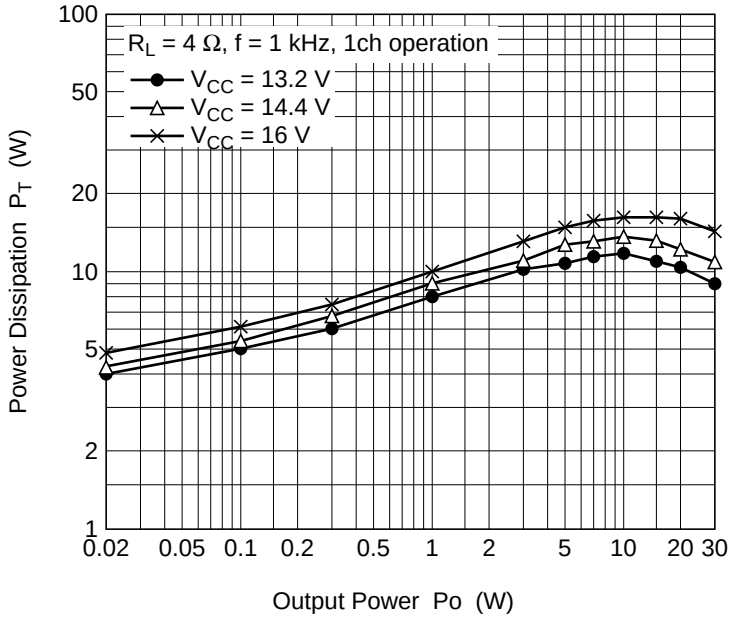
Supply Voltage Rejection Ratio vs. Frequency



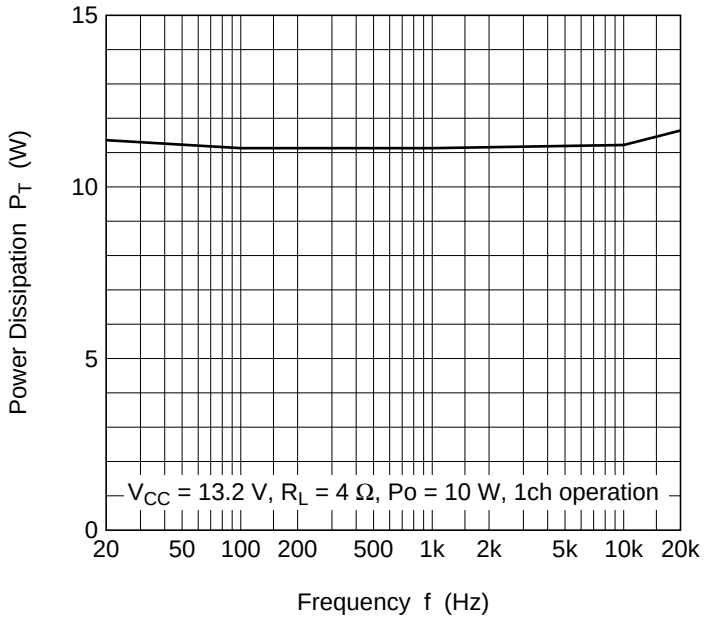
Wide Band Noise vs. Signal Source Resistance



Power Dissipation vs. Output Power

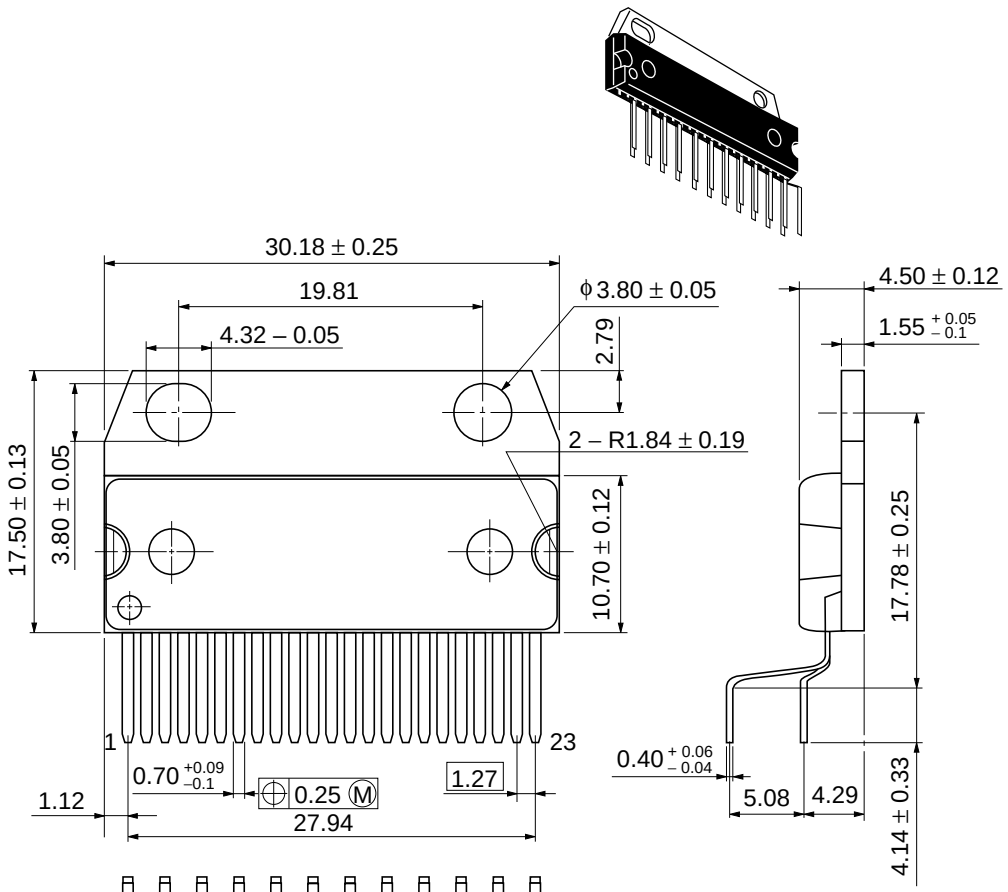


Power Dissipation vs. Frequency



Package Dimensions

Unit: mm



Hitachi Code	SP-23TE
JEDEC	Conforms
EIAJ	—
Weight (reference value)	8.5 g

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