RENESAS

M62342HP

8-Bit, 2-Channel D/A Converter (Buffered)

Description

The M62342HP is a CMOS-structure semiconductor integrated circuit incorporating two 8-bit D/A converter channels with output buffer op-amps.

Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD.

Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink and source, and can operate over the entire voltage range from almost ground to V_{CC} (0 to 5 V), making peripheral elements unnecessary and enabling configuration of a system with few component parts.

This product is currently under development, and specifications and other details may be modified at a future date.

Features

- Data transfer format
  10-bit serial data input type
- Output buffer op-amps
  Operable over entire voltage range from almost ground to V_{CC} (0 to 5 V)
- High output current capacity
  ±1 mA or higher

Application

Signal gain setting and automatic adjustment in DSC, CTV, and display monitors, conversion from digital data to analog data in consumer and industrial products

Block Diagram

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Pin Arrangement

M62342HP

A_{O1}	1		8	LD
A_{O2}	2		7	CLK
N.C	3		6	DI
V_{CC}	4		5	GND

(Top view)　　　N.C: Not connected

Outline: PRSP0008JA-A (8P2X-F)
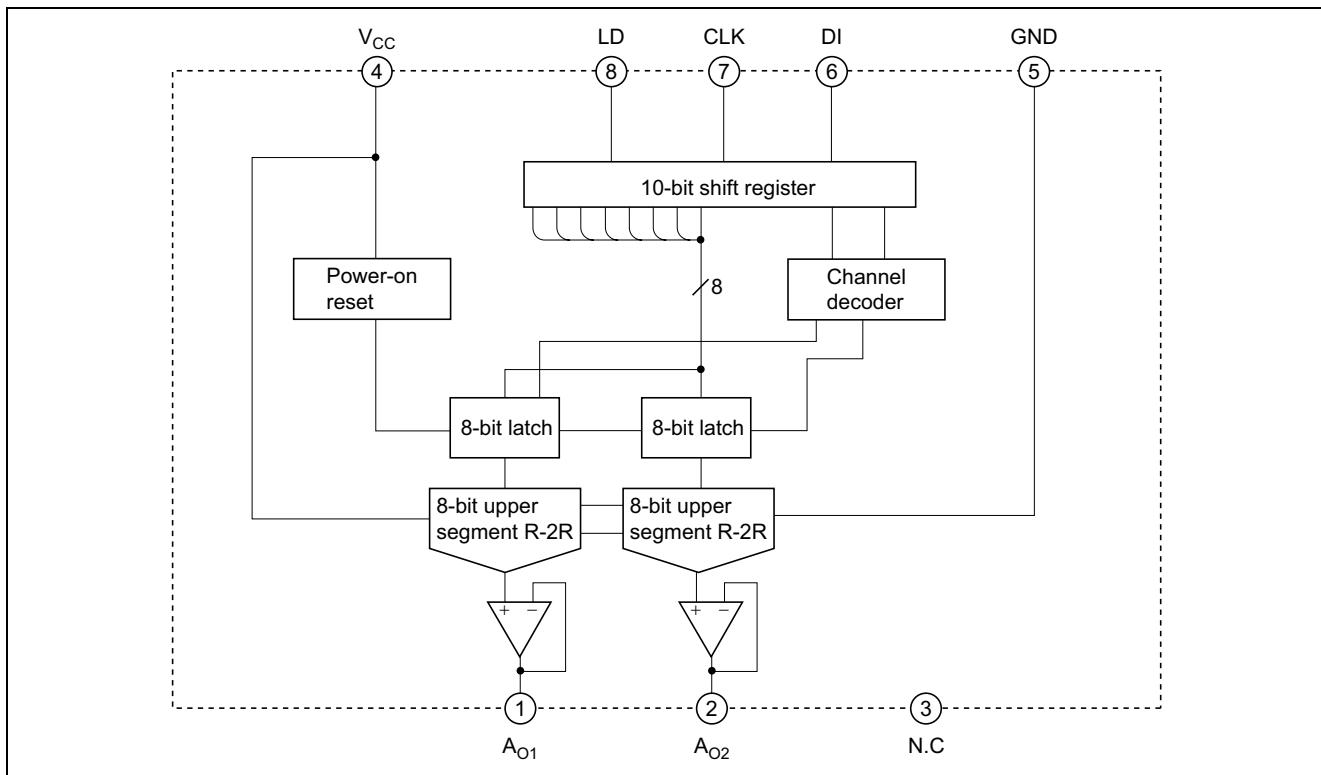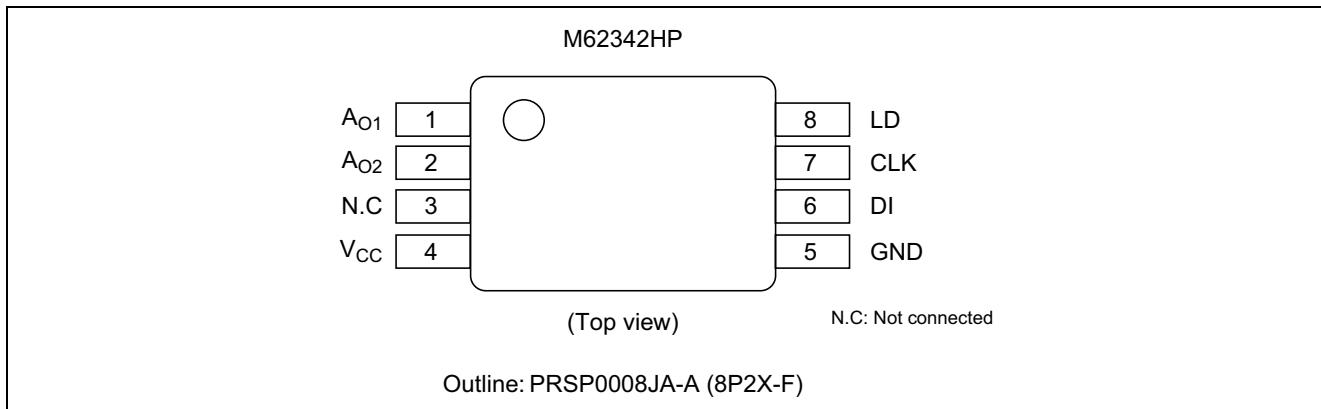
Pin Description

Pin No.	Symbol	Function
6	DI	Serial data input pin. Inputs serial data with a 10-bit data length.
7	CLK	Serial clock input pin. Input signal from DI pin is input to 10-bit shift register at rise of shift clock.
8	LD	Load pin. When "H" level is input to LD pin, value in 10-bit shift register is loaded into decoder and D/A output register.
1	A_{O1}	8-bit resolution D/A converter output pins
2	A_{O2}	(After power-on, all channels are reset and DAC data 00h is output.)
3	N.C.	(Not connected)
4	V_{CC}	Power supply voltage pin
5	GND	GND pin

Absolute Maximum Ratings

Item	Symbol	Rated Value	Unit
Power supply voltage	V_{CC}	−0.3 to 7.0	V
Input voltage	Vin	−0.3 to V_{CC}+0.3 ≤ 7.0	V
Output voltage	Vo	−0.3 to V_{CC}+0.3 ≤ 7.0	V
Internal power consumption	Pd	200	mW
Operating ambient temperature	Topr	−20 to +85	°C
Storage temperature	Tstg	−40 to +125	°C

Electrical Characteristics

(Unless specified otherwise, V_{CC} = +5 V ±10%, GND = 0 V, Ta = -20ºC to 85ºC)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Power supply voltage	V_{CC}	2.7	5.0	5.5	V	
Power supply current	I_{CC}	—	0.7	2.5	mA	At CLK = 1 MHz operation, I_{AO} = 0 µA D/A data: 6 Ah (at maximum current)
		—	0.5	1.6		DI = CLK = LD = GND, I_{AO} = 0 µA
Input leakage current	I_{ILK}	−10	—	10	µA	V_{IN} = 0 to V_{CC}
Input voltage "L"	V_{IL}	0	—	$0.2V_{CC}$	V	
Input voltage "H"	V_{IH}	$0.5V_{CC}$	—	V_{CC}	V	
Buffer amp output voltage range	V_{AO}	0.1	—	V_{CC}−0.1	V	I_{AO} = ±100 µA
		0.1	—	V_{CC}−0.2		I_{AO} = ±500 µA
Buffer amp output drive range	I_{AO}	−1.0	—	1.0	mA	Upper saturation voltage = 0.3 V Lower saturation voltage = 0.2 V
Differential nonlinearity error	S_{DL}	−1.0	—	1.0	LSB	V_{CC} = 5.12 V (20 mV/LSB) No load (I_{AO} = 0)
Nonlinearity error	S_L	−1.5	—	1.5	LSB	
Zero point error	S_{ZERO}	−2.0	—	2.0	LSB	
Full-scale error	S_{FULL}	−2.0	—	2.0	LSB	
Oscillation limit output capacitance	C_O	—	—	0.1	µF	
Buffer amp output impedance	R_O	—	5.0	—	Ω	

AC Characteristics

(Unless specified otherwise, V_{CC} = +5 V ±10%, GND = 0 V, Ta = -20ºC to 85ºC)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Clock "L" pulse width	t_{CKL}	200	—	—	ns	
Clock "H" pulse width	t_{CKH}	200	—	—	ns	
Clock rise time	t_{CR}	—	—	200	ns	
Clock fall time	t_{CF}	—	—	200	ns	
Data setup time	t_{DCH}	30	—	—	ns	
Data hold time	t_{CHD}	60	—	—	ns	
Load setup time	t_{CHL}	200	—	—	ns	
Load hold time	t_{LDC}	100	—	—	ns	
Load "H" pulse width	t_{LDH}	100	—	—	ns	
D-A output settling time	t_{LDD}	—	—	300	µs	Until output reaches last 1/2 LSB

Timing Chart

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Digital Data Format

Last
LSB ——————————————————————→ First
MSB

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9

←———————————— For D/A output ————————————→ ← for channel →
address
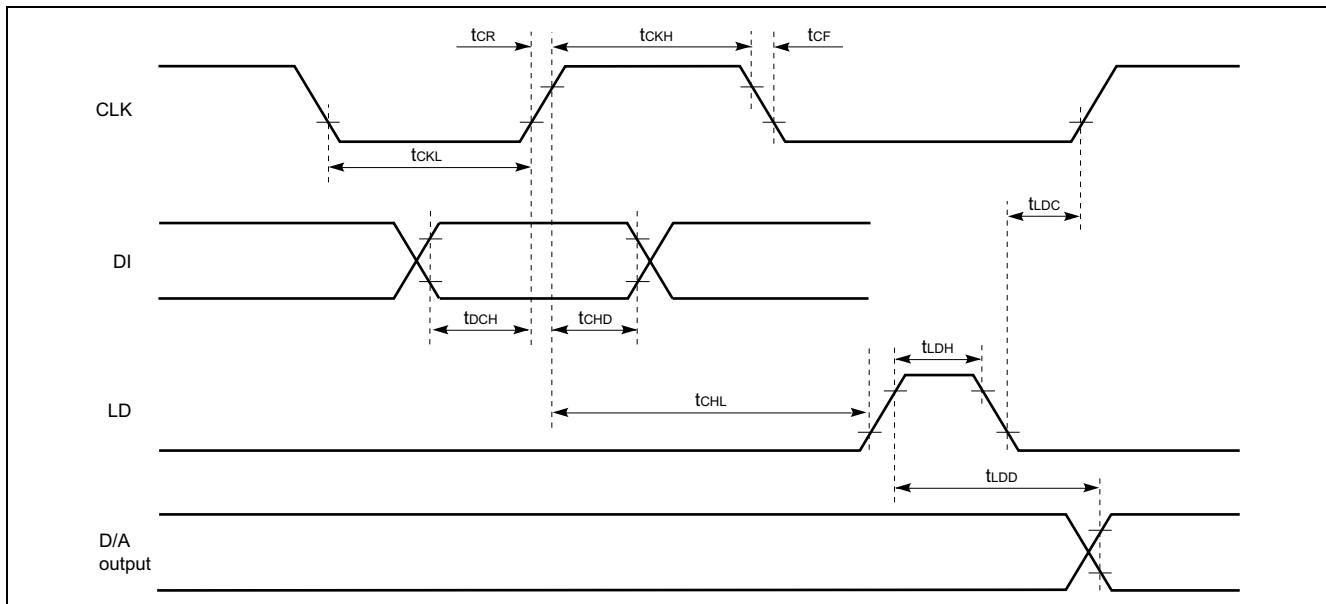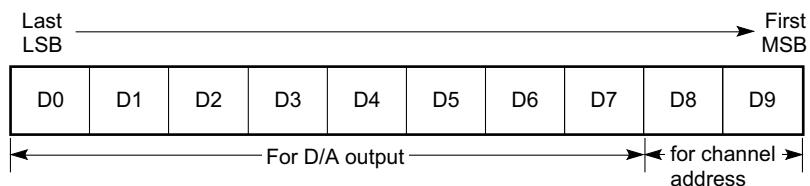
D/A Data

D0	D1	D2	D3	D4	D5	D6	D7	D-A output
0	0	0	0	0	0	0	0	$V_{CC}/256 \times 1$
1	0	0	0	0	0	0	0	$V_{CC}/256 \times 2$
0	1	0	0	0	0	0	0	$V_{CC}/256 \times 3$
1	1	0	0	0	0	0	0	$V_{CC}/256 \times 4$
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	$V_{CC}/256 \times 255$
1	1	1	1	1	1	1	1	$V_{CC}/256 \times 256$

Channel Select Data

D8	D9	Channel Selection
0	0	AO1 selected
1	0	AO2 selected
0	1	Don't care
1	1	Don't care

Data Timing Chart (Model)
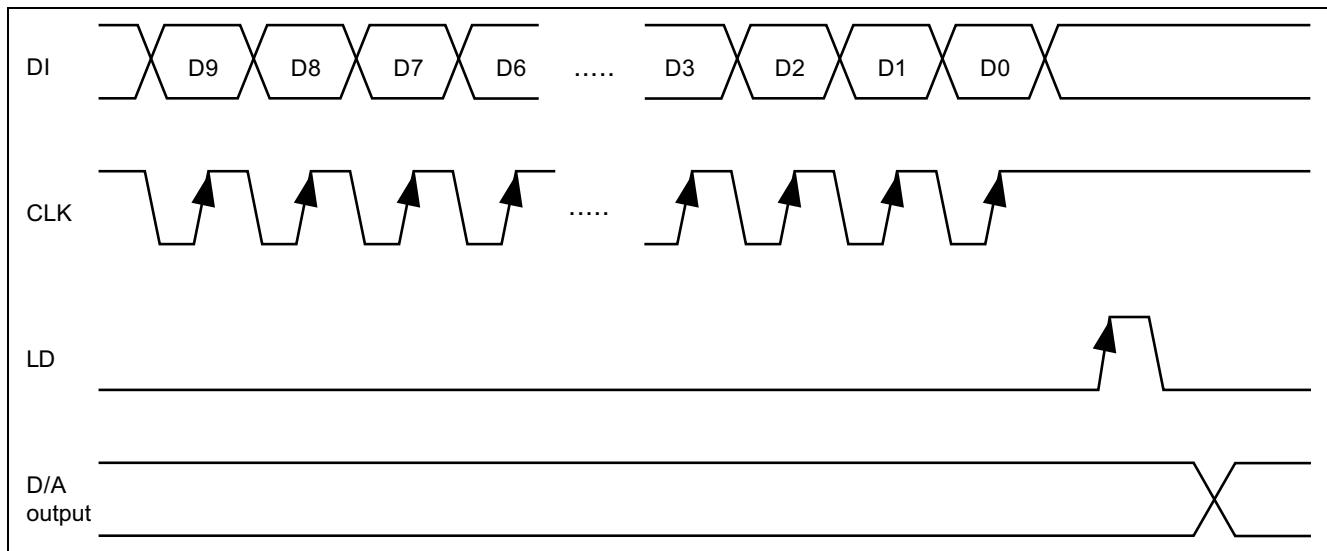
Usage Notes

1. With this IC, D/A converter upper reference voltage setting is performed by means of the power supply voltage. If ripples or spikes are imposed on this pin, conversion accuracy may fall. When using this IC, a capacitor must be inserted between the power supply pin and GND in order to ensure stable D/A conversion.
2. The output buffer amps of this IC are highly tolerant of capacitive loads. Therefore, connecting capacitors (0.1 µF max.) between the output pins and ground in order to eliminate jitter or noise due to output line wiring presents no problems whatever in terms of operation.

Sample Standard Application Circuit
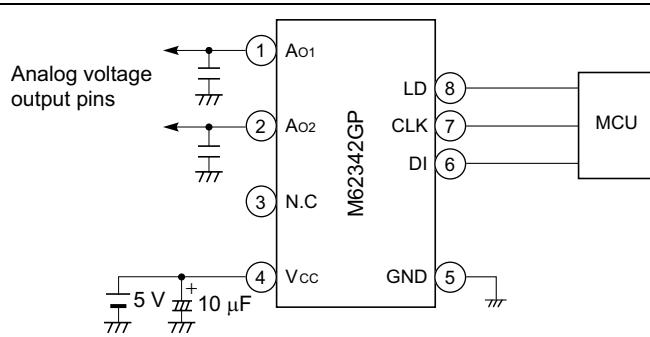
Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SOP-8	P-SOP8-2.8 × 2.9-0.65	PRSP0008JA-A	8P2X-F	0.022g
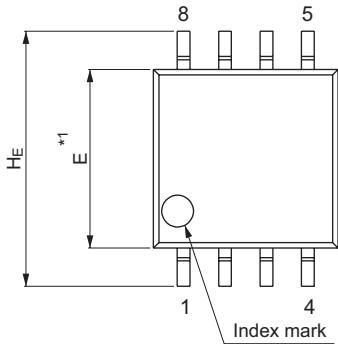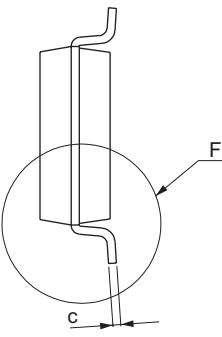
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
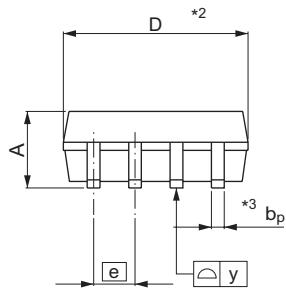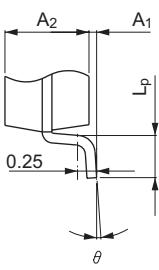
Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	2.8	2.9	3.1
E	2.6	2.8	3.0
A₂	—	1.1	—
A₁	0.05	0.10	0.20
A	—	—	1.4
bₚ	0.1	0.2	0.3
c	0.077	0.127	0.227
θ	0°	—	10°
H_E	3.7	4.0	4.3
e	—	0.65	—
y	—	—	0.1
Lₚ	0.35	0.55	0.75

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