# N-Channel 100-V (D-S) 175°C MOSFET

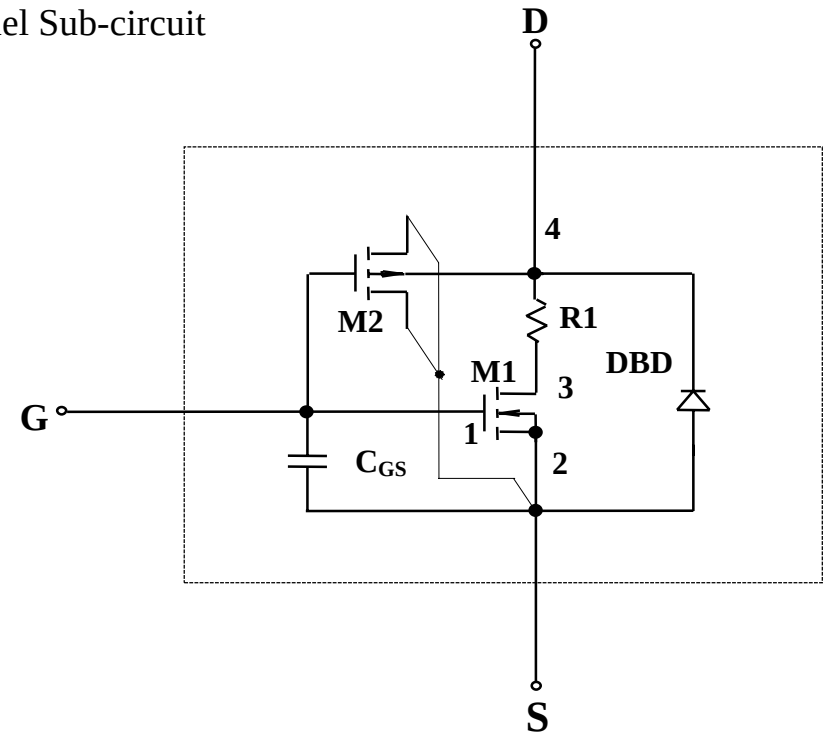
## Characteristics

- N-channel Vertical DMOS
- Macro-Model (Sub-circuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

## Description

The attached SPICE Model describes typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model was extracted and optimized over a -55°C to 125°C temperature range under pulse conditions for 0 to 10 volts gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold voltage. A novel gate-to-drain feedback capacitor network is used to model gate charge characteristics while avoiding convergence problems of switched $C_{gd}$ model. Model parameter values are optimized to provide a best fit to measure electrical data and are not intended as an exact physical description of a device.

## Model Sub-circuit




This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

## Model Evaluation

N-Channel Device ($T_J$=25°C Unless Otherwise Noted)

| Parameter | Symbol | Test Conditions | Measured | Typical | Unit |
|---|---|---|---|---|---|
| **Static** | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$= 250µA | **1.9** | | V |
| On-State Drain Current [a] | $I_{D(on)}$ | $V_{DS}$ = **5**V, $V_{GS}$ = **10**V | **588** | | A |
| Drain-Source On-State Resistance [a] | $r_{DS(on)}$ | $V_{GS}$ = **10**V, $I_D$ = **30**A | **0.0083** | 0.0085 | Ω |
| | | $V_{GS}$ = **10**V, $I_D$ = **30**A, $T_J$ = 125°C | **0.014** | | |
| | | $V_{GS}$ = **10**V, $I_D$ = **30**A, $T_J$ = 175°C | **0.017** | | |
| Forward Transconductance [a] | $g_{fs}$ | $V_{DS}$ = **15**V, $I_D$ = **30**A | **84** | | S |
| Diode Forward Voltage [a] | $V_{SD}$ | $I_F$ = **85**A, $V_{GS}$ = 0V | **0.92** | 1.0 | V |
| **Dynamic** [b] | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0V, $V_{DS}$ = 25V, f = 1MHz | **6376** | 6550 | pF |
| Output Capacitance | $C_{oss}$ | | **765** | 665 | |
| Reverse Transfer Capacitance | $C_{rss}$ | | **290** | 265 | |
| Total Gate Charge [b] | $Q_g$ | $V_{DS}$ = **50**V, $V_{GS}$ = **10**V, $I_D$ = **85**A | **106** | 105 | nC |
| Gate-Source Charge [b] | $Q_{gs}$ | | **17** | 17 | |
| Gate-Drain Charge [b] | $Q_{gd}$ | | **23** | 23 | |
| Turn-On Delay Time [b] | $t_{d(on)}$ | $V_{DD}$ = **50**V, $R_L$ = **0.6**Ω $I_D$ ≅ **85**A, $V_{GEN}$ = **10**V, $R_G$ = **2.5**Ω | **22** | 12 | ns |
| Rise Time [b] | $t_r$ | | **32** | 90 | |
| Turn-Off Delay Time [b] | $t_{d(off)}$ | | **89** | 55 | |
| Fall Time [b] | $t_f$ | | **105** | 130 | |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = **85**A, di/dt=100A/µs | **85** | 85 | |

Notes:
a) Pulse test; pulse width ≤ 300 µsec, duty cycle ≤ 2%
b) Independent of operating temperature
c) Guaranteed by design, not subject to production testing

Comparison of Model with Measured Data
($T_J$=25°C Unless Otherwise Noted)